

# Nonlinear Electronic Transport and Device Performance of HEMTs

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**Abstract**—We assess the impact of nonlinear electronic transport and, in particular, of real space transfer (RST) on device performance for advanced III/V high electron mobility transistors (HEMTs) using the device simulator MINIMOS-NT. In this context, we discuss dc and RF performance issues for pseudomorphic AlGaAs/InGaAs/GaAs HEMTs that are especially relevant for gate-lengths of about 150 nm. All results are compared to and found to be consistent with experimental data for devices processed in two different foundries.

**Index Terms**—Electron emission, equivalent circuits, MODFETs, semiconductor heterojunctions, simulation, simulation software, thermionic emission.

## I. INTRODUCTION

IN RECENT years high electron mobility transistors (HEMTs) have been developed with respect to low noise, power, and mm-wave MMIC applications and find increasing interest in standard processes on an industrial scale. It is the purpose of this paper to show the correlation between electronic transport and device performance of HEMTs. This is accomplished by the application of the device simulator MINIMOS-NT which is capable of dealing with the concurrent effects of real space transfer (RST), k-space transfer (KST), and velocity overshoot. The theoretical understanding obtained supports the device design for relevant markets, e.g., for local multipoint distribution systems (LMDS) in the Ka-band or the automotive collision avoidance radar in the W-band.

Many questions have been raised regarding HEMT performance [1]–[3], and can be answered by our simulations. We base our investigation on the achievements of HEMT performance reported by various foundries, e.g., [4]–[7].

MINIMOS-NT is capable of linking the physics of hetero-interfaces to the small-signal equivalent circuit elements that explain device performance beyond classical HEMT theory.

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The questions concerning the electronic transport become crucial as gate-lengths approach the sub-100 nm range [8] and high field transport phenomena are enhanced. These questions cannot be explored by analytical models. At instances a more complex device simulator such as the particle simulator DAMOCLES [9] was used to confirm, e.g., the interdependences of real space transfer and velocity overshoot, which are found by MINIMOS-NT. The paper is organized as follows: Section II gives a brief overview of the impact of relevant electronic transport issues on HEMT performance. Section III describes how these aspects are included into the two-dimensional device simulation of MINIMOS-NT and Monte Carlo simulations. In Section IV results are given with focus on nonlinear transport as highlighted by these results.

## II. TRANSPORT ISSUES TO HEMT PERFORMANCE

As a significant figure of merit, Fig. 1 shows the product of current gain cut-off frequency and gate-length  $f_T \times l_g$  as a function of gate-length  $l_g$  taken from literature (see also [10]) for GaAs based MESFETs, pseudomorphic AlGaAs/InGaAs/GaAs HEMTs, and InAlAs/InGaAs HEMTs on InP substrate. The lines represent the product that we consider to be realistic for a gate-length of  $l_g = 150$  nm for the given technology, and that, contrary to simplified models, is not constant. From the perspective of transport we observe two basic issues:

- the speed superiority of devices with high indium content in the channel;
- the increasing importance of the (parasitic) environment of the channel for decreasing gate-length, especially below  $l_g = 100$  nm.

To assess the reasons for the speed advantage of high indium content in the active region, a detailed review of factors that influence FET performance is presented in [11]. Yet, even with regard to publications which present a very conservative view of the advantages of low field effects such as velocity overshoot, we make the following observations: An effective carrier velocity of  $1.59 \times 10^7$  cm/s was extracted from a pseudomorphic HEMT (for an indium content  $x = 0.05$  in the channel) [12]. Ref. [13] (for an indium content of  $x = 0.25$ ) claimed the relative independence of the extracted delay times with respect to the channel material composition, but at the same time they found an effective carrier velocity of about  $1.5 - 2 \times 10^7$  cm/s. Ref. [14] obtained an effective carrier velocity of  $3.1 \times 10^7$  cm/s from channel delay for an indium content of  $x = 0.53$  and pseudomorphic indium inclusions. Reviewing various measurements of the saturated velocity at electric fields of 100 kV/cm

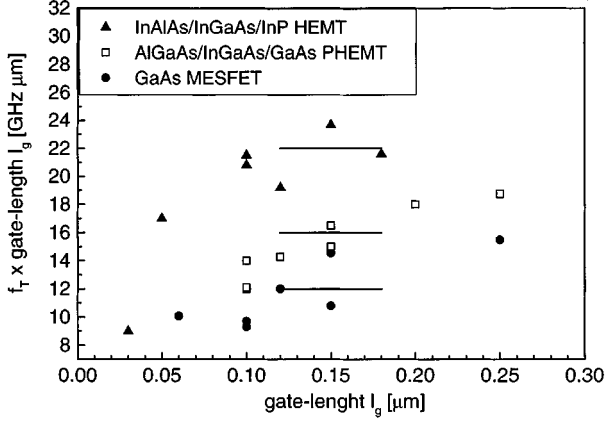


Fig. 1. Overview of the product current gain cut-off frequency  $f_T$  and gate-length  $l_g$  as a function of gate-length  $l_g$ .

and above in bulk materials, these extracted saturation velocities (even in  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ) are generally lower than  $10^7$  cm/s, e.g., [15]. We conclude from these and various other observations [11], that an effective mean carrier velocity prevails above the saturated bulk velocity, which contradicts simplified analytical models. This work can show for realistic devices that for the definition of this effective value the interdependence of RST and KST has to be taken into account, since RST is a limiting factor for overshoot phenomena [11].

When investigating the gate-source bias dependence of extracted  $S$ -parameters of pseudomorphic AlGaAs/InGaAs/GaAs HEMTs [16], [17] defined the term modulation efficiency. It describes the ability of the gate contact to modulate the drain current without modulating immobile or low-velocity charge in the AlGaAs barrier. Thus, modulation efficiency is another way of quantifying the occurrence of RST from the channel into the AlGaAs barrier with limited transport properties.

In [18] Monte Carlo simulations demonstrated RST as a limiting factor for AlGaAs/GaAs HEMT device performance. We can show the importance of the equilibrium of RST and KST, since this work links both, to insight of the high field transport phenomena on the small-signal performance of AlGaAs/InGaAs/GaAs HEMTs. This connection is very helpful, particularly as gate-lengths approach the sub-100 nm range. As it is also shown in Fig. 1, the parasitic delay times e.g., in barrier, semiconductor cap, and ohmic contact gain relatively more importance [13].

### III. NUMERICAL CALCULATIONS AND MINIMOS-NT

The Poisson equation and moments of the Boltzmann equations are solved using the two-dimensional (2-D) device simulator MINIMOS-NT, as described in previous publications e.g., [19]–[21]. The simulation area is split into several segments accounting for the different material properties, and the segments are connected by interface models. The following chapter briefly describes critical details relevant to the investigations which follow.

#### A. General Modeling

Sophisticated models are used to calculate the energy band structure, effective carrier masses, carrier densities of states, car-

rier mobilities, and energy relaxation times depending on lattice and carrier temperatures, and the material composition [21], [22]. We use material composition dependent models for the ternary semiconductors  $\text{In}_x\text{Ga}_{1-x}\text{As}$  and  $\text{Al}_y\text{Ga}_{1-y}\text{As}$  [22] that calculate the values from the corresponding binary semiconductors GaAs, InAs, and AlAs. This allows efficient simulation of complicated material structures. For aligning the band energies of the III/V materials we assumed a 60 : 40 distribution of the offsets valence band: conduction band. The model proves that it is possible for industrial standard devices to precisely model different transistors not only within one technology [19], but to use just one set of parameters for different technologies. Only geometry, doping, ohmic contacting, and parameters such as effective Schottky barrier heights are varied, that are confirmed by independent measurements.

#### B. Modeling the Overshoot and the Real Space Transfer within the Hydrodynamic Model

Velocity overshoot modeling is performed using the concept of the carrier temperature  $T_n$  dependent energy relaxation times  $\tau_w$  in the hydrodynamic model as outlined in [23]. The model of the channel interfaces is of particular importance for HEMTs, but also for other devices with heterojunctions. The interface conditions are then given by the following equations which denote the extension of a model reported previously [21]. The carrier current density  $J_{ni}$  and the energy flux density  $S_{ni}$  through a heterojunction interface are modeled as follows:

$$S_{n2} + 2 \left( k_B T_{n2} v_{n2}(T_{n2}) n_2 - \frac{m_2^*}{m_1^*} k_B T_{n1} v_{n1}(T_{n1}) n_1 \cdot \exp \left( -\frac{\Delta E_C - \partial E_C}{k_B T_{n1}} \right) \right) = 0 \quad (1)$$

$$S_{n2} = S_{n1} + \frac{1}{q} (\Delta E_C - \partial E_C) J_{n2} \quad (2)$$

$$J_{n2} - J_{n1} = 0, \quad (3)$$

$$J_{n2} - \alpha_n q \left( v_{n2}(T_{n2}) n_2 - \frac{m_2^*}{m_1^*} v_{n1}(T_{n1}) n_1 \cdot \exp \left( -\frac{\Delta E_C - \partial E_C}{k_B \cdot T_{n1}} \right) \right) = 0 \quad (4)$$

$$v_{n1,2}(T_{n1,2}) = \sqrt{\frac{2k_B T_{n1,2}}{\pi m_{n1,2}^*}} \quad (5)$$

where

$\Delta E_C$	conduction band offset;
$\partial E_C$	the barrier reduction depending on the electric field $E$ at the interface to account for the field supported tunneling effect of hot carriers at the interface;
$T_{ni}$	electron temperature in segment $i$ ;
$k_B$	Boltzmann constant;
$q$	carrier charge;
$m_i^*$	effective mass in segment $i$ ;
$x_{tun}$	electron tunneling length;

TABLE I  
SIMULATION PARAMETERS FOR THE INTERFACE MODEL

Material	$x_{tun}$	$\alpha_n$
n-In <sub>0.25</sub> Ga <sub>0.75</sub> As/	7 nm	1
p-Al <sub>0.2</sub> Ga <sub>0.8</sub> As		
Al <sub>0.20</sub> Ga <sub>0.8</sub> As/GaAs	3 nm	1

$E_{orth}$ : electric field orthogonal to the interface;

$\alpha_n$  conduction band edge form factor;

$v_{ni}$ : emission velocity.

$\alpha_n$  and  $\delta E_C$  are modeled with respect to the material system, the doping, and especially the  $\delta$ -doping near the interface. In this classical concept to describe a highly quantum mechanical situation the reduction  $\delta E_C$  is modeled by [24], [25] and references therein:

$$\delta E_C = \begin{cases} qE_{orth}x_{tun} & E_{orth} > 0 \\ 0 & E_{orth} \leq 0 \end{cases} \quad (6)$$

Starting from the Wentzel–Kramers–Brillouin approximation  $\alpha_n$  is a general, material dependent function which basically accounts for the dependence of the tunneling probability on the band gap discontinuity [24]. From simulations of examples [25] the following set of parameters was found to be useful. The values obtained for  $x_{tun}$  are of the order of the distance of the interface to  $\delta$ -doping, which typically amounts to 5 nm. This reflects the fact that the conduction band edge in the  $\delta$ -doped HEMT has its minimum in the  $\delta$ -doping plane.

The values given in Table I are used to model the interfaces in the AlGaAs/InGaAs/GaAs material system. Other interfaces e.g., for the InGaAs/InAlAs material system, were also simulated successfully using this model with a different set of parameters, including  $\alpha_n \neq 1$ . We stress the strong interdependence of the interface model and the overshoot modeling, which was carefully controlled, see also [11]. The efficient implementation of the model (with respect to CPU time) into the hydrodynamic simulation is crucial for obtaining results for steady state and transient simulations. An average bias point can be evaluated within 40 iteration steps.

### C. Contacts

For gate-lengths of  $l_g = 150$  nm and below it is found that the discussion of electronic transport strongly depends on the effective conduction band edge at the ohmic contact-semiconductor interface as a result of the alloying process into the cap geometry. The two limiting cases of contacts, possible by using alloying processes are shown in Fig. 2. Both situations are consistent with scanning electron microscope (SEM) images of the two technologies investigated in this work. In Case I the ohmic contact alloys through the cap layer and the channel is in contact with the metal. In Case II, the ohmic metal does not alloy through the cap, i.e., the cap/barrier and barrier/channel interfaces are not modified. Whether additional doping is introduced next to the regular doping depends on the alloying process. The

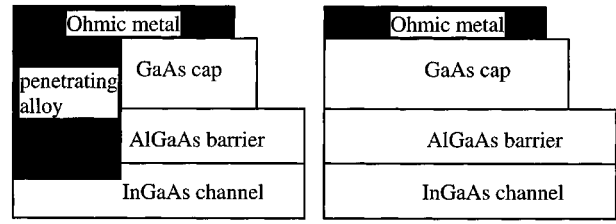


Fig. 2. Direct (Case I, left) and indirect (Case II, right) contacting of the channel by the ohmic contacts.

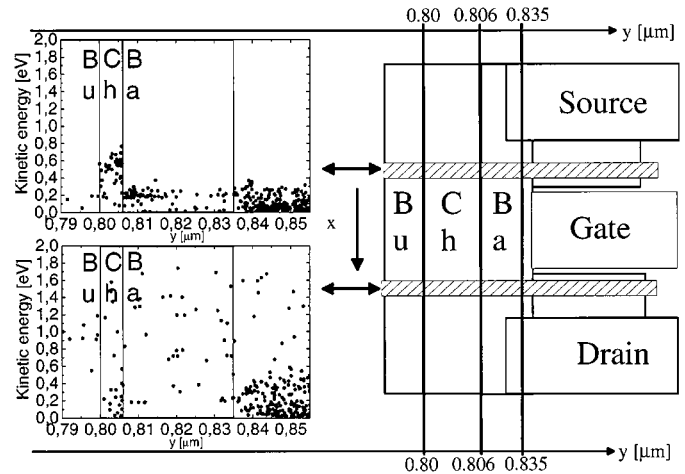


Fig. 3. Comparison of electron kinetic energy distributions on the source and drain for an Al<sub>0.25</sub>Ga<sub>0.75</sub>As/In<sub>0.3</sub>Ga<sub>0.7</sub>As HEMT of  $l_g = 250$  nm.

field distribution is strongly influenced by the ohmic contact situation: In Case I, the channel is directly contacted and RST represents a loss of carriers into the barrier and buffer only. The modeling of Case I is performed by extending the contact down to the channel. In Case II RST occurs under the gate and is the only means of current transport from the channel to the drain contact.

### D. Semiconductor Insulator Interfaces

Given barrier layers with thicknesses of 15 nm and below the occurrence of real space transfer leads to current transport close to the semiconductors–insulator interface especially near the drain. Thus, special attention was paid to that interface. To account for the strong pinning of the Fermi level between the barrier material Al<sub>x</sub>Ga<sub>1-x</sub>As and the SiN passivation [26] we used a Shockley–Read–Hall (SRH) recombination model. An inhomogeneous distribution of the trap number  $N_T$  to model the Fermi level pinning at midgap of 0.84 eV above the AlGaAs valence band-edge in the vicinity of the interface was assumed. In addition negative interface charges were applied. This model is also used to account for bulk traps in the Al<sub>x</sub>Ga<sub>1-x</sub>As layers. Since the Al concentration was kept below 22%, the DX centers in the bulk have only limited importance for device behavior.

### E. Monte Carlo Simulations

Fig. 3 shows simulation results obtained by the Monte Carlo simulator DAMOCLES for an Al<sub>0.25</sub>Ga<sub>0.75</sub>As/In<sub>0.3</sub>Ga<sub>0.7</sub>As/GaAs HEMT of a gate-length  $l_g = 250$  nm. On the right side of Fig. 3 the geometric structure of the HEMT

with a 6 nm wide  $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$  channel (Ch) between an  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$  barrier (Ba), and a GaAs buffer (Bu) can be seen. The ohmic contact is assumed to be a mixture of the two cases shown in Fig. 2. The GaAs cap-AlGaAs barrier interface is assumed to be alloyed through by the contact metal, whereas the AlGaAs/InGaAs interface remains intact. At the metal-semiconductor interfaces a doping of  $10^{19} \text{ cm}^{-3}$  is assumed. Applied bias was  $V_{DS} = 2 \text{ V}$  and  $V_{GS} = 0 \text{ V}$ . The two figures on the left show the kinetic energies of electrons as a function the relative y-position, the meaning of which can be seen also on the right. The energy distributions were obtained within two observation boxes visualized on the right with an x-extension of 30 nm symmetrically placed to the gate contact. The observation boxes were positioned at a distance of 30 nm from the gate edges, respectively. Thus, at the drain side of the gate the electrons pass the complete gate and another 30 nm of the high field zone, until they enter the observation box. The spacing of source to gate and gate to drain contact was 250 nm. On the source side the electrons enter the channel via the barrier gaining kinetic energy. On the drain side the figure demonstrates the dynamic equilibrium of electrons leaving the channel by real space transfer. Hot electrons are observed in the channel at the drain side of the gate, where they can undergo either KST in the channel, or undergo RST mostly into the gate-side barrier losing kinetic energy, followed by KST in the barrier. This shows, as described e.g., in [27], the critical function of the heterointerfaces, since they define the balance of RST and KST, and thus the mean carrier velocity.

#### IV. RESULTS FOR DC AND RF PARAMETERS AND DISCUSSION

To characterize device performance we supply a complete set of relevant dc and rf parameters as well as their bias dependence. In the following we present these parameters obtained by simulation and measurement for two pseudomorphic HEMT technologies and we discuss the relation to nonlinear transport. Technology A is based on e-beam lithography, whereas Technology B is based on an optical stepper lithography with SiN sidewall spacers. Gate-lengths of 150 nm are evaluated, both technologies represent industrially relevant standards. The ohmic contact situation of Technology A is approximated by Case I in Fig. 2, whereas Case II is applied for Technology B.

##### A. DC Results

Fig. 4(a) shows sets of simulated and measured output curves obtained for a HEMT with  $l_g = 150 \text{ nm}$  and  $2 \times 60 \mu\text{m}$  gate-width of Technology A. Fig. 4(b) shows sets of simulated and measured output curves obtained for a HEMT with  $l_g = 140 \text{ nm}$  and  $4 \times 40 \mu\text{m}$  gate-width of Technology B. The dc capabilities of the simulator including self-heating using a substrate thermal contact at  $T_L = 300\text{K}$  are demonstrated. Special care was taken to obtain realistic thermal boundary conditions. The overall good agreement for both technologies with sets of experiments is a prerequisite for the appropriate prediction of the complete device behavior. The high  $g_m$  and the high drain current density up to 900 mA/mm is characteristic for HEMTs as can be seen in Fig. 4(a). Fig. 4(b) reveals equally good agreement. Note, the negative output conductance that can be observed in the simulations.

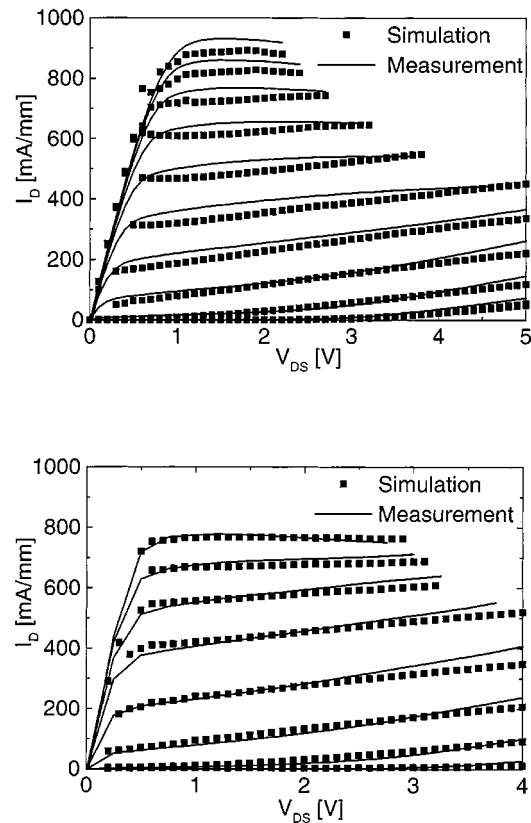


Fig. 4. Top: Output characteristics of a  $l_g = 150 \text{ nm}$   $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}/\text{In}_{0.25}\text{Ga}_{0.75}\text{As}/\text{GaAs}$  HEMT of Technology A.  $V_{GS} = -0.8 \dots 1.0 \text{ V}$ , stepping 0.2 V. Bottom: Output characteristics of a  $l_g = 140 \text{ nm}$   $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}/\text{In}_{0.25}\text{Ga}_{0.75}\text{As}/\text{GaAs}$  HEMT of Technology B.  $V_{GS} = -0.4 \dots 1.0 \text{ V}$ , stepping 0.2 V.

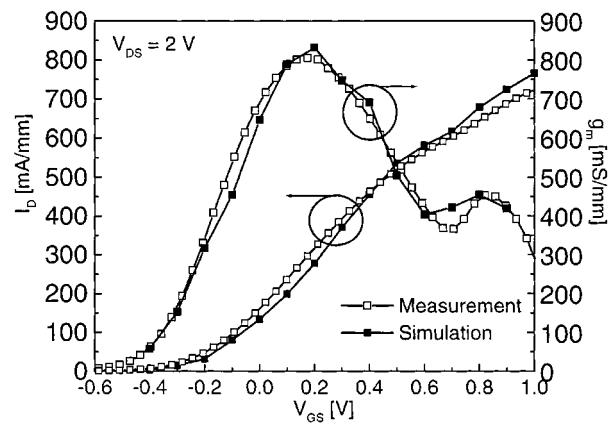


Fig. 5. Transfer characteristics and dc-transconductance at  $V_{DS} = 1.5 \text{ V}$  for Technology B at  $l_g = 140 \text{ nm}$ .

served in the simulations. Fig. 5 shows both simulated and measured transfer characteristics of a  $2 \times 40 \mu\text{m}$  HEMT of Technology B corresponding to Fig. 4(b). In the  $g_m$  curve the effect of RST can best be observed for  $V_{GS} \geq 0.2 \text{ V}$ . The current spreads into the barrier with increasing  $V_{GS}$  at given  $V_{DS}$  due to RST. This effect widens the  $g_m$  curve toward higher  $V_{GS}$  values, whereas the value for  $g_m$  is reduced. The observation of the second peak is found to be lattice temperature dependent. As a simplified explanation we suggest the decreasing of the channel depth, which smoothes the transition between the two peaks as

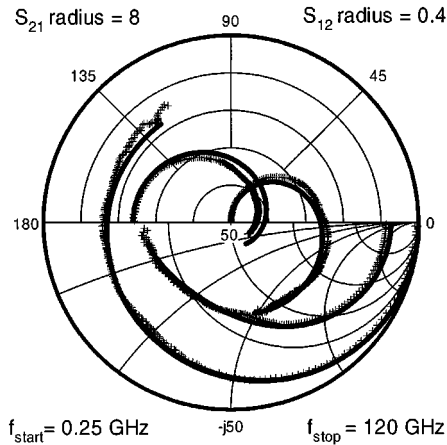


Fig. 6. Simulated (lines) and measured (+)  $S$ -parameters between 0.25 GHz and 120 GHz for gate-length  $l_g = 140$  nm at  $V_{DS} = 1.5$  V and  $V_{GS} - V_{th} = 0.4$  V.

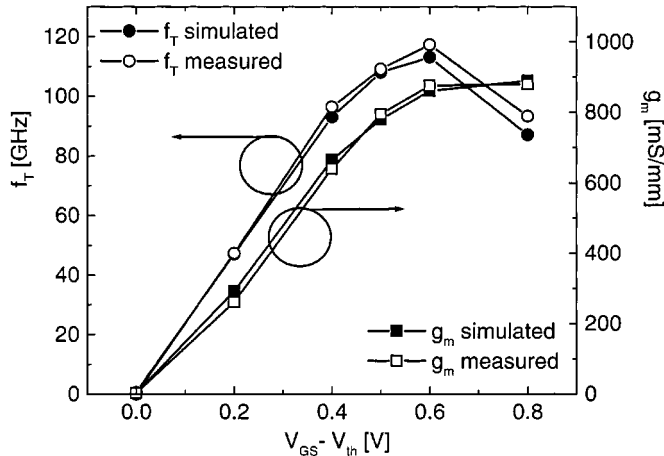


Fig. 7. Simulated and measured  $f_T$  and the rf- $g_m$  as a function of  $V_{GS}$  bias at  $V_{DS} = 1.5$  V for a device of  $l_g = 140$  nm.

a function of rising lattice temperature. Further, the observation of the second peak depends on the position of the maximum  $g_m$  relative to the opening gate diode, in this case at  $V_{GS} = 0.65$  V. If  $g_{m \max}$  occurs at  $V_{GS}$  too close the opening gate diode, the two effects cannot be separated. Thus, the interplay of RST and KST for a given carrier concentration determines  $g_m$  and the saturation current  $I_{Dsat}$ . The particular advantage of HEMT's to be high gain devices is illustrated by the maximum dc- $g_m$  in Figs. 4 and 5, respectively.

### B. RF Results

The bias dependence of the small-signal equivalent circuit elements was simulated which gives a complete description of the device small-signal performance for the bias range under investigation. The corresponding  $S$ -parameters can be simulated with MINIMOS-NT using a small-signal excitation at 5 GHz [28]. The simulated  $S$ -parameter results of a  $2 \times 30 \mu\text{m}$  HEMT are shown in Fig. 6 in comparison to measurements. Using an 8-element small-signal equivalent circuit topology small-signal equivalent elements are calculated. For the extrinsic comparison to measured  $S$ -parameters we use the same (typical) parasitic elements as extracted from the measured  $S$ -parameters. Thus,

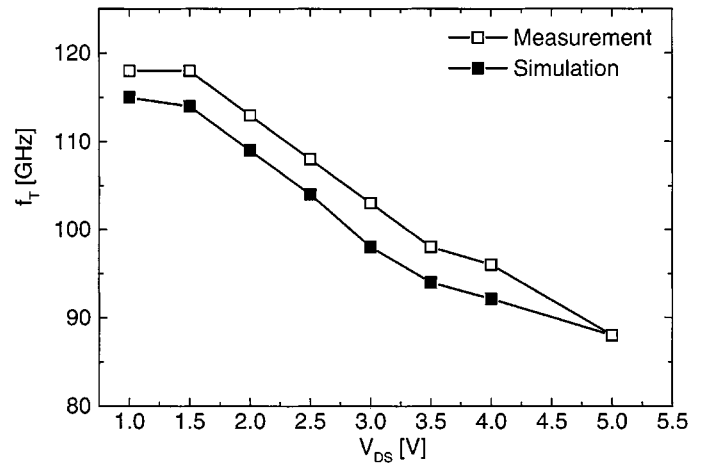


Fig. 8. Current gain cutoff frequency  $f_T$  as a function of  $V_{DS}$  bias for  $V_{GS}$  at  $g_{m \max}$  for  $l_g = 140$  nm.

using an 8-element circuit no free parameters are used in this comparison. Accordingly, Fig. 6 shows very good agreement, which serves as a basis for further discussions. Fig. 7 shows the simulated and measured  $V_{GS}$  bias dependence of the extrinsic current-gain cut-off frequency  $f_T$  and the extrinsic rf- $g_m$ . The agreement of the simulations and the values extracted from  $S$ -parameter measurements is good. The most crucial difference of the HEMT to e.g., MESFETs for circuit design is the rf-gain [20], which provides a crucial advantage for the HEMT.

In terms of small-signal equivalent circuit elements this is expressed essentially by the extrinsic  $g_m$  for a given gate-length. This results in a higher  $f_{\max}$ , in higher maximum stable gain MSG, and maximum available gain MAG. The latter can be easily seen by the representation of MAG/MSG as a function of small-signal equivalent circuit elements [29] and is a crucial advantage for the use of HEMT's e.g., in medium power amplifiers (MPA) in the W-band.

Fig. 8 shows the decay of the current gain cut-off frequency  $f_T$  with  $V_{DS}$  (both simulation and measurement) for a HEMT with  $l_g = 140$  nm. For chip design in general, the dependence of  $f_T$  on bias represents one key to optimize devices with respect to small-signal use. However, e.g., for power amplifier design, especially above 20 GHz, the use of devices is restricted both by the gain, represented by  $g_m$  and by the output power available as a function of bias at the frequency of operation. To assess factors that determine the decay of  $f_T$  for moderate  $V_{DS}$  assuming no breakdown limitation we have plotted in Fig. 9 the experimentally found dependence of the decay  $f_T/V_{DS}$  on gate-length. This was done for a variant of Technology A which was experimentally available for several gate-lengths. The nonlinear increase of the decay  $f_T/V_{DS}$  for small gate-lengths proves the influence of short channel effects and explains the advantage of a higher  $f_T \times l_g$  product for small-signal use, which allows the high indium channel HEMT to realize the same  $f_T$  at a comparably higher gate-length, e.g., relative to the GaAs MESFET.

### C. RF Results and Electronic Transport

To explain the bias dependence of the equivalent circuit elements the calculated and measured  $C_{gs}$ ,  $C_{gd}$ , and rf- $g_m$  are presented. From the point of view of electronic transport RST is a

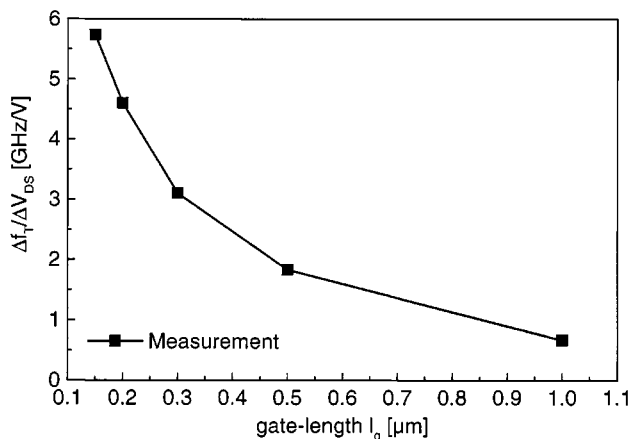


Fig. 9. Experimental dependence of the  $f_T/V_{DS}$  decay as a function of gate-length  $l_g$ .

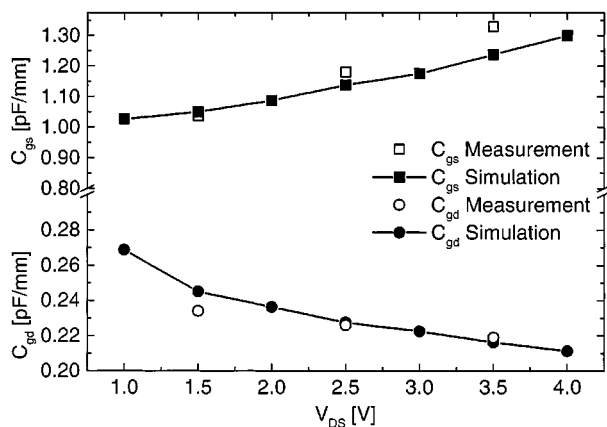


Fig. 10.  $C_{gs}$  and  $C_{gd}$  as a function of  $V_{DS}$  bias at  $g_{m,max}$  for  $l_g = 140$  nm.

key to understand these bias dependencies: With increasing  $V_{DS}$  the electrons undergo RST out of the channel and populate the barrier, where they experience much lower carrier mobility and saturation velocity. This is true both for pure dc operation and for rf operation, when the term modulation efficiency is more appropriate.

Fig. 10 shows the simulated and measured  $C_{gs}$  and  $C_{gd}$  as a function of  $V_{DS}$ . To illustrate the contributions to  $C_{gd}$ , the capacitance can be separated in the following terms [30]:

$$C_{gd}(V_{DS}) = C_{gd\text{ metallization}} + C_{gd\text{ passivation}} + C_{gd\text{ device}}(V_{DS}). \quad (7)$$

The first two contributions in (7) arise from the electric coupling of the gate and drain contact metallization and from the electric coupling of the gate-contact to the drain-contact cap. Both are bias independent in a first order approach. The bias dependence of  $C_{gd}$  on  $V_{DS}$  is caused by the increase of the size of the space charge zone. This expands with rising  $V_{DS}$  bias, so that the capacitance  $C_{gd}$  is reduced, as shown in Fig. 10, both by simulation and measurement results. Two factors define the extension of the space charge zone. On the one hand a vertically structured, non depleted semiconductor, e.g., an  $n^{++}$  doped cap, stops the extension of the depletion zone, and thus the decrease of the capacitance  $C_{gd}$ . On the other hand the shape of the space charge

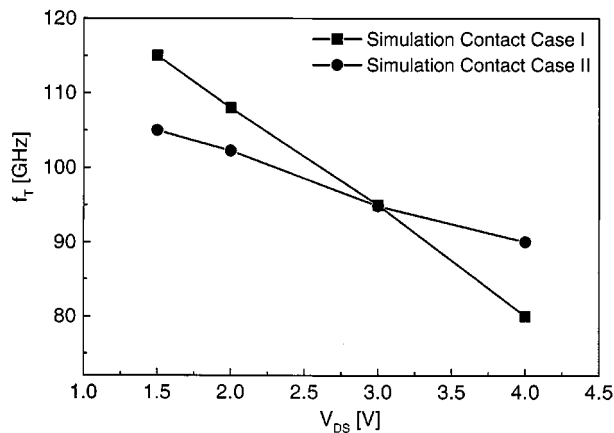


Fig. 11.  $f_T$  as a function of  $V_{DS}$  for the two contact cases at  $l_g = 140$  nm at  $V_{GS}$  for  $g_{m,max}$ .

zone is strongly influenced both by the effective drain contacts and by the SiN/AlGaAs interface. The surface states lead to an additional depletion of the vicinity of the SiN/AlGaAs interface due to the Fermi-level pinning.

$C_{gs}$  is located between the channel carrier density and the gate contact. The correlation of the RST and the bias dependence of  $g_m$ ,  $C_{gs}$  and  $C_{gd}$  is given by the electrons leaving the high field region out of the channel. In [31] experimental evidence is given suggesting that the ultimate performance limits of HEMTs arise from a combination of real space transfer into the AlGaAs, followed by k-space transfer within the AlGaAs. Thereby the mean carrier velocity is significantly reduced. The argumentation in [31] is mostly focused on the  $V_{GS}$  dependence at given  $V_{DS}$ . The increase in  $C_{gs}$  with  $V_{DS}$  can be understood as follows: the gate-foot and the current density in the channel form a capacitance with the channel charge as a movable capacitor plate. If any charge density (as a function of bias) moves closer toward the gate, the capacitance  $C_{gs}$  will increase. With rising  $V_{DS}$  the probability for RST generally increases for any given band gap discontinuity, so  $C_{gs}$  increases at a given  $V_{GS}$ , because the center of the channel side carrier charge moves closer to the gate. This mechanism can be seen as a dc equivalent of what was explained within the charge control models with the term modulation efficiency. Furthermore, the loss of carriers out of the channel by RST will cause the  $g_m$  to drop, since  $g_m$  is proportional to the effective mean carrier velocity. The latter will decrease if an increasing amount of carriers leaves the channel. At the same time  $C_{gs}$  rises with increasing  $V_{DS}$ , generally overcompensating the decay of  $C_{gd}$ , which explains the  $f_T$  decay with rising  $V_{DS}$ .

The gate-length dependence of the decreasing  $f_T/V_{DS}$  shown in Fig. 9 can also be explained with the scaling of the feature sizes already shown in Fig. 1: The fields in the high field region increase more than linearly with decreasing gate-length since applied bias are normally not scaled linearly. This results in an increased probability for RST.

Fig. 11 shows two simulations for a HEMT device to deliver proof of our explanation: the simulation is performed for two absolutely comparable devices, the only difference is the ohmic contact situation, and with it the transport through the interfaces. Both situations demonstrated their importance for industrially

relevant devices in Technology A and B, respectively. Fig. 11 compares the decay of  $f_T$  with rising  $V_{DS}$  at  $V_{GS}$  for maximum  $g_m$  for the two contact situations shown in Fig. 2. In Case II, for the indirect contacting, where RST is the only means of current transport from channel to drain, the maximum value of  $f_T$  is lower, but at the same time the decay with  $V_{DS}$  is smaller compared to Case I. In Case I, for the direct contacting of the channel, RST increases with rising  $V_{DS}$  bias, which results in a higher  $f_T$  for low  $V_{DS}$  bias, but results in a stronger decay, which even leads to the crossing of the curves. This demonstrates that for a device optimized for maximum  $f_T$  at low  $V_{DS}$  bias (Case I), the performance limiting factor is RST. These simulation results confirm a general experience during HEMT optimization on various structures. The simulations further allow to separate the transport effects from superimposed technological variations. The direct consequences for the small-signal parameters support the idea that RST, from the perspective of carrier transport, is a determining factor for the HEMT device performance and must under no circumstances be neglected when assessing the fundamental limits of HEMT devices.

#### V. SUMMARY

By simulations the interplay of nonlinear transport effects and rf/dc performance in HEMTs has been demonstrated. These simulations show the function of the hetero-barrier to define an equilibrium of real space transfer and k-space transfer. Real space transfer explains the importance of carrier confinement for HEMT device performance at high  $V_{DS}$  bias. Fully optimized devices must be used to evaluate HEMT performance and a complete set of circuit relevant criteria needs to be included, such as maximum drain current  $I_{D\max}$ , transconductance  $g_m$ , capacitances, and the bias dependence of the transit frequency  $f_T$ . It was shown that real space transfer is a determining factor to understand the bias dependence of the small-signal equivalent circuit elements in a HEMT.

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