Proceedings of IPACK'01
The Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition
July 8-13, 2001, Kauai, Hawaii, USA

IPACK2001-15601

THREE-DIMENSIONAL ELECTRO-THERMAL SIMULATION OF INTERCONNECT STRUCTURES WITH TEMPERATURE-DEPENDENT PERMITTIVITY

Christian Harlander, Rainer Sabelka, and Siegfried Selberherr
Institute for Microelectronics
Technische Universität Wien
Gusshausstrasse 27-29 / E360
A-1040 Wien, AUSTRIA / Europe
Email : Harlander@iue.tuwien.ac.at

ABSTRACT

We present an extraction tool that computes parasitic interconnect parameters with temperature-dependent dielectrics. A stationary electro-thermal analysis is performed, followed by the capacitance extraction, taking the permittivity as function of the temperature distribution into account. The tool is based on the finite element method for two- and three-dimensional analyses of interconnect structures. The simulation package includes a layout file converter as well as a geometry processing and a mesh generation engine, thus allowing a fully automatic layout to capacitance extraction. Our approach has been designed for highly accurate capacitance calculation in modestly large simulation domains, but not for full chip extraction. The main module computes the resistances, capacitances and inductances of the interconnect structures, the distribution of the electric potential, the temperature, and the current density.

INTRODUCTION

Recently, low-k materials gain importance as interline dielectrics. For some of these materials (e.g. fluorinated amorphous carbon (Fujii et al., 1998)) the permittivity depends significantly on the temperature, and beyond the thermal conductivity is lower than the oxide's one, hence thermal simulations are of increasing importance.

State of the art capacitance extraction tools can only analyze structures with constant permittivity. Our program package supports a model for temperature-dependent permittivity and can be applied for optimization of interconnect structures as well as for studies to verify the reliability of interconnects.

MATHEMATICAL BACKGROUND

For the numerical calculation of Joule self-heating effects two partial differential equations have to be solved.

$$\operatorname{div}(\gamma_E \operatorname{grad}\varphi) = 0 \tag{1}$$

gives the electric potential φ and needs to be solved only inside domains of conductive material. γ_E denotes the electric conductivity. Then the power loss density p is obtained by computing

$$p = \gamma_E (\operatorname{grad}\varphi)^2 . \tag{2}$$

The heat conduction equation is solved to obtain the temperature distribution

$$\operatorname{div}(\gamma_T \operatorname{grad} T) = -p . \tag{3}$$

γ_T represents the thermal conductivity. The temperature dependence of the conductivities is modeled by

$$\gamma(T) = \frac{\gamma_0}{1+\alpha(T-T_0)}, \tag{4}$$

where γ_0 is the thermal or electrical conductivity at the reference temperature 300 K and α is the temperature coefficient of the specified material.

After the numerical calculation of the Joule self-heating the capacitance extraction is tackled. The solution of the Laplace equation inside the insulator domain gives the potential φ:

$$\mathrm{div}(\underline{\varepsilon}(T;x,y,z)\mathrm{grad}\varphi) = 0, \tag{5}$$

$\underline{\varepsilon}$ denotes the permittivity tensor, whereby dependence on the temperature is modeled as in (4). Conductor surfaces are represented by Dirichlet boundary conditions. For n conductors $n-1$ simulations with different voltages on each conductor are performed. The energy of the electric field is derived from the calculated potential distribution for each simulation run and the partial capacitances are calculated thereof.

THE PROGRAM PACKAGE

The SMART ANALYSIS PROGRAMS (Sabelka and Selberherr, 2001) uses the finite element method to solve above equations. Thereto, the program package includes preprocessors for geometry modeling and generating the grid. The program CUTGRID is used for two-dimensional applications and LAYGRID for three-dimensional applications. The latter allows a layer-based input of the simulation geometry and the specification of the boundary conditions on the borders of each simulation subdomain. Furthermore, the gridder DELINK (Fleischmann et al., 1999) is used to provide a fully unstructured grid.

APPLICATION EXAMPLE

Figure 1 shows the temperature distribution as contour surfaces representation of a Tungsten-via and a neighboring line in dual-damascene technique. In spite of the high resistance at the bottom of the W-plug (high heat generation rate) a large area of the tungsten-via is exposed to elevated temperature. This is because the thermal conductivity of the simulated dielectrics (fluorocarbon plasma C_2F_6 (Fujii et al., 1998)) is much less than the thermal conductivity of classical dielectrics such as SiO_2.

In Table 1 is a confrontation of the partial capacitances with and without consideration of the temperature-dependent permittivity of the low-k material and the resulting error for neglecting the temperature-dependent permittivity of the low-k material.

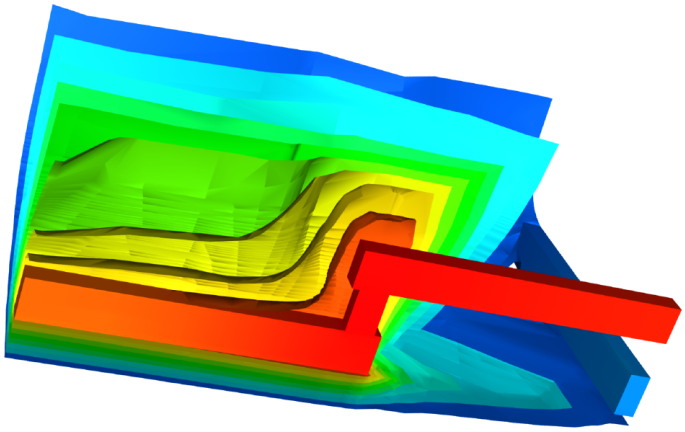

Figure 1. TEMPERATURE DISTRIBUTION WITH THE MAXIMUM TEMPERATURE OF 99°C AT THE BOTTOM OF THE TUNGSTEN PLUG.

Table 1. PARTIAL CAPACITANCES:

	C_{ij} [F]	$C_{ij}(T)$ [F]	Error [%]
Ground plane-Via	4.19e-16	3.98e-16	5.27
Ground plane-Line	6.83e-16	6.52e-16	4.75
Via-Line	7.21e-17	6.49e-17	11.09

CONCLUSION

We have presented an advanced method for computing parasitic interconnect parameters with temperature-dependent dielectrics. Thus the program package SMART ANALYSIS PROGRAMS offers highly accurate analysis of VLSI circuits with temperature-dependent low-k materials.

ACKNOWLEDGMENT

Our work is partly supported by Sony Corporation, Atsugi, Japan.

REFERENCES

Fleischmann, P., Pyka, W., and Selberherr, S. (1999). Mesh generation for application in technology CAD. *IEICE Trans.Electron.*, E82-C(6):937–947.

Fujii, T., Hiramatsu, M., and Nawata, M. (1998). Characteristics of low-k interlayer dielectric films prepared by fluocarbon plasma cvd with hexamethyldisiloxane. In *VMIC Conference*, pages 541–546.

Sabelka, R. and Selberherr, S. (2001). A finite element simulator for three-dimensional analysis of interconnect structures. *Microelectronics Journal*, 32(2):163–171.