

EFFECTIVENESS OF SILICON NITRIDE PASSIVATION IN III-V BASED HETEROJUNCTION BIPOLAR TRANSISTORS

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(Received 7 April 2000)

The quality of Si₃N₄ thin film passivation is of importance for the reliability of III-V based Heterojunction Bipolar Transistors (HBTs). Both theoretical and experimental studies have been conducted in order to minimize base leakage currents as a major source of degradation. In the present work we investigate the effectiveness of the passivation of devices before and after electrothermal stress aging by the means of two-dimensional numerical simulations. For that purpose proper electrical and thermal models were implemented in our simulator MINIMOS-NT allowing simulation of silicon nitride as a wide bandgap semiconductor material.

Keywords: Nitride passivation; Heterojunction bipolar transistors; Two-dimensional simulation; Device reliability; Thermoelectrical stress aging

1. INTRODUCTION

Our two-dimensional device simulator MINIMOS-NT deals with different complex materials and structures, such as binary and ternary III-V alloys with arbitrary material composition profiles. Various important physical effects, such as band gap narrowing, surface recombination, and self heat-

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ing, are taken into account. The model's efficiency was proven by hydrodynamic DC-simulations with self-heating of forward, reverse, and output HBT characteristics [1]. Simulation results are in very good agreement with measured data.

2. ROLE OF THE INGAP LEDGE

It is well known that GaAs-HBTs with an InGaP ledge lead to improved reliability if the emitter material remains over the complete p-doped base layer [2] forming the so-called ledge. For devices with ledge thickness of less than 20 nm the ledge is almost depleted by the base-emitter space charge region; therefore, such devices are of quite good quality and are not the subject of this work.

Degradation Mechanisms in Devices with No Ledge

In the case of devices where no ledge is present (see Fig. 1) the simulation results suppose that during stress some of the electrons flowing in the emitter are injected in to the insulator and are trapped. The negative charge at the semiconductor/insulator interface can lead to a hole leakage path in the vicinity of the interface, and therefore, to undesirably high base currents.

Influence of the Ledge Thickness and the Interface Charge Density

Furthermore, we investigated devices of InGaP/GaAs HBTs with different ledge thicknesses when no surface charges are present. The simulation results show a strong increase in the base current at low bias with increasing ledge thickness. The reason is that insulator surface Fermi-level pinning does not take place and therefore, an electron current path occurs in the upper part of the ledge. We found that the upper part of the ledge is also depleted through the influence of fixed negative surface charges which are homogeneously distributed along the interface between ledge and passivation. We found a value of 10^{12} cm^{-2} to be sufficient to obtain good agreement with the measured data.

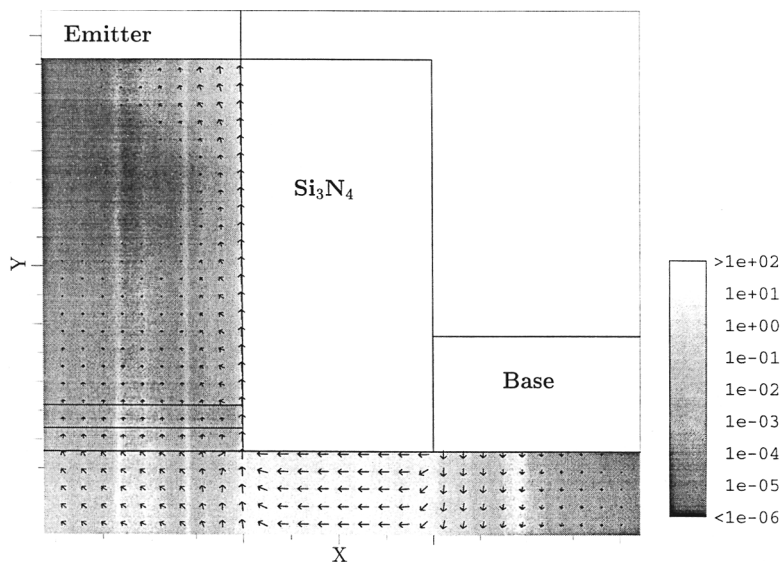


FIGURE 1 Hole current density [A/cm²]. Leakage path near the Si₃N₄ interface in the presence of negative charges.

3. SILICON NITRIDE AS A WIDE BANDGAP SEMICONDUCTOR

We account for the non-ideal properties of the passivation by considering it as a semiconductor material. A bandgap of 5 eV, relative dielectric constant of 7, and constant carrier mobilities based on a resistivity of 10^{16} Ω -cm are used. Thus, previous results assuming an ideal insulator material are verified. However, it has to be noted that the transport properties in the insulator strongly depend on the band gap alignment on the insulator/semiconductor interface which can be altered in the presence of surface charges. The impact of the surface charge density is illustrated in Figure 2 where simulation results for the electron current density at $V_{BE} = 1.2$ V without and with a surface charge density of 10^{12} cm⁻², respectively, are shown. Shockley–Read–Hall recombination is taken into account also in the SiN with a trap density of 10^8 cm⁻³. Note, the decrease in the electron current density also in the insulator in the presence of negative charges.

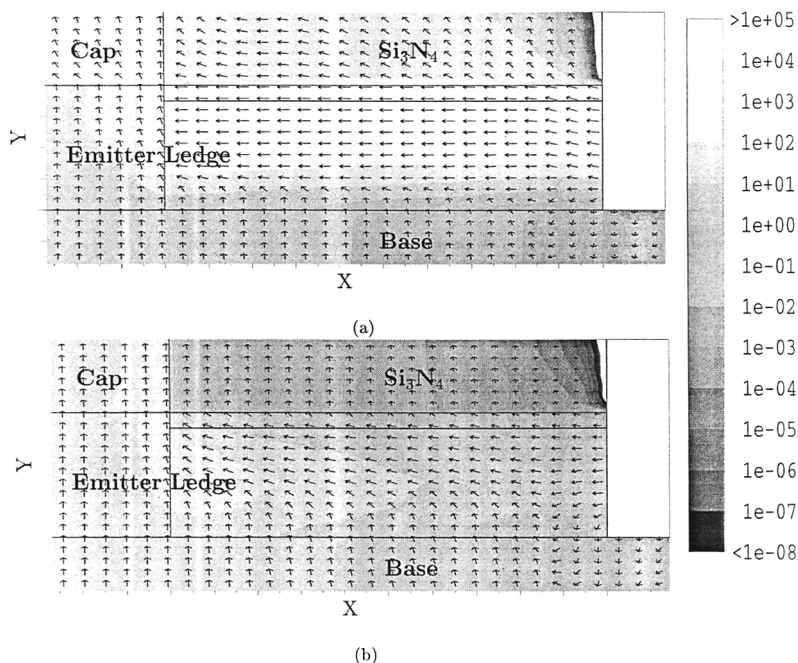


FIGURE 2 Electron current density [A/cm²] at $V_{BE} = 1.2$ V. Simulation without surface charges (a) and with 10^{12} cm⁻² (b).

4. DEVICE RELIABILITY

Based on these investigations it is possible to explain the base current degradation of an InGaP/GaAs HBT which was strongly stressed under conditions far from normal operating conditions. In this case the base current degradation in the middle voltage range can be explained by a decreasing surface charge density along the interface between ledge and passivation from 10^{12} cm⁻² to $4 \cdot 10^{11}$ cm⁻². This might be due to compensation of the negative surface charges by H⁺ ions which are known to be present in the device due to the epitaxial manufacturing processes [3, 4]. In Figure 3 a comparison of measured and simulated forward Gummel plots at $V_{CB} = 0$ V is shown. Filled and open symbols denote measured characteristics of the non-degraded and degraded device, respectively. The corresponding simulation results are shown with lines. The good agreement

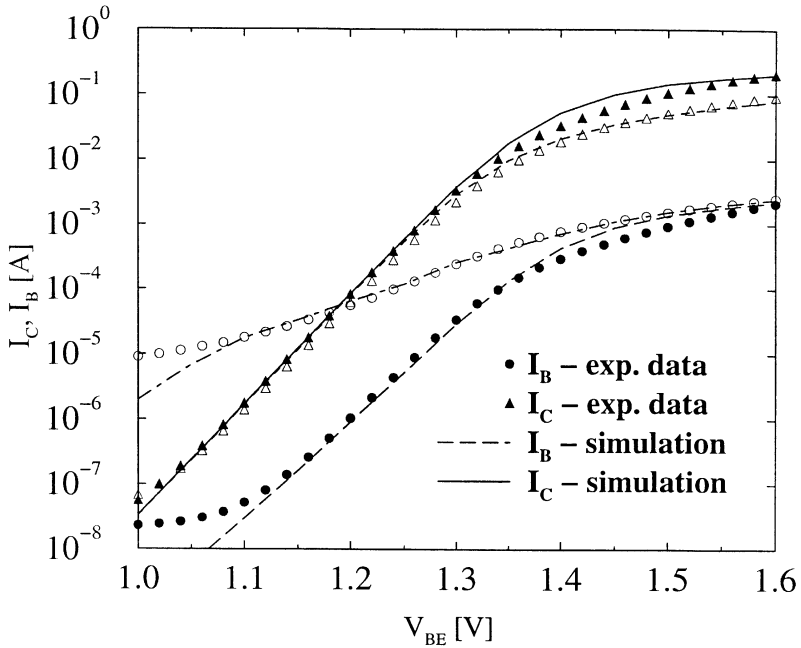


FIGURE 3 Forward Gummel plots at $V_{CB} = 0$ V. Comparison between simulation and measurements before and after electrothermal stress.

also for stressed devices demonstrates the applicability of physics-based device simulation to device reliability issues.

Acknowledgment

The authors acknowledge Dr. W. Kellner for supporting this work.

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