Reliable Prediction of Deep Sub-Quartermicron CMOS Technology Performance

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Abstract

We present a novel methodology for characterization of sub-quartermicron CMOS technologies. It involves process calibration, device calibration employing two-dimensional device simulation and automated Technology Computer Aided Design (TCAD) optimization, and, finally, transient mixed-mode device/circuit simulation. The proposed methodology was tested on 0.25 μm technology and applied to 0.13 μm technology in order to estimate ring oscillator speed. The simulation results show an excellent agreement with available experimental data.

1. Introduction

The manufacturing process with shrinking technology is becoming so complicated that using simulation in a predictive manner has been recognized as an integral part of any advanced technology development. In order to satisfy predictive capabilities the simulation tools must capture the process as well as device physics. Before going to final production runs one can optimize the process steps and estimate device performance characteristics such as threshold voltage, saturation current, leakage current, and circuit speed.
Several tools for simulation of semiconductor technology (e.g. [1, 2]) as well as semiconductor devices (e.g. [3]–[6]) are well established for device engineering applications. The two-dimensional device simulator MINIMOS-NT is equipped with an extensive mixed-mode circuit capability including modeling of distributed devices [7]. It works in an automated device optimization framework [8]. This allowed creation of a novel methodology for deep sub-micron technology characterization. In the following two sections the methodology is explained and the simulation results are presented.

2. Methodology

The technology characterization system implemented at LSI Logic has been successfully used for 0.25 μm and 0.18 μm technologies. This system included previous technology process and device calibration, creation of new technology extrapolation and optimization with TSUPREM4 [1] and MEDICI [3], respectively, sensitivity analysis and Monte Carlo statistical analysis, and, finally, gate delay estimation using a physical compact model in HSPICE [9]. For 0.13 μm technology, the HSPICE physical model failed to fit the I-V characteristics extracted by MEDICI and it was impossible to estimate the gate delay characteristic of that technology using the old methodology.
In our new approach the process calibration part was kept the same while device simulation was performed by MINIMOS-NT in the SIESTA optimization TCAD framework [8]. The same distributed devices are then employed in transient mixed-mode device/circuit simulation to predict circuit performance. The calibration procedure involved devices of gate lengths in the range from 0.2 μm to 1 μm for 0.25 μm technology and from 0.115 μm to 0.7 μm for 0.13 μm technology, while the circuit simulation was performed with the nominal devices.

2.1 Device Fabrication and Process Calibration

The process simulation starts from the blank wafer to the final device and reflects real device fabrication as accurately as possible. All implant profiles, e.g. LDD, V_t-adjust, source/drain pocket implants as well as annealing steps were calibrated to one-dimensional SIMS profiles. Process calibration is completed when the threshold voltage – gate length characteristic (V_t-L_g) matches experimental data which indicates that the simulation includes advanced device behavior such as the reverse short channel effect (RSCE). It is necessary to include the V_t-L_g characteristic into the process calibration loop because any change in process conditions would affect the electrical data (V_t) of the device. A Monte Carlo procedure was used for accurate simulation of the large angle low dose implants and TSUPREM4 was invoked for

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the thermal and topological steps. The threshold voltage simulation was performed by MEDICI. The gate length L_g, gate width W_g, optical gate oxide thickness T_{ox}, and applied voltage V_{dd} for the investigated technologies are summarized in Table 1.

Table 1: Key parameters for the technologies considered in this work

Technology	L_g	W_g	T_{ox}	V_{dd}
0.25 μm	0.2-1.0 μm	20 μm	4.7 nm	2.5 V
0.13 μm	0.115-0.7 μm	10 μm	2.3 nm	1.5 V

2.2 Device Calibration

We used the SIESTA TCAD framework to perform an automated device calibration operation without user interaction during the optimization process. Our optimization strategy is based on an iterative method where the performance metric is gradually improved using gradient information of the design parameters. The goal is to find a combination of physical parameters within a specified range that delivers the best performance metric.

The physical models in MINIMOS-NT are well calibrated [11], especially for silicon-based devices. There are only a few technology dependent model parameters that can be used for calibration purposes. One parameter is the gate workfunction difference E_w which depends on the interface charges at the Si/SiO_2 interface and the properties of the polysilicon gate. Other parameters are from the mobility models (1)-(2), which strongly depend on the quality of the Si/SiO_2 interface and electric field distribution in the channel. The high-field mobility models (2), must be used carefully, because their parameter values, e.g. the carrier saturation velocities at 300K, v_ν^{sat}, cannot generally be used as fitting parameters. The mobility models used are,

$$\mu_\nu^{\mathrm{LIS}} = \frac{\mu_\nu^{\mathrm{ref}} + (\mu_\nu^{\mathrm{LI}} - \mu_\nu^{\mathrm{ref}}) \cdot (1 - F(y))}{1 + F(y) \cdot \left(\frac{S_\nu}{S_\nu^{\mathrm{ref}}}\right)^{\gamma_\nu}}, \quad \nu = n, p \tag{1}$$

$$\mu_\nu^{\mathrm{LISF}} = \frac{2 \cdot \mu_\nu^{\mathrm{LIS}}}{1 + \left(1 + \left(\frac{2 \cdot \mu_\nu^{\mathrm{LIS}} \cdot F_\nu}{v_\nu^{sat}}\right)^{\beta_\nu}\right)^{1/\beta_\nu}}. \tag{2}$$

Here μ_ν^{LI} incorporates lattice mobility reduction due to ionized impurity scattering, μ_ν^{LIS} adds surface scattering, and μ_ν^{LISF} gives the final mobility including high-field reduction effects. $F(y)$ is a function giving the depth dependence, F_ν are the driving forces for carrier ν, and S_ν are the pressing forces equal to the magnitude

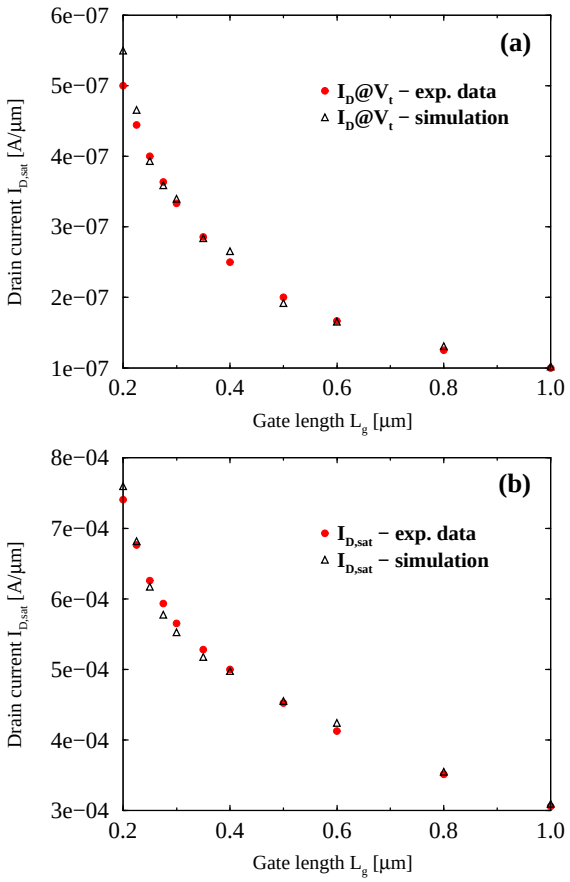

Figure 1: Calibration of the threshold voltage V_t (a) and the saturation current $I_{D,\mathrm{sat}}$ (b) for NMOS devices created with 0.25μm technology

of the normal field strength at the interface if the carriers are attracted by the interface, otherwise zero [11].

The physical parameters used in the optimization procedure and their final values are summarized in Table 2.

Table 2: Mobility model parameters for the 0.25 μm and 0.13 μm technologies

Parameter	0.25 μm NMOS	0.25 μm PMOS	0.13 μm NMOS	0.13 μm PMOS
E_w [eV]	-0.372	0.551	-0.433	0.407
μ_ν^{ref} [cm^2/Vs]	582	78	573	82
S_ν^{ref} [V/cm]	5.4e5	6.6e5	6.3e5	6.2e5
γ_ν	7.1	8.0	6.0	8.7
β_ν	1.18	1.06	1.1	1.1
v_ν^{sat} [cm/s]	9.8e6	9.8e6	1.2e7	1.18e7

After reading a given set of parameters for optimization, the simulations are performed by MINIMOS-NT to obtain $I_{D,\mathrm{sat}}$ (I_D @ V_{dd}) and $I_{D,t}$ (I_D @ V_t) for all devices

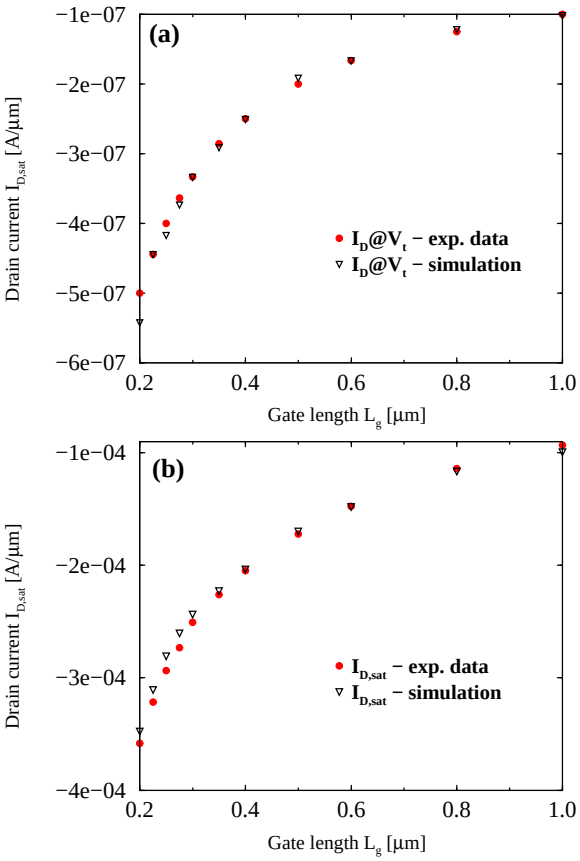

Figure 2: Calibration of the threshold voltage V_t (a) and the saturation current $I_{D,\mathrm{sat}}$ (b) for PMOS devices created with 0.25 μm technology

of different gate lengths (see Table 1). The results are then compared to experimental data. The saturation current is adjusted to the experimental one at applied voltages (V_d=V_g=V_{dd}), while the threshold voltage is fitted implicitly. Because threshold voltages V_t are measured at calculated current $I_{D,t} = (0.1 \cdot W_g/L_g)\ \mu$A, the optimizer adjusts the drain current to this value at applied V_d=V_{dd} and V_g=V_t. This approach turned out to be more effective in two aspects. The matrix solved for the device simulation are much better conditioned with voltage boundary condition. Additionally it gives comparatively small relative errors for the threshold voltage. We found errors of 10-15% in $I_{D,t}$ correspond to errors of less than 2% in V_t.

The SIESTA setup allows a simultaneous calibration, using the same model suite and set of model parameters, of I_D @ V_{dd} and I_D @ V_t to the measured values for several devices of different gate lengths with minimum global error [10].

The proposed methodology of device calibration was tested on 0.25 μm technology. 11 NMOS and 11 PMOS devices, respectively, were simulated at V_{dd} and V_t. The NMOS and PMOS device calibration is performed separately, because the model parameters are different. The parameter ranges are varied within 50% of the default values. In Fig. 1 the NMOS calibration results are presented. Fig. 1(a) actually shows threshold voltage calibration results by presenting the drain current at V_t versus gate length. Fig. 1(b) illustrates the saturation drain current for different gate lengths. The same dependencies for PMOS are shown in Fig. 2. The agreement achieved is within 2% for V_t and $I_{D,\mathrm{sat}}$.

2.3 Circuit Simulation

High speed operation is a key challenge for devices for the rapidly growing portable electronics market. In CMOS digital circuits with static logic, the average gate delay time of a simple inverter chain provides a useful metric for the overall circuit speed. On a test chip a ring oscillator circuit, consisting of a finite inverter chain with the output fed to the input (see Fig. 3 for a circuit with five stages), is often used. By determining the oscillation frequency f_0 of such a ring circuit the average gate delay time t_d of one inverter stage can be calculated using,

$$t_d = \frac{1}{2 \cdot n \cdot f_0} \tag{3}$$

with n being the number of stages.

Our device simulator MINIMOS-NT is equipped with extensive mixed-mode capability including distributed devices. This allows insight into the performance of devices under realistic dynamic boundary conditions imposed by a circuit. However, circuit simulation with distributed devices is rather demanding on computational resources. Therefore using the device simulator for circuits became necessary only for the deep sub-micron technologies where the physics-based compact model in HSPICE is not effective anymore.

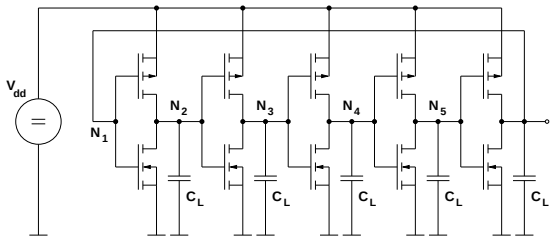

Figure 3: Circuit diagram of a five stage ring oscillator.

The I_d-V_g characteristics simulated by MEDICI and MINIMOS-NT were compared. Excellent agreement (see Fig. 4) should provide comparable gate delay times obtained by HSPICE and MINIMOS-NT. In Fig. 5 the

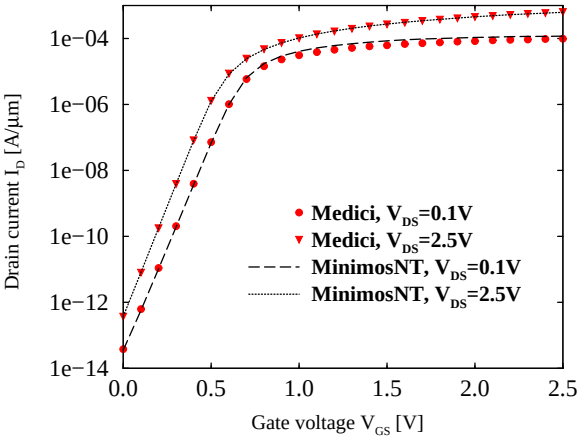

Figure 4: Comparative simulation of a 0.25 μm NMOS Id-Vg characteristics using MEDICI and MINIMOS-NT

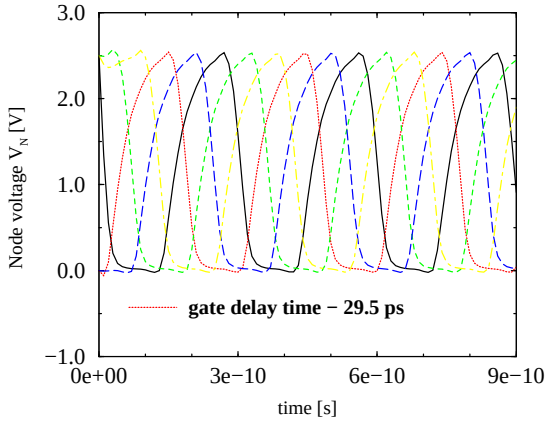

Figure 5: The simulated node voltages of a five stage ring oscillator created with 0.25 μm technology

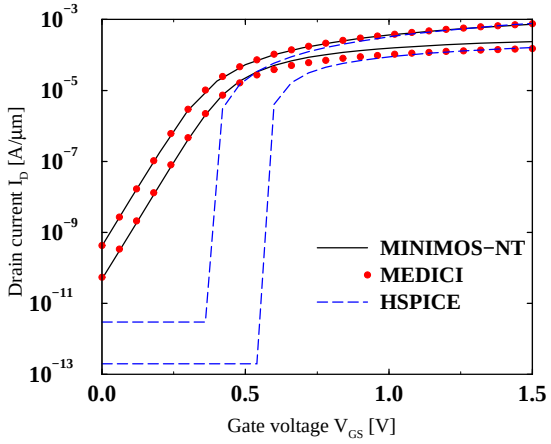

Figure 6: Comparative simulation of a 0.13 μm NMOS Id-Vg characteristics at V_{DS}=0.1 V and V_{DS}=1.5 V using MEDICI, HSPICE, and MINIMOS-NT

MINIMOS-NT simulation results of the 0.25 μm ring oscillator circuit with five stages are shown. The interconnect capacitances C_L are 5.11 fF. The simulation was carried out in transient mixed-mode using basic drift-diffusion (DD) equations. As one can see in Fig. 5 the gate delay is 29.5 ps/stage which is in a very good agreement with the experimental 32 ps/stage and with the 28.6 ps/stage extracted by the HSPICE physical model.

To explore how many stages are sufficient to guarantee accurate results at minimum computational cost, ring oscillator circuits with three, five, and seven inverter stages were simulated. As shown in Table 3, a simulation with five stages is sufficient to achieve the same results for the circuit speed as in simulations with more stages. Table 3 also includes the computer resource expenses for various numbers of ring oscillator stages simulated on a Sun Ultra2 workstation with a clock frequency of 450 MHz.

Table 3: Comparison of calculated gate delays for a different number of inverter ring oscillator stages

stages	delay time	time steps	matrix size	CPU time
3	26.0 ps	120	28 140	7 hours
5	29.5 ps	120	46 900	12 hours
7	29.6 ps	120	65 660	19 hours

3. Characterization of the 0.13 μm Technology

As stated above, for 0.13 μm technology the HSPICE physical model failed to fit the I-V characteristics extracted by MEDICI and it was impossible to estimate the gate delay characteristic of that technology using the old methodology. Fig. 6 shows a comparison between device simulation results from MINIMOS-NT and MEDICI, which are in comparatively good agreement, but very different from the best fit achieved with HSPICE.

Thus, a new approach was applied, in which the process calibration part was kept unchanged and the device simulation and calibration were performed by MINIMOS-NT in the SIESTA optimization TCAD framework. The same distributed devices are then employed in a transient mixed-mode device/circuit simulation, instead of using the MEDICI-HSPICE combination.

The calibrated system, comprising of process simulators (TSUPREM4 - MEDICI) and device simulators (SIESTA - MINIMOS-NT), was applied to 0.13 μm technology. 8 NMOS and 8 PMOS devices, respectively, of different gate lengths (see Table 1) were considered. Device calibration was completed in about eight CPU-hours. Good agreement with measured data

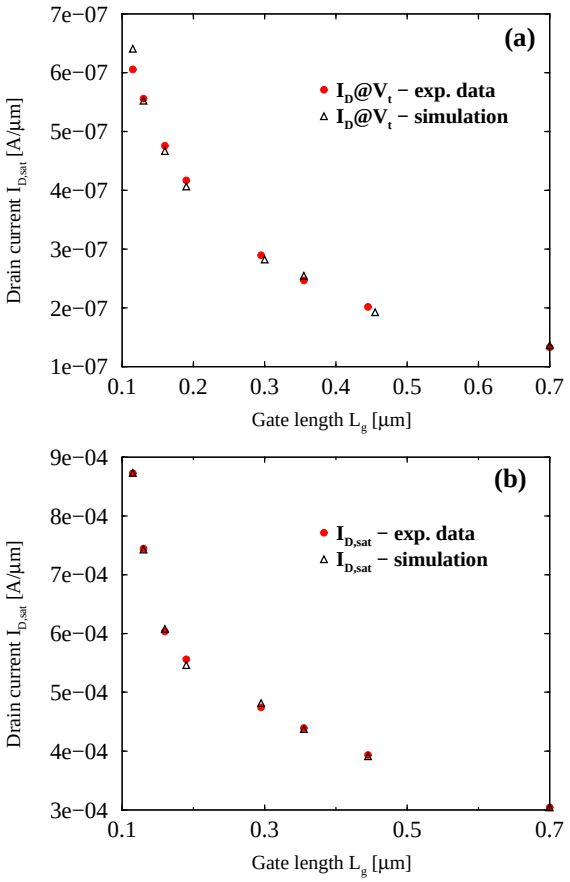

Figure 7: Calibration of the threshold voltage V_t (a) and the saturation current $I_{D,\mathrm{sat}}$ (b) for NMOS devices created with 0.13 μm technology

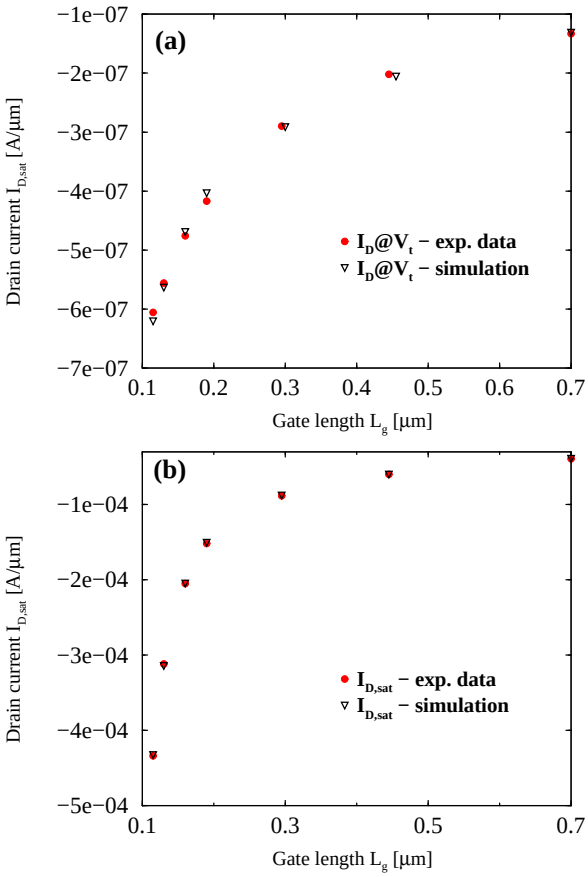

Figure 8: Calibration of the threshold voltage V_t (a) and the saturation current $I_{D,\mathrm{sat}}$ (b) for PMOS devices created with 0.13 μm technology

was achieved for NMOS (Fig. 7) as well as for PMOS (Fig. 8). However the saturation velocity (v_ν^{sat}) resulting from the calibration is $\sim$ 20% higher than the default value of $v_\nu^{sat} = 10^7$ cm/s (see Table 2). Therefore, we performed a comparative hydrodynamic (HD) simulation. Fig. 9 demonstrates significant velocity overshoot over the greater part of the channel length in the nominal 0.13 μm NMOS device compared to the overshoot observed in the 0.7 μm device. In DD simulation this overshoot effect can be accounted for by increasing v_ν^{sat} [12]. Such a change will only slightly influence the long channel devices, but will have a large effect on the short channel ones. Thus, the high value of v_ν^{sat} in our calibration is justified considering that DD simulations were performed.

The calibrated model parameters were used for the circuit simulation. The interconnect capacitances C_L are 3.8 fF. The node voltages of a five stage ring oscillator circuit are depicted in Fig. 10. The simulated inverter delay time is 15.2 ps/stage. In Fig. 11 the gate delay times extracted from several ring oscillators, each with 119 inverter stages (solid line represents the mean value) are compared to simulations (filled circles) performed for two calibrated wafers. The predicted gate delays are within the scatter range of the measured data.

4. Conclusion

A new methodology was established for deep subquartermicron technology characterization. The new approach includes process calibration performed by TSUPREM4 - MEDICI, device calibration carried out by MINIMOS-NT in the SIESTA optimization framework and, finally, mixed-mode circuit simulation with distributed devices made by MINIMOS-NT. The methodology was tested and the tools were calibrated with a 0.25 μm technology. The approach was applied to a 0.13 μm technology characterization. Predicted ring oscillator speed is in excellent agreement with experimental data.

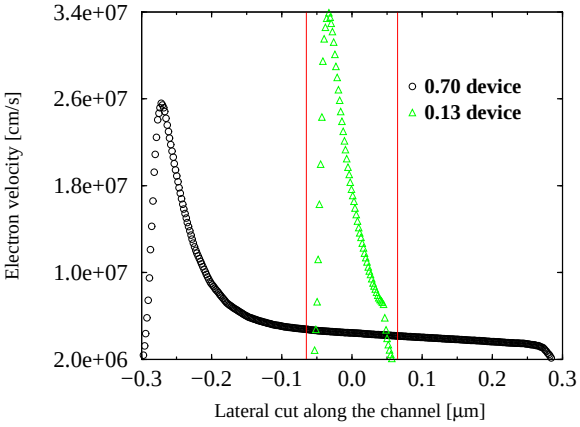

Figure 9: Electron velocity overshoot in the channel of 0.13 μm and 0.7 μm NMOS devices

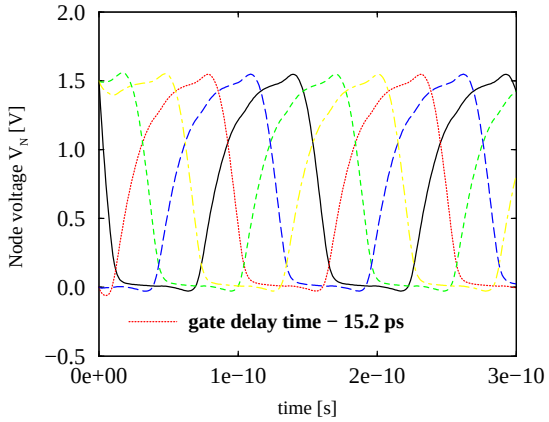

Figure 10: The simulated node voltages of a five stage ring oscillator created with 0.13 μm technology

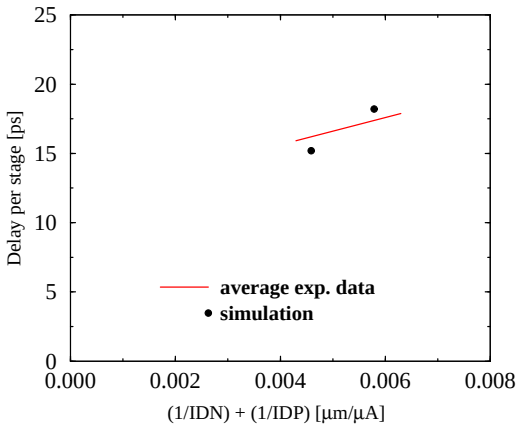

Figure 11: The average experimental gate delay compared to simulation results obtained for two calibrated wafers

Our methodology is extremely beneficial in the early stages of process development for estimation of device performance.

5. Acknowledgment

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