

## Optimization of High-Speed SiGe HBTs

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### Abstract

We present a methodology for characterization and optimization of SiGe HBTs from our 0.8  $\mu\text{m}$  Bi-CMOS technology. It involves process calibration, device calibration employing two-dimensional device simulation, and automated Technology Computer Aided Design (TCAD) optimization. The simulation results show a very good agreement with experimental data. In particular, we perform an optimization of collector doping for specific requirements (high speed or high breakdown voltage).

### 1. INTRODUCTION

Our Silicon-Germanium (SiGe) HBT-CMOS integrated process is based on a proven 0.8  $\mu\text{m}$  mixed-signal CMOS process and includes an additional high performance analog oriented heterojunction-bipolar-transistor (HBT) module. The applications reach from circuits for mobile communication to high speed networks. Using simulation in a predictive manner has been recognized as an integral part of any advanced technology development. In order to satisfy predictive capabilities the simulation tools must capture the process as well as the device physics. Before going into production one can optimize the process steps and estimate device performance characteristics.

Beside mainstream Silicon, the two-dimensional device simulator MINIMOS-NT [1] can deal with different complex materials and structures, such as III-V binary and ternary compounds, and SiGe, with arbitrary material composition profiles. Various important physical effects, such as band gap narrowing, surface recombination, and self-heating, are taken into account. Previous experience gained in the area of III-V HBT simulation which lead to successful results [2] was a prerequisite to use MINIMOS-NT also for simulation of SiGe HBTs. The influence of the selectively-implanted-collector (SIC) implant on device performance was studied both experimentally and by means of process simulation using DIOS [3], followed by two-dimensional device simulation using MINIMOS-NT.

### 2. DEVICE FABRICATION AND PROCESS CALIBRATION

Four Double Base SiGe HBT structures with emitter areas of 2.4  $\mu\text{m}^2$  were epitaxially grown by a Chemical Vapor Deposition (CVD) process.

An implanted n-well, similar to the one used in the standard CMOS technology, is grown during the epitaxial process. The buried layer is connected to a sinker to conduct the electron current from the buried layer to the collector contact. The base consists of an intrinsic base (below the emitter window) and the extrinsic base (highly-doped under the base contact). The Germanium content has a triangular shape. After ion implantation, a Rapid Thermal Processing (RTP) forms the base-emitter junction within the crystalline Silicon.

The process simulation using DIOS starts from the blank wafer to the final device and reflects real device fabrication as accurately as possible. The implant profiles as well as annealing steps were calibrated to one-dimensional SIMS profiles. The simulated device structure with the net doping profile is shown in Fig. 1. To save computational resources the simulation domain covers only one half of the real device which is symmetric and the collector-sinker is not included in the structure. This allows to use very precise simulation grid in areas of interest (Fig. 2). For Dev. 1 high-energy (480 keV)/low-dose, for Dev. 2

high-energy/high-dose, for Dev. 3 low-energy (300 keV)/low-dose, and for Dev. 4 low-energy/high-dose SIC implants were used, as shown in Table 1. This is the only process step in which the four HBTs differ. The Phosphorus doping profiles for the four devices are shown in Fig. 3. A comparative Monte Carlo (MC) simulation of ion implantation of Phosphorus in Si and SiGe was performed to check the accuracy of the process simulation in respect to SiGe (see Fig. 4).

### 3. DEVICE SIMULATION

The physical models in MINIMOS-NT are well calibrated [4], especially for silicon-based devices. The same is true for DESSIS [5] which was used for comparison. Both device simulators correctly reproduced the measured forward Gummel plot at 300 K (see Fig. 5) with the default models. The slight increase of collector current  $I_C$  with dose and energy at high bias is due to the differences in the base push-out effect. Two different methods were used to extract the current gain cutoff frequency  $f_T$ . The first one employs transient S-parameter simulation at 5 GHz and their calculation for the range from 0 to 20 GHz using T-like eight element small-signal equivalent circuit as demonstrated in [6] for GaAs HBTs. The second employs a small-signal ac-analysis as shown in [7]. We found that the results from both methods are in very good agreement.

However, as can be seen in Figs. 6 and 7, both DESSIS and MINIMOS-NT failed to explain the experimentally observed similarity in peak  $f_T$  for Dev. 1 and Dev. 3 and for Dev. 2 and Dev. 4, respectively. This again turned our attention to the SIC implant. An automated device calibration within our TCAD framework [8] was performed. It turned out that 50% more Phosphorus in the collector of the two low-dose devices (Dev. 1 and Dev. 2) already gives acceptable qualitative agreement.

It is known that with shrinking device dimensions non-local effects, such as velocity overshoot, become more pronounced. Neglecting these effects can be a reason for underestimation of  $f_T$  [9, 10]. For that purpose, we performed simulations with the hydrodynamic model (HD) to improve the results (see Fig. 8). Fig. 9 shows the velocity overshoot over the greater part of the base region which is about twice the saturation velocity limit in the drift-diffusion (DD) case ( $10^7$  cm/s). This correlates to the higher electron energy (see Fig. 10) in the collector and explains the increase of  $f_T$  in comparison to DD simulation. The good agreement at low currents is very important since HBTs typically operate at much lower frequencies than at the maximum  $f_T$ . The simulations prove that in this range optimizations of the SIC implant do not have an influence on  $f_T$ , i.e. the base-emitter capacitance and not the base-collector capacitance is the dominating one. The maximum  $f_T$  was found to have a stronger dependence on the dose than on the energy of the implants.

Furthermore, the important figure-of-merit  $BV_{CE0} \times f_T$  (see Table 1) reaches a maximum for high SIC implant energies (deep implant) and high SIC dose. We found that the higher  $f_T$  for high-dose/low-energy SIC implants is due to a smaller base width and a delayed onset of the base push-out effect due to the higher collector doping.

### 4. CONCLUSION

We have presented experiments and simulations of SiGe HBTs. Good agreement was achieved both with experimental DC-results (forward and output characteristics) and with the high-frequency data. We believe the established setup can be beneficial in future for our next process development.

#### Acknowledgment

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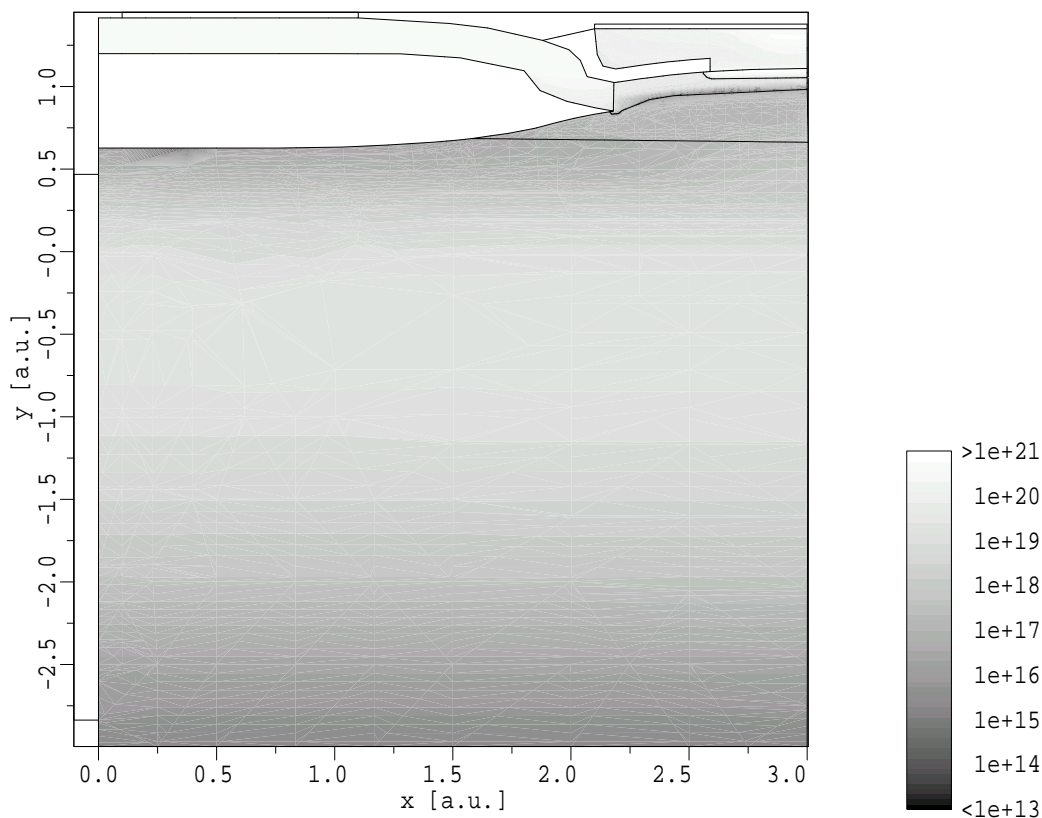


Fig. 1: Simulated device structure and net doping profile [ $\text{cm}^{-3}$ ] (absolute value).

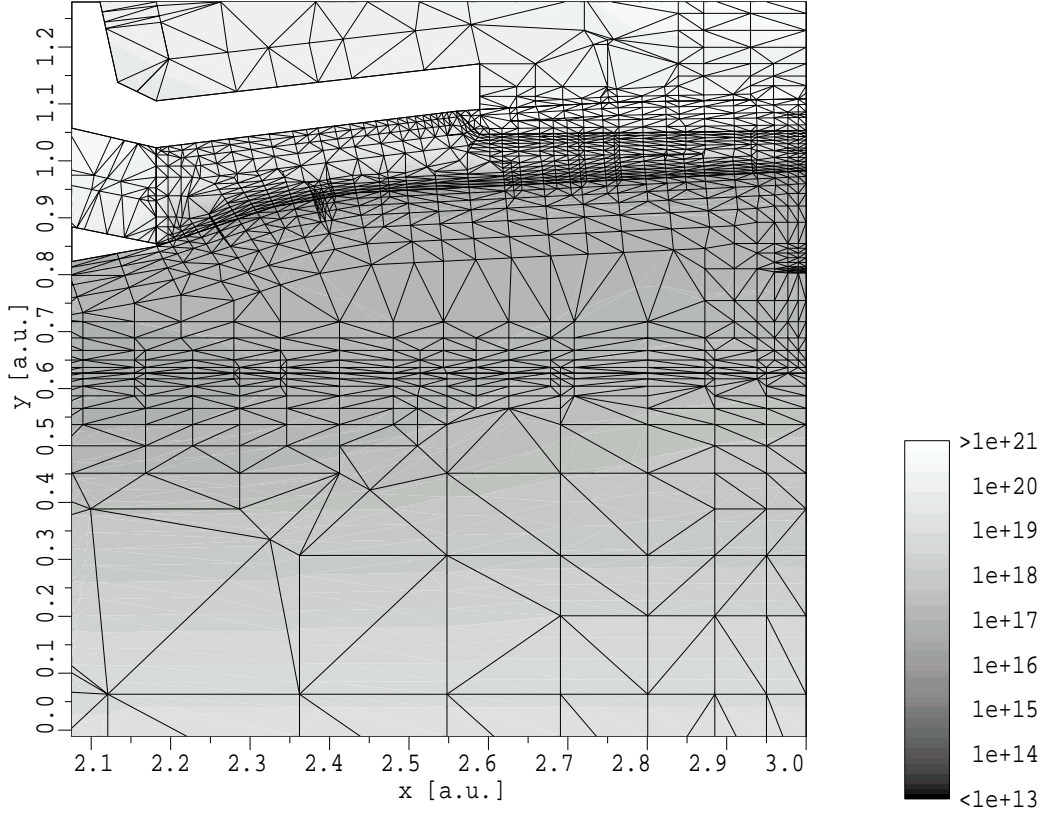


Fig. 2: Gridding example from the active device area.

Device	Energy [keV]	Dose	$f_T$ [GHz]	$BV_{CE0}$ [V]	$f_T \times BV_{CE0}$
Dev.1	480	0.7	32	4.0	128
Dev.2	480	3.0	40	3.7	148
Dev.3	300	0.7	33	3.1	102
Dev.4	300	3.0	42	2.3	97

Table 1: Summary of key process and device parameters.

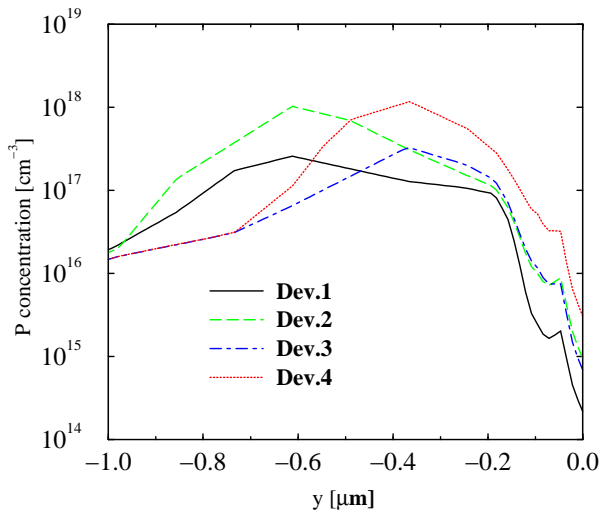


Fig. 3: Phosphorus doping profile under the emitter contact for the four devices.

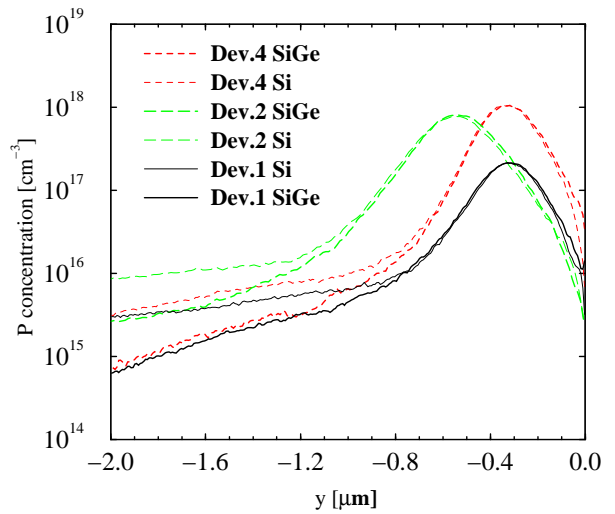


Fig. 4: Comparative simulation of MC ion implantation of Phosphorus in Si and SiGe.

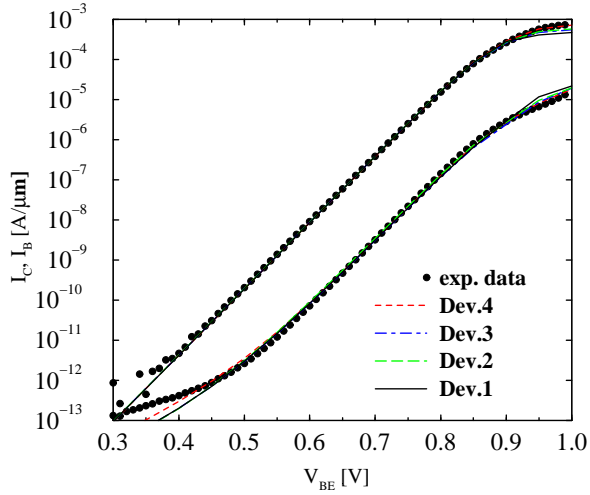


Fig. 5: Forward Gummel plots at  $V_{CB} = 0$  V. Comparison between measurement and simulation.

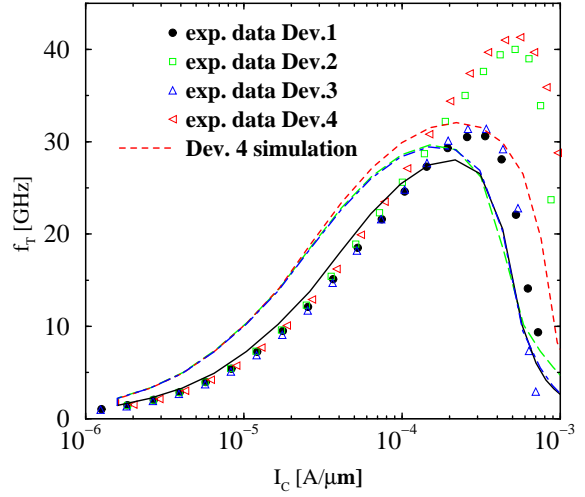


Fig. 6:  $f_T$  vs.  $I_C$  at  $V_{CE} = 1.5$  V. Comparison between measurement and simulation with DESSIS.

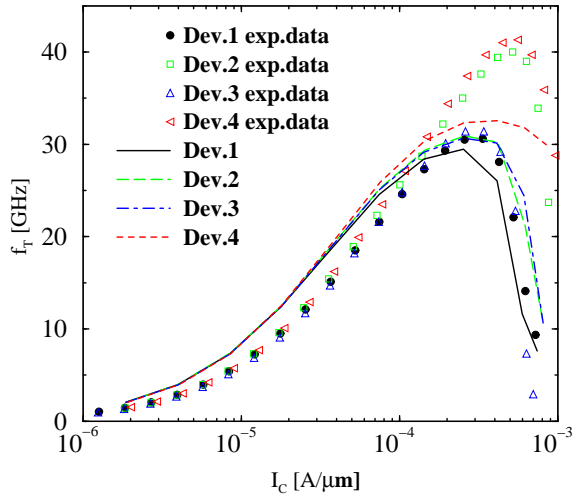


Fig. 7:  $f_T$  vs.  $I_C$  at  $V_{CE} = 1.5$  V. Comparison between measurement and DD simulation with MINIMOS-NT.

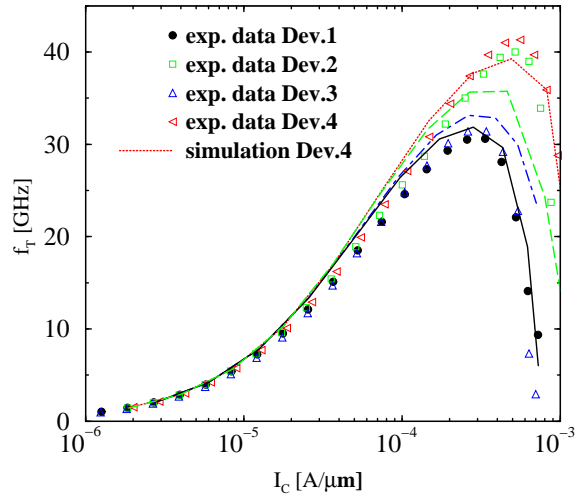


Fig. 8:  $f_T$  vs.  $I_C$  at  $V_{CE} = 1.5$  V. Comparison between measurement and HD simulation with MINIMOS-NT.

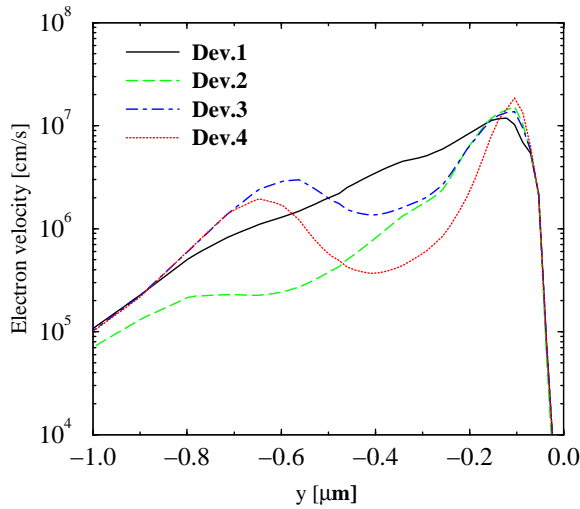


Fig. 9: Electron velocity overshoot in the base-collector space charge region at  $V_{CE} = V_{BE} = 0.88$  V.

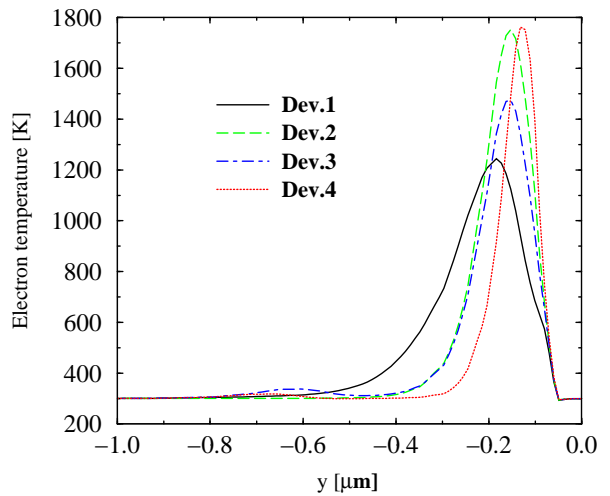


Fig. 10: Electron temperature distribution in the four simulated devices at  $V_{CE} = V_{BE} = 0.88$  V.