Improving Strained-Si on $Si_{1-x}Ge_x$ Deep Submicron MOSFETs Performance by Means of a Stepped Doping Profile

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***Abstract*—We have made use of a stepped doping profile to improve the performance of strained-Si ultra-short MOSFETs. Electron mobility curves are calculated by a Monte Carlo simulator including electron quantization and Coulomb scattering, in addition to phonon and surface roughness scattering. In the first part of the paper, the effect of Coulomb scattering due to both interface charges and bulk impurities is carefully analyzed. We show that the strain enhances the Coulomb-limited mobility due to the interface-trapped charges as a consequence of a better screening of these charges by mobile carriers. However, we also show that this improvement in the Coulomb-limited mobility does not occur if the Coulomb scattering is due to bulk doping impurities, since they share the same physical space with the carriers, and therefore the screening is the same for the same inversion charge concentration. Nevertheless, we have shown that the use of a stepped doping profile bypasses this inconvenience. The introduction of a low doped layer below the oxide reduces the scattering produced by the bulk ionized impurities, enhancing Coulomb-limited mobility in deep-submicron devices. On the other hand, we have seen (by using MINIMOS-NT) that the use of the low doped silicon layer significantly improves the drain current while degrade the turn-off behavior of very short-channel devices only moderately. This design provides the possibility of taking full advantage of the great reduction in phonon scattering produced by the strain in the Si layer in these MOSFETs.**

***Index Terms*—Inversion layers, MOSFETs, SiGe, simulation.**

I. Introduction

THE technological improvements achieved in relation to the growth of $Si/Si_{1-x}Ge_x$ heterostructures have enabled the fabrication of devices in which a very important enhancement in electron mobility has been experimentally observed [1]. For example, significant mobility improvements have been reported, not only in modulation doped heterostructures, but also in n- and p-MOSFETs with strained-Si channels grown on relaxed $Si_{1-x}Ge_x$ substrates, manufactured using standard CMOS processing [2]–[4].

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As is well known, mobility improvement in strained-Si channel MOSFETs is mainly due to the following two facts:

1) the reduction in the carrier conductivity effective mass;
2) the reduction in the intervalley phonon scattering rates [5]–[7].

Both facts are a consequence of the splitting of the six-fold degeneracy in the Si conduction band minimum caused by the strain [8]. The six-fold degenerate valleys separate into two groups: two lowered valleys with longitudinal mass axis normal to the interface, and four raised valleys with longitudinal mass axis parallel to the interface [8], [9]. According to the above, most of the inversion electrons, which will occupy the two lower valleys, will have a lower conductivity effective mass for transport in the direction parallel to the interface. Intervalley phonon scattering rates are also reduced by the valley splitting due to the separation of the energy levels associated with each type of valley. In this respect, the intervalley scattering rate between nonequivalent valleys (f scattering events) is reduced since the energy difference between initial and final states increases and, therefore, the scattering processes are less likely [5]–[7] [10], [11].

In a previous paper we studied the isolated contribution of the two effects to mobility improvement as strain increases [6]. In the conclusions, we reported that the contribution of the reduction of intervalley scattering is not as important as the contribution of the reduction of conductivity-effective mass in the low longitudinal-electric-field transport regime; in other words, the reduction of the conduction effective mass is the main factor responsible for low-field mobility improvement in strained channels. In the same paper, we showed that a reduction in the intervalley scattering rate mainly produces a stronger electron velocity overshoot effect as the Ge mole fraction increases.

Previous studies performed have focused on the contribution of surface-roughness and phonon scattering mechanisms to inversion layer low-field mobility [6], [12]. However, we should not forget the role of Coulomb scattering, specially now, when strained-Si MOSFETs are the subject of a debate to try to clarify the use of these devices as alternatives to existing deep-submicron CMOS technologies.

Short-channel effects are usually controlled by increasing the channel-doping concentration, thus suppressing the spread of source and drain depletion layers. Therefore, as the channel length is scaled down to 0.1 μm and below, the doping concentration must be raised to values around 1×10^{18} cm^{-3}. Such high bulk-impurity concentrations lead to an increase

in threshold voltage and to an important decrease in electron mobility, which strongly degrades the electrical properties of the device [13]–[16], [19]. The reduction in electron mobility caused by Coulomb scattering is so important that it is becoming one of the main limiting agents that have to be dealt with in order to continue the dimension reduction process.

Bearing in mind the above, it is clear that a study of the influence of Coulomb scattering on the transport properties of electrons in strained inversion layers is welcome in order to accurately assess the suitability of strained-Si/SiGe deep-submicron MOSFET technology.

To do this, we implemented a Monte Carlo (MC) simulator and made use of MINIMOS-NT [20] to evaluate, respectively, electron mobility and the drain current in strained Si on relaxed $Si_{1-x}Ge_x$ MOSFETs. The effect of Coulomb scattering on electron mobility in strained $Si/Si_{1-x}Ge_x$ is summarized in Section II. We found a very interesting and curious pattern of electron mobility depending on where the scattering centers are located. Thus, if the main source of Coulomb scattering centers is the interface trapped charge, the greater the germanium mole fraction the lower the Coulomb scattering, and therefore the higher the electron mobility. However, in the case where Coulomb scattering is mainly due to substrate doping impurities, the strain does not contribute at all to reducing Coulomb scattering. A physical explanation of this behavior is provided in Section II.

We will see in Section III that to take advantage of the strain and thus improve the Coulomb limited mobility in highly doped samples we should physically separate bulk impurities from inversion layer electrons. An easy method to achieve this separation between bulk impurities and channel carriers is to make use of a stepped doping profile [13]–[15]. In Section III, electron mobility curves and I–V characteristics of stepped doping profile strained silicon MOSFETs are provided. A comparison of these results with those obtained in unstrained-Si devices is also shown. Finally the main conclusions of our work are presented in Section IV.

II. Coulomb Scattering in Strained $Si/Si_{1-x}Ge_x$ MOSFETs

In order to study the effect of Coulomb scattering we developed a comprehensive Coulomb scattering model [21] that includes the effects of the charged-center space correlation and the random nature of the charged centers in the Born approximation. Using this model we were able to accurately reproduce experimental effective mobility in unstrained silicon inversion layers, in a wide variety of situations [22], [23]. We used this Coulomb scattering model in the framework of a one-electron Monte Carlo simulator, which enabled us to study the stationary transport properties of the electrons in such devices, and, in particular, to evaluate the stationary drift velocity and the low-field electron mobility.

Electron quantization in the inversion layer has been shown to play a very important role in the performance of these devices, and therefore, it was properly taken into account in our simulation. To do so, the Poisson and Schroedinger equations were self-consistently solved. A detailed description of this simulation can be found elsewhere [21]–[23]. In addition, the nonparabolicity of conduction band effects has been included [24]. In this work, the effect of the strain is included only in the band structure as the valley splitting energy $\Delta E = 0.67x$ (x being the Germanium mole fraction) between the two lowered valleys with longitudinal mass axis parallel to the interface and the four raised ones with longitudinal mass perpendicular to the interface, assuming that the strain does not modify the shape of the valleys. Changes in nonparabolicity with strain were neglected as second-order effects. The effective masses of electrons were assumed to be the same as in unstrained silicon, as is usually done. The coupling constants for phonon scattering were also assumed to remain unchanged.

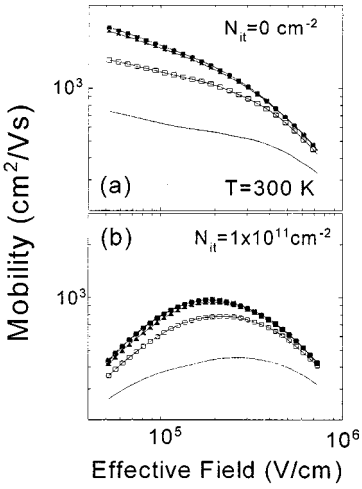

Fig. 1. Electron mobility: (a) without Coulomb scattering and (b) including Coulomb scattering versus transverse effective field at room temperature in strained silicon inversion layers grown on $Si_{1-x}Ge_x$ for a low doped substrate ($N_A = 9 \times 10^{14}$ cm^{-3}) (solid line: $x = 0$; □ : $x = 0.1$; ▲ : $x = 0.2$; • : $x = 0.3$; ■ : $x = 0.4$).

A. Interface-Trapped Charge

In the first instance, we analyzed the effect of the Coulomb interaction due to the charged centers located right at the interface or inside the oxide. Therefore, we assumed a low uniform doping concentration ($N_A = 9 \times 10^{14}$ cm^{-3}), and that the Coulomb scattering is only due to charges trapped right at the interface. The simulated MOSFET structure was formed by a strained silicon layer (10 nm thick) grown epitaxially on a relaxed $Si_{1-x}Ge_x$ substrate. The oxide thickness was assumed to be 5 nm. Fig. 1 shows simulated mobility curves assuming (a) no Coulomb scattering and (b) an interface charged layer of $N_{it} = 1 \times 10^{11}$ cm^{-2}, for strained silicon inversion layers.

In the present case, as the Coulomb scattering is only due to charges trapped right at the interface, i.e., right at the limit of the electron distribution, there is a spatial separation between electrons and Coulomb scattering centers [8]. In this situation, a modification of the electron distribution in the direction perpendicular to the interface (in order to move it closer to the interface-trapped charge) causes the screening to increase, thus decreasing Coulomb scattering, even when the proximity of the carriers to the scattering centers is lower and therefore

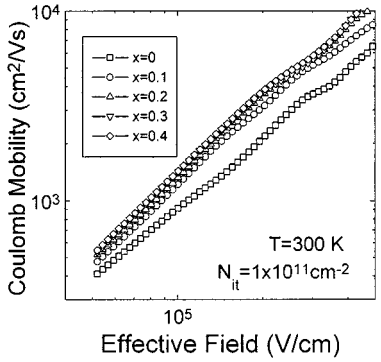

Fig. 2. Coulomb limited mobility versus transverse effective field at room temperature in strained silicon inversion layers grown on $Si_{1-x}Ge_x$ for different values of the Ge mole fraction.

the bare scattering potential (that is to say, without screening) is stronger. This is what happens when the population of the ground subband is increased as a consequence of valley splitting as the germanium mole fraction, and therefore the strain, increases. This effect is similar to what happens in an unstrained silicon inversion layer when the transverse effective field increases: the Coulomb limited mobility increases thanks to a higher screening, even though carriers are closer to the scattering centers.

To show the effect of the strain on the Coulomb scattering, we made use of the Matthiessen rule and the mobility curves of Fig. 1 to isolate the Coulomb scattering contribution to the mobility (Fig. 2). The following conclusions can be drawn.

1) As mentioned above, the well-known fact that the greater the effective field the greater the Coulomb limited mobility, as a consequence of better screening of the interface charges by the mobile carriers [23] even when the greater the effective field the closer the electrons are to the interface-trapped charges.
2) For a fixed value of the transverse electric field, the greater the Germanium mole fraction the greater the Coulomb limited mobility. As the Germanium mole fraction increases, the higher band splitting causes the ground subband population to increase, thus decreasing the number of electrons in the excited subbands. Therefore, the screening of the charged centers by the mobile carriers will be more effective, thereby reducing Coulomb scattering, and increasing the electron mobility.

This latter result is very important since it proves that the strain also contributes to improve electron mobility by decreasing the Coulomb scattering effects and not only by reducing intervalley scattering and the conduction effective mass as has been maintained until now.

In this context, we would like to draw the reader's attention to the important role of quantization: if quantum effects are ignored, screening only depends on the total inversion charge, and therefore, no Coulomb mobility enhancement would be appreciated as strain increases.

B. Doping Impurity Charge

In the previous analysis we considered a very low doped substrate. Nevertheless, in state-of-the-art technology, very high nonuniform doped substrates are used to avoid short-channel effects. In such cases, channel impurity profiles are carefully selected to obtain higher transconductances and to prevent punchthrough [13], [15]. We have considered one of these channel impurity profiles, and studied the effect of the strain on the Coulomb scattering due to this doping profile. The profile considered was the result of an ion implantation (BF_2^+, 100 KeV, 1×10^{13} cm^{-2}) over a substrate concentration of 8.85×10^{15} cm^{-3}. Although this profile has a peak concentration of 1×10^{18} cm^{-3} at about 0.06 μm under the silicon surface, the doping impurity concentration right at the interface is 2×10^{17} cm^{-3}. Therefore, in this case, in contrast to the case studied above, there is no physical separation between Coulomb scattering centers and inversion electrons. Furthermore, a modification of the electron distribution in the direction perpendicular to the interface does not modify the proximity of the electrons to the bulk impurities and thus the screening (in this case only a modification of the total number of carriers, not its redistribution in the different subbands, would modify the screening). Fig. 3 shows electron mobility curves (a) and Coulomb limited mobility (b) for different Germanium mole fractions. Fig. 3(b) shows that Coulomb scattering is very slightly improved by the strain, since screening is hardly modified by the strain as explained above. Nevertheless, it is worth noting that Fig. 3(a) shows that as the effective field increases, so that Coulomb scattering is not dominant, mobility curves separate, maintaining the enhancement provided by the intervalley scattering and conduction effective mass reduction.

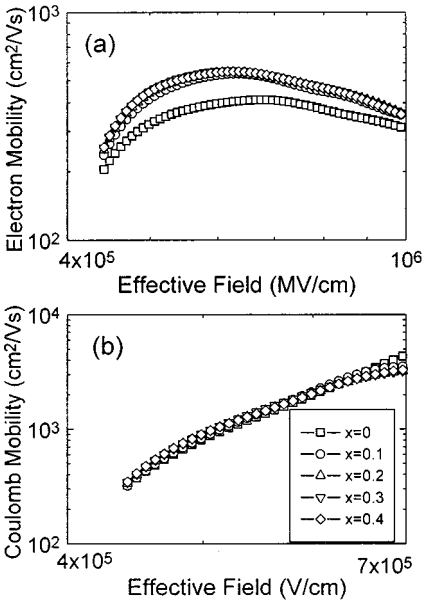

Fig. 3. (a) Electron mobility including Coulomb scattering versus transverse electric field at room temperature in strained silicon inversion layers grown on $Si_{1-x}Ge_x$ for a high doped substrate. (b) Coulomb limited mobility for the same devices as in Fig. 3(a).

III. Stepped-Doping Profile

As established above, the strain does not contribute to improving the mobility behavior in highly doped substrates due to the fact that carriers and Coulombic centers share the same

physical space. As a consequence, the carrier redistribution due to the strain does not enhance the effect of the screening and therefore, does not improve the mobility. Therefore, if we want to take advantage of the strain to improve the Coulomb limited mobility we should physically separate carriers and scattering centers (doping impurities), and thus, a modification of the carrier distribution in the channel could effectively modify the screening, reducing the total Coulomb scattering rate.

In doing this, it is clear that Coulomb scattering would be reduced as a consequence of the greater distance between scattering centers and carriers, but not only or even mainly due to this reason, but rather as the Ge mole fraction increases (and therefore so does the strain), by a more effective screening (which becomes the main reason for the decrease in Coulomb scattering) [16]–[18].

To test the previous statement, two types of MOSFET were simulated. Basically, both devices consist of a low-doped ultrathin silicon layer over a heavily doped substrate, which in the strained case is $Si_{1-x}Ge_x$, and in the unstrained case is just Si. In the first case, the epitaxial silicon layer is strained as a consequence of the different lattice constants of silicon and silicon-germanium, while in the second case, the epitaxial silicon layer is unstrained, since it is grown on a silicon substrate. In both cases, the thickness of the epitaxial silicon layer is denoted as x_i, and its doping density is set equal to $N_{\text{low}} = 10^{14}$ cm^{-3}. This means that for the strained-silicon channel case, the low doped layer exactly coincides with the strained silicon layer. The Ge mole fraction was assumed to be $x = 0.3$. The doping concentration of the substrate was $N_{\text{high}} = 10^{18}$ cm^{-3} in all devices. For the sake of simplicity, we also assumed that the stepped doping profile was perfectly abrupt. In both devices, oxide thickness was $T_{\text{ox}} = 5$ nm, and a p^+-poly gate was assumed.

The width of the depletion region in the centre of the channel was calculated following the procedure explained in [16] assuming that drain and source junction depths are 30 nm. Basically, the same results reported in [16] for conventional-Si MOSFETs were obtained for the strained-Si case, that is to say, the depletion region width remained fixed until $x_i = 30$ nm, and then increased concomitantly with x_i. In this respect, short channel effects are under control as in high-uniform-doping MOSFETs both in the unstrained- and strained-Si cases for $x_i < 30$ nm.

A. Electron Mobility Curves

Electron mobility curves versus transverse effective field are plotted in Fig. 4(a) for unstrained-Si devices and in Fig. 4(b) for strained-Si devices, considering different thicknesses of the low-doped silicon layer. Typical interface charges were used in each case: $N_{\text{it}} = 4 \times 10^{10}$ cm^{-2} for the unstrained-Si MOSFETs [16] and $N_{\text{it}} = 1 \times 10^{11}$ cm^{-2} for the superficial strained-$Si/Si_{0.7}Ge_{0.3}$ channel MOSFETs [2]. It is necessary here to draw the reader's attention to Curve 1 in Fig. 4(b). This mobility curve corresponds to a device with a low-doped silicon layer 30 nm thick, grown over a $Si_{0.7}Ge_{0.3}$ substrate that, in this case, also remains undoped ($x_i = \infty$). So, in this case, the thickness of the strain silicon layer does not coincide with the thickness of

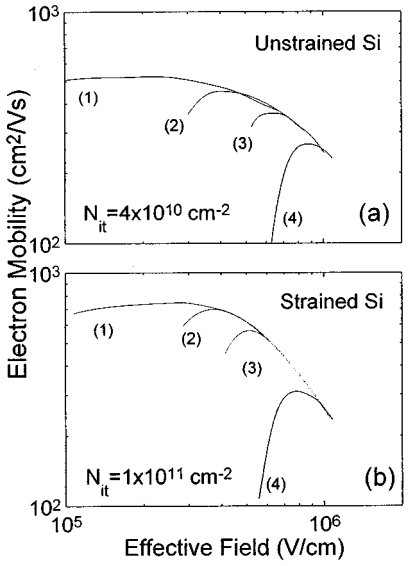

Fig. 4. (a) Mobility curves versus effective-electric field at room temperature for conventional Si with a typical interface-charge concentration of $N_{\text{it}} = 4 \times 10^{10}$ cm^{-2}. The different values of x_i used are: (1) ∞, (2) 30 nm, (3) 10 nm, (4) 0 nm. (b) Mobility curves versus effective-electric field at room temperature for a superficial strained-$Si/Si_{0.7}Ge_{0.3}$ channel MOSFETs with a typical interface-charge concentration of $N_{\text{it}} = 10^{11}$ cm^{-2}. The different values of x_i used are: (1) $T_w = 30$ nm, $x_i = \infty$, (2) $T_w = x_i = 30$ nm, (3) $T_w = x_i = 10$ nm, (4) $T_w = 30$ nm, $x_i = 0$ nm. In both figures ($T_{\text{ox}} = 5$ nm, $N_{\text{low}} = 10^{14}$ cm^{-3}, $N_{\text{high}} = 10^{18}$ cm^{-3}).

the low-doped zone. From the comparison of Fig. 4(a) and (b), the following facts can be observed.

1) In both devices, electron mobility increases as the low doped-layer thickness increases, as expected from the greater separation between inversion charge electrons and bulk impurities [16].
2) It is also clear that mobility in strained devices [Fig. 4(b))] is higher than mobility in unstrained ones [Fig. 4(a)]. This behavior is as expected, due to the reduction in conduction effective mass and the reduction in the intervalley scattering rate [6], [7].
3) The comparison of Curves 1 and 2 in the two figures indicates that Coulomb scattering is also reduced in the strained case (Fig. 4(b)), even when the interface charge concentration is much higher than in the unstrained case ($N_{\text{it}} = 10^{11}$ cm^{-2} in the strained case versus $N_{\text{it}} = 4 \times 10^{10}$ cm^{-2} in the unstrained case). As established in Section II above, this behavior could be also predictable as a consequence of the more effective screening of the interface-trapped charge (when they comprise the main Coulomb scattering source) due to the greater population within the ground subband in the strained case.

In order to understand, from a physical point of view, the causes of the Coulomb scattering reduction that is obtained in strained-Si MOSFETs, we studied the mobility curves of these devices step by step.

Mobility curves for strained- and unstrained-Si devices for $x_i = 30$ nm (open squares) and $x_i = \infty$ (solid line) are plotted in Fig. 5(a), taking into account only the effect of the bulk impurities in the Coulomb scattering rate calculation, that is to say,

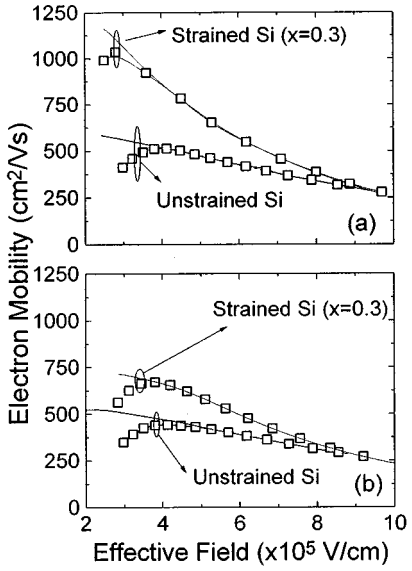

Fig. 5. Mobility curves versus effective-electric field for conventional Si and superficial strained-Si/$Si_{0.7}Ge_{0.3}$ channel MOSFETs at room temperature. The mobility curves including Coulomb scattering mechanisms are plotted in open squares; solid lines show mobility curves with this scattering mechanism off. ($T_{ox} = 5$ nm, $N_{low} = 10^{14}$ cm^{-3}, $N_{high} = 10^{18}$ cm^{-3}, $T_w = x_i = 30$ nm). In (a) $N_{it} = 0$ cm^{-2}. In (b) $N_{it}(\text{Unstrained}) = 4 \times 10^{10}$ cm^{-2}, $N_{it}(\text{Strained}) = 1 \times 10^{11}$ cm^{-2}).

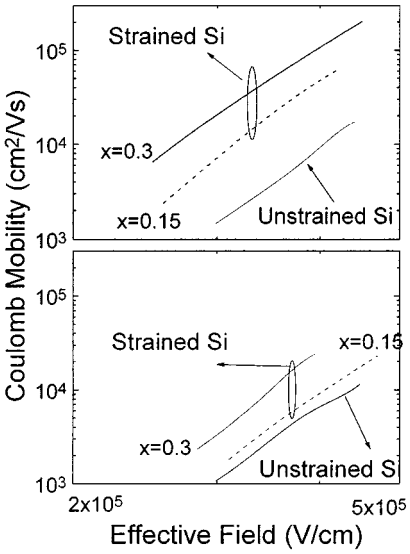

Fig. 6. Coulomb limited mobility for the same devices as in Fig. 6 at room temperature. ($T_{ox} = 5$ nm, $N_{low} = 10^{14}$ cm^{-3}, $N_{high} = 10^{18}$ cm^{-3}, $T_w = x_i = 30$ nm). In (a) $N_{it} = 0$ cm^{-2}. In (b) $N_{it}(\text{Unstrained}) = 4 \times 10^{10}$ cm^{-2}, $N_{it}(\text{Strained}) = 1 \times 10^{11}$ cm^{-2}.

assuming a null interface charge ($N_{it} = 0$). The separation between the two mobility curves (solid and open-squares curves) is smaller in the strained case. This means that the contribution of Coulomb scattering in the strained-Si case is lower than in unstrained-Si. This fact can be observed more clearly in Fig. 6(a), where Coulomb limited mobility was extracted by using the Mathiessen rule. In Fig. 6(a), we have also added the Coulomb-limited mobility curve corresponding to a less strained-sample ($x = 0.15$) in order to observe the gradual effect of the strain on the Coulomb limited behavior.

Fig. 6(a) only corroborates the results previously obtained for the interface-trapped charge in Section IIA, but now for the doping impurity charge. In addition to the well-known fact that the greater the effective field the greater the Coulomb limited mobility, as a consequence of the better screening of the charged centers by the mobile carriers [22], the following conclusions can be drawn from Fig. 6(a).

1) For a fixed value of the transverse electric field, the Coulomb limited mobility due to bulk impurities is much higher in the strained case than in the unstrained one. As the Germanium mole fraction increases, the higher band splitting causes the ground subband population to increase, thus decreasing the number of electrons in the excited subbands. Therefore, the screening of the doping impurities (which are now separated from the carriers) by the mobile carriers will be more effective, thereby reducing Coulomb scattering and increasing electron mobility. It is worth stressing this result, since in nonstepped doping substrate devices, Coulomb-limited mobility in strained and unstrained silicon channels almost coincides, as shown above [Fig. 3(b)]. Therefore, the improvement in Coulomb limited mobility due to the strain in this kind of highly-doped substrates is a direct consequence of the stepped-doping profile.

In order to consider the simultaneous effect of interface-trapped charge and doping impurities, the same mobility curves shown in Fig. 5(a) are plotted in Fig. 5(b), adding a typical interface-charge in both types of devices in the Coulomb scattering rate calculation ($N_{it} = 4 \times 10^{10}$ cm^{-2} for a conventional-Si MOSFET and $N_{it} = 10^{11}$ cm^{-2} for a surface strained-Si/$Si_{0.7}Ge_{0.3}$ MOSFET). Once more, we obtained the Coulomb limited mobility by using Matthiessen's rule [Fig. 6(b)]. Despite the greater interface charge concentration in the strained case, Coulomb limited mobility remains much higher than in conventional-Si devices. This means that the mobility enhancement obtained by the improvement of screening by the strain is much more important than the reduction that the much greater interface trap concentration of these devices would produce. In this respect, the use of these stepped doping profile structures in strained-Si MOSFETs could be an interesting alternative to support the role they might play when they are considered as serious alternatives to conventional-Si CMOS technology.

B. Simulation Results

Device simulations have been performed to show the effect of the stepped doping profile and the strained Si layer on the device performance. The mobility data depicted in Fig. 5(b) has been used in tabulated form in MINIMOS-NT [20]. The mobility roll-off at small effective field strengths has been neglected in the simulation. Instead, mobility was kept at its maximum value down to zero field in order to extend the mobility data to the whole field range, which is in qualitative compliance with analytical surface mobility models [25], [26]. The quantum correction of Hänsch is employed [27] to ensure a more realistic distribution of the inversion layer charge in the conventional device simulation.

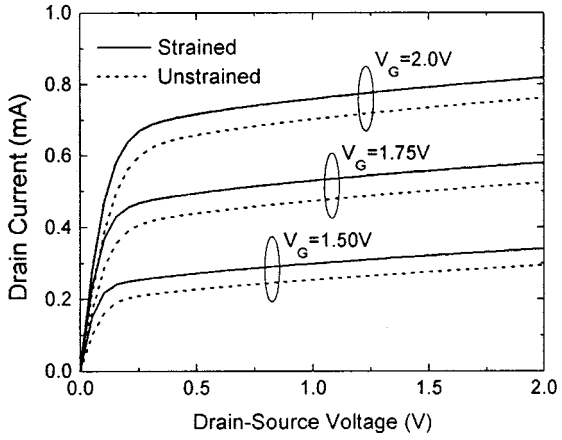

Fig. 7. Simulated output characteristics for the strained ($Si/Si_{0.7}Ge_{0.3}$) and unstrained channel devices. The parameters of the devices are $L_G = 100$ nm, $T_{ox} = 2.5$ nm, $N_{low} = 10^{14}$ cm^{-3}, $N_{high} = 10^{18}$ cm^{-3}, $T_w = x_i = 30$ nm, $N_{it}(\text{Unstrained}) = 4 \times 10^{10}$ cm^{-2}, $N_{it}(\text{Strained}) = 1 \times 10^{11}$ cm^{-2}.

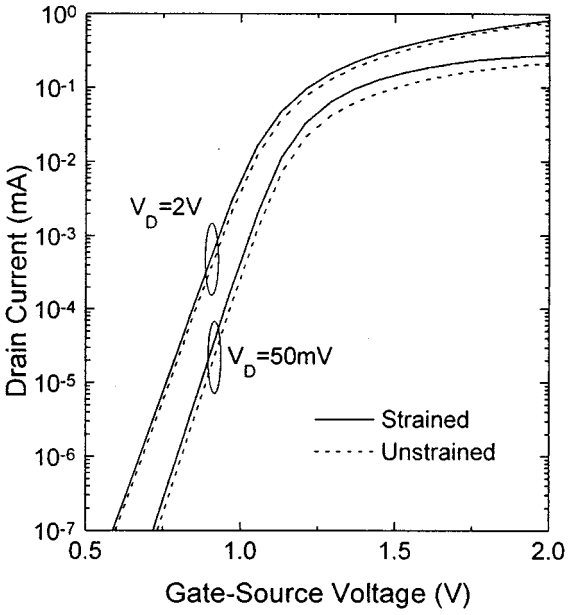

Fig. 8. Subthreshold characteristics of the simulated devices in Fig. 7.

Fig. 7 shows the simulated output characteristics for the strained and unstrained channel devices. The parameters of the devices are $L_G = 100$ nm, $T_{ox} = 2.5$ nm, x_i, the thickness of the low doped Si layer, equals 30 nm, and for the substrate doping $N_A = 10^{18}$ cm^{-3} is assumed. The on-current at $V_{DS} = 2$ V of the unstrained device is already as high as 760 μA/μm, whereas strain increases this figure up to 820 μA/μm.

In Fig. 8 the subthreshold characteristics of the simulated devices are depicted. From these results the subthreshold swing at $V_{DS} = 2$ V is estimated by $S_t = 85$ mV/dec, whereas drain induced barrier lowering (DIBL) is extracted as 52 mV/V at $I_{DS} = 0.1$ μA/μm. To show the influence of the low doped Si layer on the turn-off behavior, a device without such layer is simulated. That is, $N_A = 10^{18}$ cm^{-3} both in the channel and the substrate. For this device the extracted parameters are $S_t = 75$ mV/dec and DIBL $= 43$ mV/V. These comparative simulations show that the measures taken to optimize the on-current degrade the turn-off behavior of the device only moderately.

IV. Conclusion

We have studied the effect of Coulomb scattering on electron mobility due to both silicon bulk impurities and to the interface trapped-charge in strained-Si on $Si_{1-x}Ge_x$. It has been demonstrated that strain contributes to enhancing Coulomb limited mobility when charged centers and electrons are physically separated, since in this way the strain enhances the screening effect. We have also studied in depth the mobility improvement obtained in superficial strained-Si devices when a low doped layer is introduced beneath the oxide in deep-submicron devices. It is shown that this design can enhance the mobility at low effective fields by reducing Coulomb scattering and therefore taking full advantage of the conduction effective mass and phonon scattering reduction that can be obtained in strained-Si MOSFETs. Finally, we have seen (by using MINIMOS-NT) that the use of the low doped silicon layer significantly improves the drain current while degrade the turn-off behavior of very short-channel MOSFETs only moderately.

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