HIGH-VOLTAGE SUPER-JUNCTION SOI-LDMOSFETS WITH REDUCED DRIFT LENGTH

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Abstract. We describe high-voltage super-junction SOI-LDMOSFETs which have a trench oxide in the drift region. The super-junction helps to increase the effective drift doping. The trench oxide in the drift region allows to reduce the drift length without degrading the breakdown voltage. With the proposed device structure a reduction of the on-resistance of the n-drift layer can be achieved. The breakdown voltage and the specific on-resistance of the suggested devices as a function of the trench oxide depth, the p-column width, and the doping are studied. Using the two-dimensional numerical simulator MINIMOS-NT, we confirm that the specific on-resistance of the device proposed is lower than that of conventional SOI-LDMOSFETs, and the drift length is reduced to 65% compared to conventional devices.

INTRODUCTION

Lateral double diffused MOS transistors (LDMOSFETs) on SOI (Silicon on Insulator) have attracted much attention in a wide variety of applications such as automotive applications, consumer electronics, telecommunications, and industrial applications [1]. Advantages of SOI technology are the superior isolation, reduced parasitic capacitances and leakage currents, and the superior high temperature performance compared to the traditional junction isolation (JI). The isolation area of the JI becomes larger as the voltage rating of the device is increased. In the case of SOI devices it depends on only the fabrication process, this results in a compact chip size of high-voltage devices. These advantages allow efficient monolithic integration of multiple power devices and low-voltage control circuitry on a single chip. The main issues in the development of these devices is to obtain the best trade-off between the specific on-resistance (R_{sp}) and the breakdown voltage (BV), and to shrink the feature size without degrading device characteristics. In order to achieve these requirements new structures such as super-junctions (SJ) [2], buried gate oxide devices [3], LUDMOSFETs [4], and trench lateral power MOSFETs with a trench bottom source contact (TLPM/S) [5] have been proposed. Vertical SJ devices such as COOLMOS [6] and MDmesh [7] assume complete charge balance of the depletion layer. This can be achieved by introducing alternating n and p columns in the drift region, which allows to drastically increase the doping in this region. The doping of the columns has the inverse relationship with the width of each columns. Even the current conduction area is reduced by additional

p-columns which do not contribute towards on-state conduction. This results in significant reduction in $R_{\rm sp}$ of the devices. Recently the lateral SJ SOI-LDMOSFET [8] which has a channel on the side wall of the device was proposed to improve on-state characteristics. The channel can be made by the lateral trench gate, and it increases the channel area.

To obtain the best trade-off between $R_{\rm sp}$ and BV, we suggest a SJ SOI-LDMOSFET which has an extra p-column and a trench oxide in the drift region. The extra p-column is doped to achieve a balanced charge condition which means that the net depletion layer charge is zero. The trench oxide in the p-column helps to reduce the drift length without further decreasing the conduction area (only the n-column contributes to the current conduction). The $R_{\rm sp}$ of the proposed structure is effectively reduced by the SJ concept together with the trench oxide. SJ helps to increase the doping concentration of the n-drift layer, and the trench oxide in the drift allows to reduce the device size. Lowering $R_{\rm sp}$ without degrading the BV gives rise to a reduction in silicon area, and it allows for the economic fabrication of smart power devices. Two-dimensional numerical simulations with MINIMOS-NT [9] have been performed to investigate the influence of device parameters on $R_{\rm sp}$ and BV.

DEVICE STRUCTURES AND OPERATION

Figure 1 shows the schematic structure of the proposed SJ SOI-LDMOSFET which has a trench oxide in the drift region. This structure can be made by introducing buried p-columns in the drift region and by an additional trench process. Generally the maximum BV of the conventional SOI-LDMOSFET is limited by the thickness of the buried oxide. The optimum drift length must be ensured to get the best trade-off between $R_{\rm sp}$ and BV. With the structure proposed it is possible to reduce the drift length drastically without degrading the maximum BV by increasing the surface path of the drift layer. This buried p-column can be connected to the p-body directly or indirectly. The optimum p-column doping concentration is determined by the width of the p-column and the net charge of the n-column.

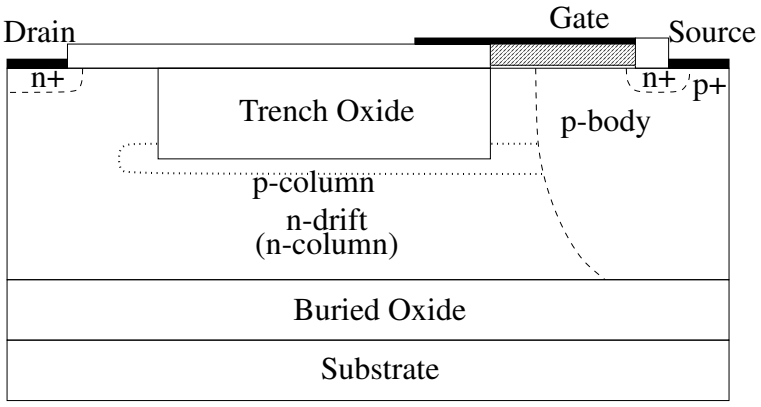

Figure 1. Schematic of the SJ SOI-LDMOSFET with a trench oxide in the drift. It has a buried p-column in the n-drift region.

Our device is designed to achieve a BV of 300 V with an SOI thickness $t_{\rm soi}$ of 7.0 μm and with a buried oxide thickness $t_{\rm ox}$ of 2.0 μm. With these structure parameters the maximum BV of conventional SOI-LDMOSFETs is 300 V at the minimum allowable drift length of 20.0 μm. The main focus of the paper is to optimize the device parameters of the proposed structure shown in Figure 1. The trench oxide depth affects the BV and it must be designed to ensure a long enough surface path of the device. It is important to minimize the p-column width, because it shrinks the conduction area of the device. n and p-column doping concentrations are a function of the column width. The n-column doping must be increased to lower the on-resistance of the SJ devices. Simulations are performed to find optimum device parameters with a trench oxide depth from 2.0 to 3.0 μm and a p-column width from 0.3 to 1.3 μm. With an n-column width $W_{\rm N}$ of 4.0 μm, a p-column width $W_{\rm P}$ of 0.3 μm and a drift length $L_{\rm d}$ of 13.0 μm the doping concentration of the n-column can be raised up to 6.0 $\times$ 10^{15} cm^{-3}. As shown in Figure 2, the current of the proposed structure flows through the n-column. The figure shows clearly that only the n-column contributes to the current conduction.

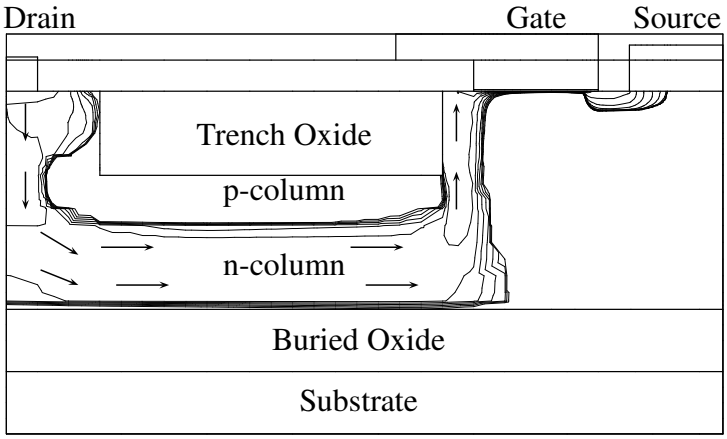

Figure 2. Current distribution of a SJ SOI-LDMOSFET with a trench oxide at $V_{\rm GS} = 15$V and $V_{\rm DS} = 20$ V. The p-column below the trench oxide does not contribute to the current conduction. The arrows show the current flow in the drift region.

SIMULATION RESULTS

$R_{\rm sp}$ and the BV of high-voltage SOI-LDMOSFETs strongly depend on the doping and the length of the drift layer. The drift doping of conventional SOI-LDMOSFETs is restricted by the RESURF (Reduced Surface Field) effect [10]. To increase the BV the drift length must be increased and the doping decreased. This results in an increase in the on-resistance. With the SJ structure it is possible to increase the doping concentration of the drift layer drastically, and $R_{\rm sp}$ can be reduced effectively. The on-resistance of the SJ devices has a linear volatge dependence instead of the square-law dependence of standard power MOSFETs [11]. The BV of the SJ depends on the critical electric field $E_{\rm c}$ of the device and the length of the n and p-columns. With the SJ concept the n-column charge

$Q_{\rm n}$, the p-column charge $Q_{\rm p}$, and the charge $Q_{\rm db}$ of the p body depletion region should be balanced in this structure. Assuming that all columns are completely depleted before breakdown, the charges and BV are given by [8]

$$Q_{\rm n} = Q_{\rm p} + Q_{\rm db} < 2\frac{\varepsilon_s E_{\rm c}}{q} \tag{1}$$

$$Q_{\rm n} = N_{\rm D}\, W_{\rm N};\;\; Q_{\rm p} = N_{\rm A}\, W_{\rm P} \tag{2}$$

$$\mathrm{BV} = E_{\rm c}\, t_{\rm N,P} \tag{3}$$

where $t_{\rm N,P}$ is the length of the n and p-columns, respectively. From (3) follows that the BV depends both on the critical electric field $E_{\rm c}$ and the column length. To reduce the column length of the SJ SOI-LDMOSFET a trench oxide is proposed in this study.

Figure 3 shows the comparison of the BV of conventional SOI-LDMOSFETs which have an n-drift length $L_{\rm d} = 20.0$ μm and 13.0 μm, respectively, and the SJ SOI-LDMOSFET with a trench oxide and $L_{\rm d} = 13.0$ μm. As shown in the figure the BV of the conventional devices strongly depends on the drift length. The conventional SOI-LDMOSFET with $t_{\rm soi}$ = 7.0 μm and $t_{\rm ox} = 2.0$ μm has a BV of 300 V (the solid line) at $L_{\rm d} = 20.0$ μm and $N_{\rm D}$ = 2.3 $\times$ 10^{15} cm^{-3}. If the n-drift length is reduced to 13.0 μm in this structure, a BV of 245 V (the dotted line) is obtained at $N_{\rm D} = 3.5 \times 10^{15}$ cm^{-3}. The dashed line in the figure shows the BV of the SJ SOI-LDMOSFET with trench oxide. Because of the increased surface path of the device, the BV increases with the trench oxide in the drift region. A BV of 300 V is obtained with $L_{\rm d} = 13.0$ μm in this structure. Note that this is the same BV as that of the conventional SOI-LDMOSFET with $L_{\rm d} = 20.0$ μm.

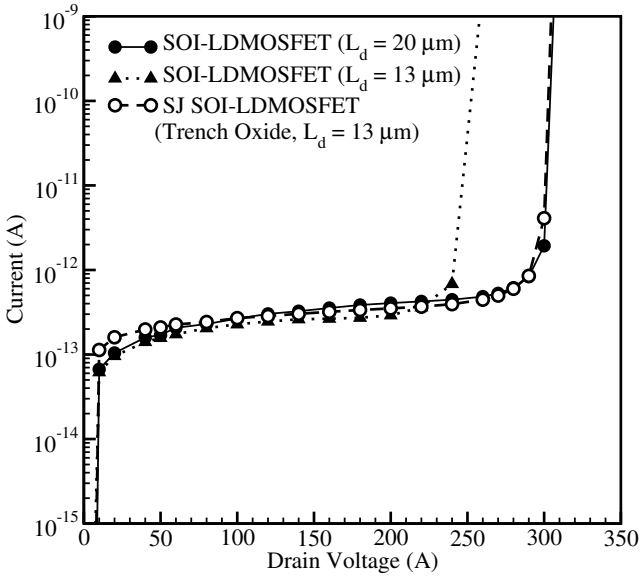

Figure 3. Comparison of the BV of the conventional SOI-LDMOSFETs ($L_{\rm d} = 20.0$ μm and 13.0 μm) and the SJ SOI-LDMOSFET with trench oxide ($L_{\rm d} = 13.0$ μm). $N_{\rm D}$ of conventional devices are 2.3 $\times$ 10^{15} cm^{-3} (at $L_{\rm d} = 20.0$ μm) and 3.5 $\times$ 10^{15} cm^{-3} (at $L_{\rm d}$ = 13.0 μm), respectively, and 6.0 $\times$ 10^{15} cm^{-3} of the SJ SOI-LDMOSFET.

Figure 4 shows the potential distribution of the fully resurfed SJ SOI-LDMOSFET which has a trench oxide and $L_{\rm d} = 13.0$ μm. Because of the increased surface path to the vertical direction in the drift region, we can see potential lines at the side wall of the trench oxide. These potential lines help to increase BV to the maximum value of the conventional SOI-LDMOSFET which has $L_{\rm d} = 20.0$ μm.

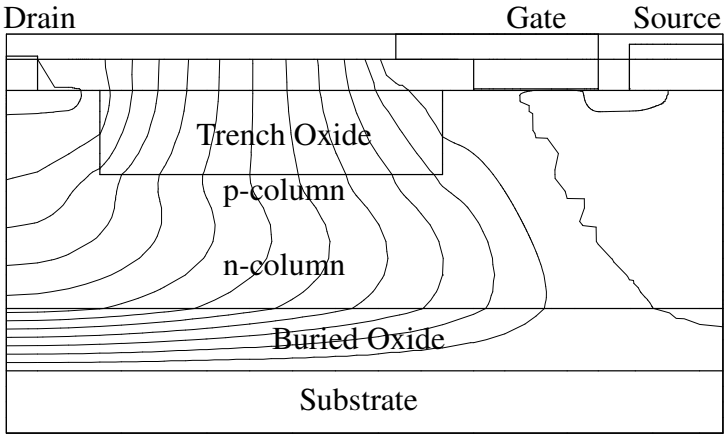

Figure 4. Potential distribution of a SJ SOI-LDMOSFET which has a trench oxide in the drift region at $V_{\rm DS} = 300$ V.

Figure 5 shows the electric field distribution of the suggested device at $V_{\rm DS}$ = 300 V, higher electric field can be observed at the trench oxide edges. From this figure we can see clearly several peaks of the electric field. The SJ SOI-LDMOSFET with a trench oxide has an additional peak in the middle of the SOI below the gate. Figure 6 shows a comparison of the electric field strength at the top surface between the conventional SOI-LDMOSFETs with $L_{\rm d} = 20.0$ μm and 13.0 μm. Conventional SOI-LDMOSFETs have the peak electric field at the drain, the field plate, and the gate edge near the top surface of the silicon.

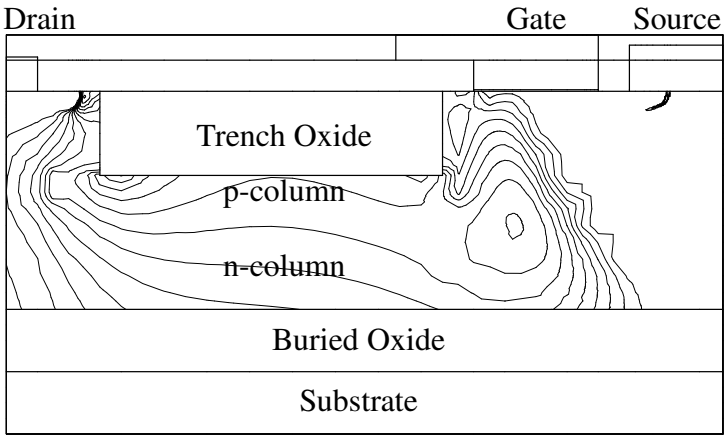

Figure 5. Electric field distribution of a SJ SOI-LDMOSFET which has a trench oxide in the drift region at $V_{\rm DS} = 300$ V.

Figure 7 shows a comparison of the electric field strength at the bottom of the trench oxide between the SOI-LDMOSFET and the SJ SOI-LDMOSFET. $L_{\rm d}$ of both structures is 13.0 μm. At the n-drift and p-body junction both devices show similar trends as that of the conventional device, but the abrupt peak can be seen at the trench oxide edge. Generally, in the middle of the device (along the lateral direction of the device) the conventional SOI-LDMOSFET has a broad range of higher electric field near the n-drift and p-body junction, and no abrupt peak can be found. The SJ SOI-LDMOSFET with a trench oxide with $L_{\rm d}$ = 13.0 μm and $N_{\rm D} = 6.0 \times 10^{15}$ cm^{-3}, the optimum electric field strength distribution is obtained with $N_{\rm A}$ of 1.5 $\times$ 10^{16} cm^{-3} (with $W_{\rm P} = 0.8$ μm).

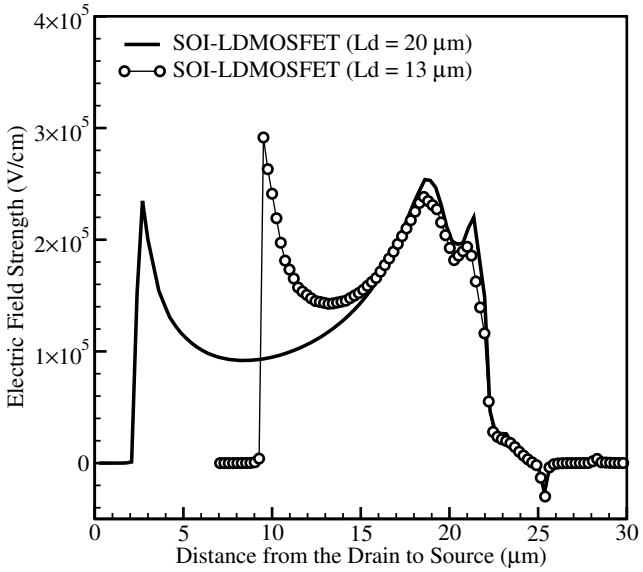

Figure 6. Comparison of the electric field strength at the top surface between the conventional SOI-LDMOSFETs with $L_{\rm d} = 20.0$ μm and 13.0 μm, respectively.

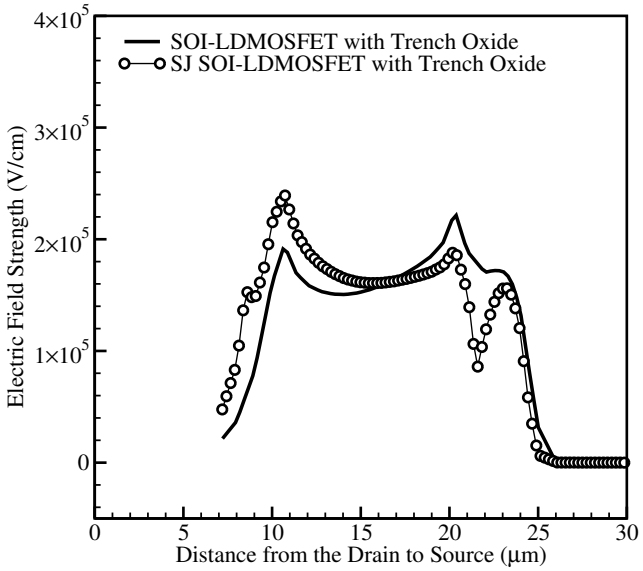

Figure 7. Comparison of the electric field strength at the bottom of the trench oxide between the SOI-LDMOSFET and the SJ SOI-LDMOSFET. Both structures have a trench oxide in the drift region with $L_{\rm d} = 13.0$ μm.

The solid line of Figure 8 shows the BV versus n-drift doping of the conventional SOI-LDMOSFET with an optimum $L_{\rm d} = 20.0$ μm. To achieve the best trade-off between $R_{\rm sp}$ and the BV, a higher drift doping with optimum $L_{\rm d}$ is essential. From the figure we can see the optimum n-drift doping is 2.3×10^{15} cm^{-3}. If the n-drift doping is reduced below the optimum value, the maximum electric field is moved towards the drain edge. If it exceeds the optimum value, a high electric field is moved towards the gate edge. Both cases cause lower BV. $R_{\rm sp}$ can be lowered with a reduced $L_{\rm d}$. Which shrinks the surface path of the depletion region at the breakdown. The dotted line of the figure shows the BV of the conventional SOI-LDMOSFET with $L_{\rm d} = 13.0$ μm, where a maximum BV of 245 V is obtained at $N_{\rm D} = 2.0 \times 10^{15}$ cm^{-3}. With the trench oxide in the drift region it is possible to increase the surface path of the depletion region and $L_{\rm d}$ can be reduced drastically without degrading BV. The dashed line shows the BV of the SOI-LDMOSFET which has a trench oxide in the drift region and a maximum BV of 300 V is obtained at $L_{\rm d} = 13.0$ μm. Because the reduced n-drift area by the trench oxide affects the charge balance condition, the optimum doping $N_{\rm D}$ is slightly increased compared to the conventional device.

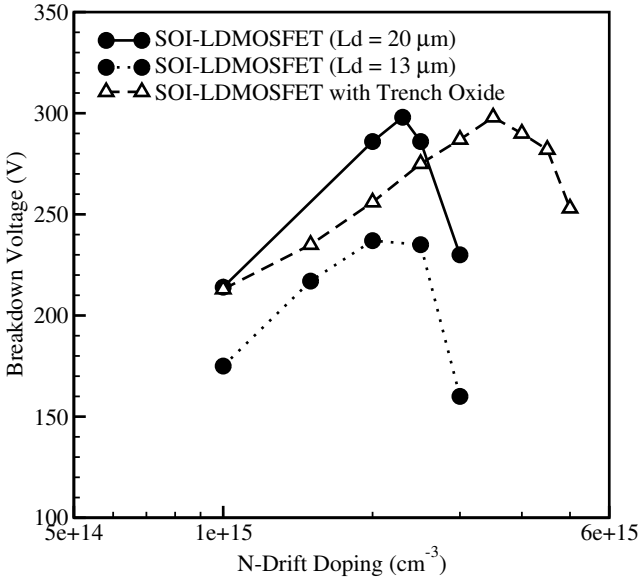

Figure 8. BV versus n-drift doping of the conventional SOI-LDMOSFETs and SOI-LDMOSFET with trench oxide (trench depth $= 2.7$ μm and $L_{\rm d} = 13.0$ μm).

The reduced conduction area by the trench oxide increases the $R_{\rm sp}$ of the device. To solve this problem we propose the SJ SOI-LDMOSFET by introducing the buried p-column in the n-drift region together with a trench oxide. With this structure $R_{\rm sp}$ can be lowered effectively. Figure 9 shows the BV versus p-column doping of the proposed devices with various trench depths. $L_{\rm d}$ and $N_{\rm D}$ are fixed to 13.0 μm and 6.0×10^{15} cm^{-3}, respectively. The trench depth determines the length of the surface path of the device. If it is below 2.5 μm (solid and dot-dashed lines) the BV is lower than that of conventional devices. With the trench depth over 2.7 μm the same BV is reached as the maximum value of conventional SOI-LDMOSFETs.

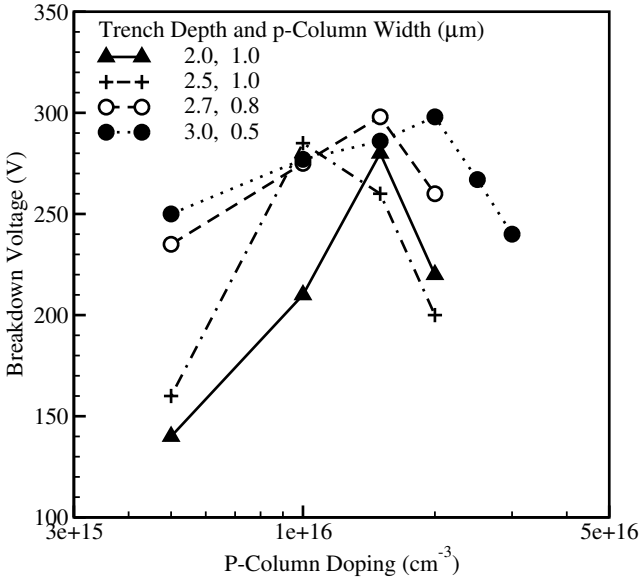

Figure 9. BV versus p-column doping of the SJ SOI-LDMOSFETs with trench oxide which have $L_{\rm d} = 13.0$ μm and $N_{\rm D} = 6.0 \times 10^{15}$ cm^{-3}.

To obtain the maximum BV, $Q_{\rm n}$, $Q_{\rm p}$, and $Q_{\rm db}$ in the SJ SOI-LDMOSFET should be balanced for complete depletion of the drift region at breakdown. If the p-column width is larger, the doping of this layer should be reduced to fulfill the charge balance. To make it larger the conduction area it is also important to minimize the p-column width. Figure 10 shows the p-column doping and $R_{\rm sp}$ versus p-column width of the proposed SJ SOI-LDMOSFET which has a trench oxide. The p-column doping concentration at each point in the figure is optimized to have the maximum BV of 300 V. Other device parameters such as the trench oxide depth, the drift length $L_{\rm d}$, and the n-column doping $N_{\rm D}$ are 2.7 μm, 13.0 μm, and 6.0 $\times$ 10^{15} cm^{-3}, respectively. The doping of the p-column is reduced with the increased p-column width .

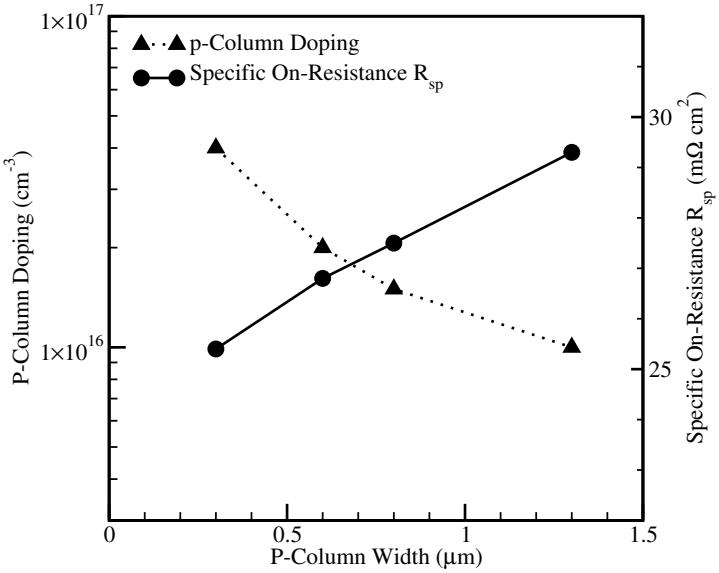

Figure 10. p-column doping and $R_{\rm sp}$ versus p-column width of the SJ SOI-LDMOSFET which has a trench oxide.

Equation (3) shows this relationship, and the dotted line of the figure clearly denotes this dependence. With $W_{\rm P}$ 0.3 and 1.3 μm, the optimum $N_{\rm A}$ is 4.0 and 1.0 $\times$ 10^{15} cm^{-3}, respectively. $Q_{\rm p} = N_{\rm A} \times W_{\rm P}$ of both cases remains approximately constant. The solid line shows the relationship between $W_{\rm P}$ and $R_{\rm sp}$. With reduced p-column width $R_{\rm sp}$ of the proposed device is improved by the increased conduction area. With lower $W_{\rm P}$ of 0.3 μm it is possible to achieve the minimum $R_{\rm sp}$ of 25.4 mΩ cm^2. If $W_{\rm P}$ of the structure is increased to 1.3 μm, $R_{\rm sp}$ is increased to 29.3 mΩ cm^2.

Table 1. DC performance comparison between the conventional SOI-LDMOSFET and the proposed device.

	Conventional SOI-LDMOSFET	SJ SOI-LDMOSFET with a trench oxide
$N_{\rm D}$, cm^{-3}	2.3 $\times$ 10^{15}	6.0 $\times$ 10^{15}
$L_{\rm d}$, μm	20.0	13.0
$R_{\rm sp}$, mΩ cm^2	33.4	25.4
BV, V	300	300

Table 1 shows a DC performance comparison of the simulation results between the conventional SOI-LDMOSFET and the proposed SJ SOI-LDMOSFET which has a trench oxide in the drift region. For the proposed device with an n column doping $N_{\rm D}$ of 6.0 $\times$ 10^{15} cm^{-3} and a drift length $L_{\rm d}$ of 13.0 μm, a maximum BV of 300 V is obtained at the p-column doping $N_{\rm A}$ = 4.0 $\times$ 10^{16} cm^{-3} and the p-column width $W_{\rm P}$ = 0.3 μm. These results demonstrate that the drift length can be reduced with a trench oxide in the drift region. The on-state characteristics depend on the p-column width and the drift doping. The $R_{\rm sp}$ of the proposed device is 25.4 mΩ cm^2. It is about 76% of the corresponding $R_{\rm sp}$ of the conventional 300 V SOI-LDMOSFET. Even the width of the drift region is reduced by the p-column and $R_{\rm sp}$ is lower than that of the conventional device by the reduced $L_{\rm d}$ and the increased $N_{\rm D}$ of the proposed device.

CONCLUSION

A high-voltage SJ SOI-LDMOSFET transistor with a trench oxide in the drift region is proposed. A lower $R_{\rm sp}$ is obtained in the proposed device. The $R_{\rm sp}$ of the proposed device which has a drift length $L_{\rm d}$ = 13.0 μm, a p-column doping $N_{\rm A}$ = 4.0 $\times$ 10^{16} cm^{-3} and a p-column width $W_{\rm P}$ = 0.3 μm is 25.4 mΩ cm^2. Even $L_{\rm d}$ is reduced to 13.0 μm, the BV is the same as that of the conventional SOI-LDMOSFET which has $L_{\rm d}$ = 20.0 μm. Our simulations confirm that the $R_{\rm sp}$ of the proposed device is about 76% and the n-drift length is about 65% of that of conventional SOI-LDMOSFETs, respectively. With this new device concept it is possible to reduce the device size and $R_{\rm sp}$ without degrading the BV.

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