

Lateral Trench Gate Super-Junction SOI-LDMOSFETs with Low On-Resistance

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Abstract

This paper describes low on-resistance lateral trench gate super-junction LDMOSFETs on SOI. The specific on-resistance (R_{sp}) of the SOI-LDMOSFETs is effectively improved by the super-junction concept together with the lateral trench gate. The super-junction helps to increase the doping concentration of the n-drift layer, and the lateral trench gate allow to increase the channel area. It can be achieved to reduce the on-resistance both of the n-drift and channel regions, respectively. Using the three-dimensional numerical simulator MINIMOS-NT, we confirm that the R_{sp} of the proposed lateral trench gate super-junction SOI-LDMOSFETs is about 60% of conventional SOI-LDMOSFETs. With the larger n column width than that of the p column the doping in the drift region can be reduced to 70% of the value of standard super-junction devices without degrading the on-resistance. As a result the sensitivity of the breakdown voltage to the charge imbalance can be improved in the proposed device.

1. Introduction

Lateral double diffused MOS transistors (LDMOSFETs) on SOI (Silicon on Insulator) are widely used as smart power devices in automotive and consumer applications. Reducing the on-resistance while maintaining a desired breakdown voltage rating has been the main issue in the development of these devices. The on-resistance of the medium and high-voltage SOI-LDMOSFETs strongly depends on the doping of the drift layer. Conventionally the drift layer doping concentration of the SOI-LDMOSFETs is restricted by the RESURF (Reduced Surface Field) effect [1]. In order to increase the breakdown voltage of the RESURF devices the doping of the drift layer must be reduced and the drift layer length increased. Recently, new concepts such as super-junction [2] and lateral trench gate [3] are proposed to improve the specific on-resistance (R_{sp}) of MOSFETs. Most of the super-junction devices such as COOLMOS [4] and MDmesh [5] assume complete charge balance. It can be achieved by introducing alternating n and p columns in the drift region, and the doping in this region can be increased drastically. It has the inverse relationship with the width of the n and

p columns [2]. Even the current conduction area is reduced by additional p columns which do not contribute towards on-state conduction. This results in significant reduction in the specific on-resistance (R_{sp}) of the devices. This paper presents for the first time a lateral trench gate super-junction SOI-LDMOSFETs to obtain the low on-resistance. Contrary to the conventional vertical trench MOSFETs, the gate is formed laterally on the side wall of a trench and the channel current flows to the lateral direction through the trench side walls. This allows increasing the channel area, and it decreases the on-state resistance of the devices. To increase the on-state conduction area in the drift region an unbalanced structure is examined where the width of the n column is larger than that of the p column. Three-dimensional numerical simulations with MINIMOS-NT [6] have been performed to investigate the influence of device parameters on R_{sp} , breakdown voltage, and the sensitivity of the charge imbalance.

2. Device Structures and Operation

Fig. 1 and Fig. 2 show the schematic structures of a standard super-junction (SJ) LDMOSFET on SOI and a proposed lateral trench gate SJ SOI-LDMOSFET which are used for simulation of breakdown voltage and on-resistance, respectively. As shown in Fig. 1, the standard SJ SOI-LDMOSFETs can be made by introducing extra p columns in the drift region. It is assumed that the charge in the n and p column of the drift layer should be exactly balanced, and this is true only when the drift length of the device is large enough to ignore the effect of the charge in the p body. The breakdown voltage (BV) is limited by the buried oxide thickness and drift layer length. It is designed to achieve the BV of 120 V with an SOI thickness t_{soi} of 1.0 μm , and with a buried oxide thickness t_{ox} of 1.0 μm . With the same n and p column width (W_N and W_P) of 0.5 μm and the drift layer length of 6.0 μm the doping concentration of the n column N_D can be raised up to $9.9 \times 10^{16} \text{ cm}^{-3}$. The extra p column is doped to achieve a balanced charge condition which means that the net depletion layer charge is zero.

As shown in Fig. 2, the proposed lateral trench gate SJ SOI-LDMOSFET has a similar structure as that of a standard SJ SOI-LDMOSFET (see Fig. 1) except that it

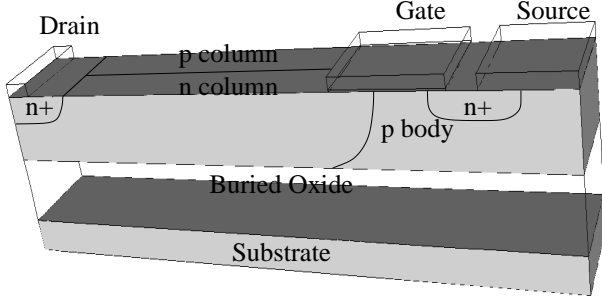


Figure 1. SJ LDMOSFET on SOI.

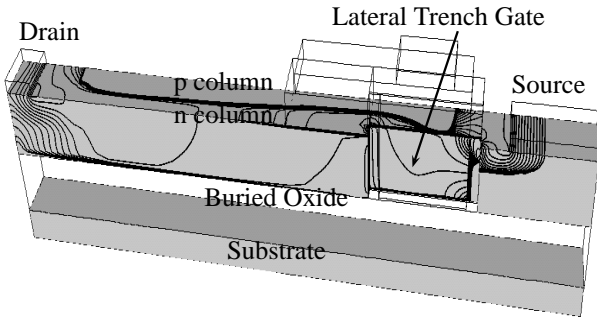


Figure 2. Proposed 120 V lateral trench gate SJ SOI-LDMOSFET and current flow iso-lines at $V_{GS} = 12$ V and $V_{DS} = 10$ V.

has a trench gate on the side wall. Together with the channel on the top of the SOI this allows obtaining an increased channel area compared to that of conventional SOI-LDMOSFETs. From Fig. 2 it is clear that only the n column of the drift region contributes to the current conduction in the on-state, and the channel current flowing on the side wall of the trench can be seen. With the increased channel area the reduction of the channel resistance can be achieved. The unbalanced structure which has larger W_N than W_P is proposed to examine the effects on the on-resistance and the sensitivity of the BV to the charge imbalance. Because of the increased n column width W_N from $0.5 \mu\text{m}$ (in the case of SJ SOI-LDMOSFET in Fig. 1) to $1.0 \mu\text{m}$ the doping of this region is reduced to $6.0 \times 10^{16} \text{ cm}^{-3}$ by the SJ concepts [2]. The width, space, and depth of the lateral trench gate are $0.4 \mu\text{m}$, $1.1 \mu\text{m}$ and $1.0 \mu\text{m}$, respectively. Simulations are performed for the 120 V lateral trench gate SJ SOI-LDMOSFETs with an n column width $W_N = 2 \times W_P$ of $1.0 \mu\text{m}$ and doping N_D of $6.0 \times 10^{16} \text{ cm}^{-3}$. The other structure parameters are the same as that in the Fig. 1.

3. Simulation Results and Discussion

In the standard vertical SJ devices the doping of the n and p column of the drift region must be balanced exactly. Most of the previous works assume that the charge of the n column Q_n is equal to that of the p column Q_p . The BV depends on the critical electric field E_c of the

device and the length of the n and p columns. In the SOI-LDMOSFETs a large portion of the voltage is supported by the buried oxide layer and the charge of the p body affects the RESURF condition significantly. Unlike in conventional RESURF devices, three-dimensional RESURF phenomena can be seen in this structure. Q_n , Q_p , and the charge Q_{db} of the p body depletion region should be balanced. Assuming that all columns are completely depleted before breakdown, the charges and BV are given by

$$Q_n = Q_p + Q_{db} < 2 \frac{\epsilon_s E_c}{q} \quad (1)$$

$$Q_n = N_D W_N; Q_p = N_A W_P \quad (2)$$

$$BV = E_c t_{N,P} \quad (3)$$

where $t_{N,P}$ is the length of the n and p columns, respectively. The BV depends both on the critical electric field E_c and the column length.

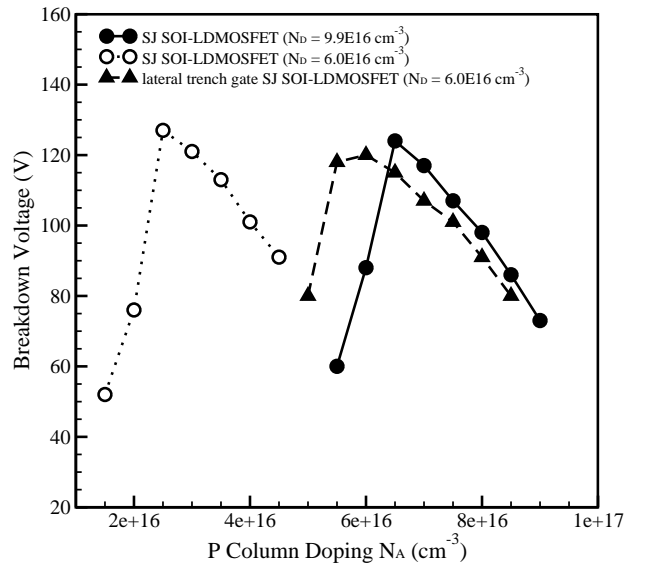


Figure 3. P column doping N_A dependence on the BV of the SJ SOI-LDMOSFETs and lateral trench gate SJ SOI-LDMOSFET.

Fig. 3 shows the p column doping N_A dependence on the BV of the SJ SOI-LDMOSFETs. In contrast to previous results [2, 8] the doping of the p column is lower than that of the n column. For the SJ SOI-LDMOSFET with an n column doping N_D of $9.9 \times 10^{16} \text{ cm}^{-3}$, a maximum BV of 124 V is obtained at $N_A = 6.5 \times 10^{16} \text{ cm}^{-3}$. With the N_D of $6.0 \times 10^{16} \text{ cm}^{-3}$, a maximum BV of 127 V is obtained at $N_A = 2.5 \times 10^{16} \text{ cm}^{-3}$. These results demonstrate that the charge of the p body strongly affects the charge balance condition of the SJ SOI-LDMOSFETs. Fig. 4 shows the N_A dependence on the electric field strength near the surface of the device along the n and p column junction. At the gate edge a high electric field can be seen with a low N_A of $5.5 \times 10^{16} \text{ cm}^{-3}$, and if the N_A is increased to the value of $9.0 \times 10^{16} \text{ cm}^{-3}$, a high electric field is moved toward the drain edge. The optimum

electric field strength distribution is obtained with the N_A of $7.0 \times 10^{16} \text{ cm}^{-3}$. It proves that the optimum RESURF condition can be obtained with N_A much lower than N_D .

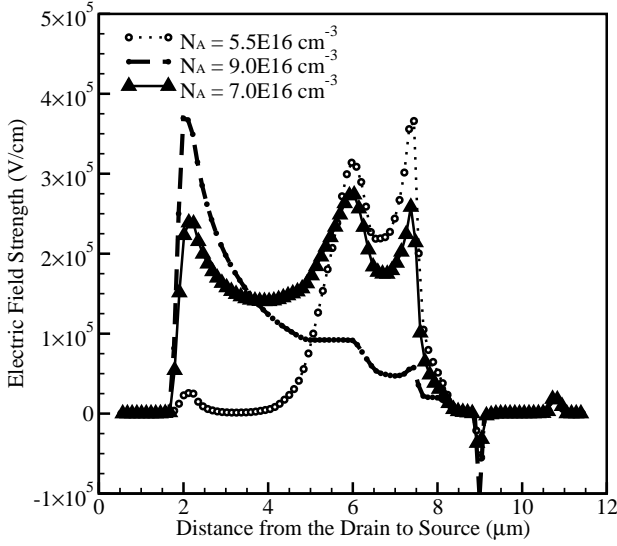


Figure 4. Comparison of the electric field strength in SJ SOI-LDMOSFET for different values of N_A at the BV (along the n and p column junction in Fig. 1).

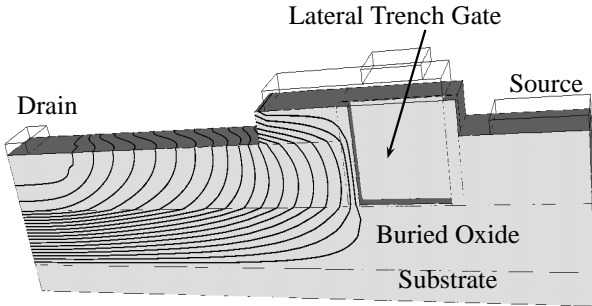


Figure 5. Potential distribution of a lateral trench gate SJ SOI-LDMOSFET at the V_{DS} of 120 V.

Similar result can be seen for the lateral trench gate SJ SOI-LDMOSFET (dashed line in Fig. 3). With the n column doping N_D of $6.0 \times 10^{16} \text{ cm}^{-3}$ and the width $W_N = 2 \times W_P$ of $1.0 \mu\text{m}$, the maximum breakdown voltage is 120 V at $N_A = 6.0 \times 10^{16} \text{ cm}^{-3}$. Even with the 2 times larger n column width than that of the p column the optimum doping N_A is the same as N_D in this case. Fig. 5 shows the almost uniformly distributed potential lines of the lateral trench gate SJ SOI-LDMOSFET at the drain voltage V_{DS} of 120 V. One can clearly see that most of the potential is supported by the buried oxide layer. Curved potential lines at the top surface of the device by the lateral depletion along the n and p column junction are also visible. The BV of the SJ devices strongly depends on the charge balance condition. As has been shown in Fig. 3, the BV decreases abruptly with decreasing N_A . In practical manufacturing it is difficult to achieve perfect charge

balance. Generally it is assumed that the doping could be controlled within $\pm 10\%$ of the nominal charge [7]. Fig. 6 shows the effect of sensitivity of the charge imbalance on the BV. By proper choice of the p column doping N_A (near the value of the maximum breakdown region in Fig. 3) the relations between BV and charge imbalance can be seen clearly. In this figure N_A of $7.0 \times 10^{16} \text{ cm}^{-3}$ (SJ SOI-LDMOSFET with N_D of $9.9 \times 10^{16} \text{ cm}^{-3}$), $3.0 \times 10^{16} \text{ cm}^{-3}$ (SJ SOI-LDMOSFET with N_D of $6.0 \times 10^{16} \text{ cm}^{-3}$), and $6.0 \times 10^{16} \text{ cm}^{-3}$ (lateral trench gate SJ SOI-LDMOSFET with N_D of $6.0 \times 10^{16} \text{ cm}^{-3}$) are used as reference values, respectively.

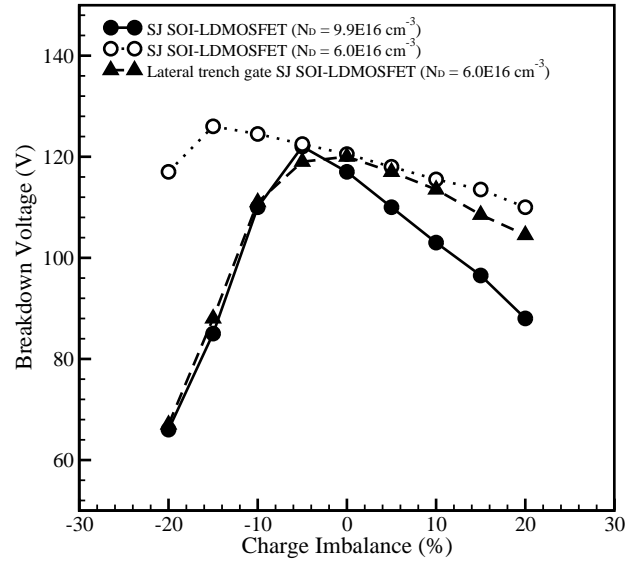


Figure 6. Sensitivity of the BV to the charge imbalance (as a function of N_A) for the different values of N_D . Reference N_A : $7.0 \times 10^{16} \text{ cm}^{-3}$ (SJ SOI-LDMOSFET with N_D of $9.9 \times 10^{16} \text{ cm}^{-3}$), $3.0 \times 10^{16} \text{ cm}^{-3}$ (SJ SOI-LDMOSFET with N_D of $6.0 \times 10^{16} \text{ cm}^{-3}$), and $6.0 \times 10^{16} \text{ cm}^{-3}$ (lateral trench gate SJ SOI-LDMOSFET with N_D of $6.0 \times 10^{16} \text{ cm}^{-3}$).

As shown in Fig. 6, this sensitivity (slope of the line) is reduced if the doping of the drift region is low. One can see the drastically reduced sensitivity in the SJ SOI-LDMOSFET with the $N_D = 6.0 \times 10^{16} \text{ cm}^{-3}$ (dotted line). The reduced BV (110 V) with the N_A change from -20% to $+20\%$ is over 90% of the reference value (120 V at zero charge imbalance). However this results in an increasing on-resistance. This problem can be solved by increasing the n column width together with the lateral trench gate. Then it is possible to lower the doping of the drift region without degrading the on-resistance. The reduced BV (104 V) of the lateral trench gate SJ SOI-LDMOSFET with the N_A change from 0% to $+20\%$ is about 87% of the reference value (120 V). Compared to the BV reduction (88 V) of the standard SJ SOI-LDMOSFET with the $N_D = 9.9 \times 10^{16} \text{ cm}^{-3}$, the sensitivity of the BV to the charge imbalance is reduced in the proposed structure.

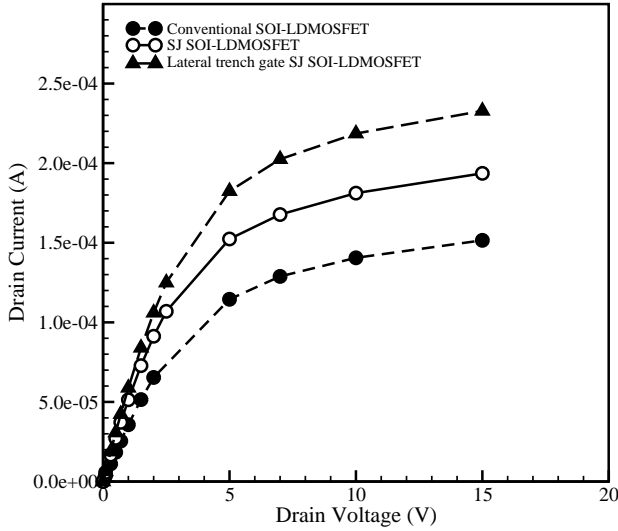


Figure 7. On-state characteristics of a conventional SOI-LDMOSFET, a SJ, and a lateral trench gate SJ SOI-LDMOSFET at the $V_{GS} = 12$ V.

Table 1. DC performance comparison between 120 V SJ and lateral trench gate SJ SOI-LDMOSFETs.

| | SJ LDMOSFET on SOI | Lateral trench gate SJ SOI-LDMOSFET |
|--------------------------------------|----------------------|-------------------------------------|
| N_D, cm^{-3} | 9.9×10^{16} | 6.0×10^{16} |
| N_A, cm^{-3} | 7.0×10^{16} | 6.0×10^{16} |
| $R_{sp}, \text{m}\Omega \text{cm}^2$ | 2.03 | 1.79 |
| BV, V | 117 | 120 |

Fig. 7 and Table.1 show the results of the on-state characteristics of a conventional, a SJ and a lateral trench gate SJ SOI-LDMOSFET. From this figure it is clear that the lateral trench gate SJ SOI-LDMOSFET has superior current handling capability compared to others. The R_{sp} of this device is $1.79 \text{ m}\Omega \text{cm}^2$ at $V_{GS} = 12$ V and $V_{DS} = 0.5$ V. It is about 60% of the corresponding R_{sp} value of conventional 120 V SOI-LDMOSFET (about $3.0 \text{ m}\Omega \text{cm}^2$). Even the doping of the drift region is reduced by increasing the width of n column, R_{sp} is lower than that of the SJ SOI-LDMOSFET with a much higher n column doping up to $9.9 \times 10^{16} \text{ cm}^{-3}$.

4. Conclusions

A lateral trench gate SJ SOI-LDMOSFET transistor is proposed. A lower specific on-resistance is obtained in the suggested structure. Our simulations confirm that the R_{sp} of the lateral trench gate SJ SOI-LDMOSFETs is about 60% lower than that of conventional SOI-LDMOSFETs. This value is lower than that of a SJ SOI-LDMOSFET which has a much higher n column doping of $9.9 \times 10^{16} \text{ cm}^{-3}$. Unlike the standard vertical SJ devices, the optimum p column doping of the SJ SOI-LDMOSFETs

is lower than that of the n column. For the SJ SOI-LDMOSFET with an n column doping N_D of $9.9 \times 10^{16} \text{ cm}^{-3}$, a maximum BV of 124 V is obtained at $N_A = 6.5 \times 10^{16} \text{ cm}^{-3}$. With N_D of $6.0 \times 10^{16} \text{ cm}^{-3}$, a maximum BV of 127 V is obtained at $N_A = 2.5 \times 10^{16} \text{ cm}^{-3}$. Similar result can be seen with the lateral trench gate SJ SOI-LDMOSFET. Together with the larger width of the n column than that of the p column in the drift region it is possible to lower the doping of the n column without degrading the on-resistance. As a result the sensitivity of the BV to the charge imbalance is reduced compared to that of the standard SJ SOI-LDMOSFET.

- [1] J.A. Appels, and H.M.J. Vaes, "HV thin layer devices (RESURF devices)", *Proc. of Intl. Electron Devices Meeting (IEDM), Technical Digest*, 1979, pp. 238-241.
- [2] T. Fujihira, and Y. Miyasaka, "Simulated Superior Performances of Semiconductor Superjunction Devices", *Proc. of 10th Intl. Symp. Power Semiconductor Devices & ICs (ISPSD)*, 1998, pp. 423-426.
- [3] Y. Kawaguchi, T. Sano, and A. Nakagawa, "20V and 8V Lateral Trench Gate Power MOSFETs with Record-Low On-resistance", *Proc. of Intl. Electron Devices Meeting (IEDM), Technical Digest*, 1999, pp. 197-200.
- [4] L. Lorenz, G. Deboy, A. Knapp, and M. März, "COOLMOSTM- a new milestone in high voltage Power MOS", *Proc. of 11th Intl. Symp. Power Semiconductor Devices & ICs (ISPSD)*, 1999, pp. 3-10.
- [5] M. Saggio, D. Fagone, and S. Musumeci, "MDmeshTM: innovative technology for high voltage PowerMOSFETs", *Proc. of 12th Intl. Symp. Power Semiconductor Devices & ICs (ISPSD)*, 2000, pp. 65-68.
- [6] Institute for Microelectronics, TU Wien, "MINIMOS-NT", 2001.
- [7] P.M. Shenoy, A. Bhalla, and G.M. Dolny, "Analysis of the Effect of Charge Imbalance on the Static and Dynamic Characteristics of the Super Junction MOSFET", *Proc. of 11th Intl. Symp. Power Semiconductor Devices & ICs (ISPSD)*, 1999, pp. 99-102.
- [8] S. Xu, K.P. Gan, G.S. Samudra, Y.C. Liang, and J.K.O. Sin, "120 V Interdigitated-Drain LDMOS (IDLDMOS) on SOI Substrate Breaking Power LDMOS Limit", *IEEE Trans. Electron Devices*, Vol. 47, No. 10, 2000, pp. 1980-1985.