# Three-Dimensional Analysis of Leakage Currents in III-V HBTs

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## Abstract

*We present fully three-dimensional simulation results for a real HBT structure as applied in MMICs. Investigation of the leakage is performed in attempt to explain device behavior in the complete voltage range. The paper gives a justification for the need of three-dimensional simulation and addresses critical development, modeling, and simulation issues.*

## INTRODUCTION

Heterojunction Bipolar Transistors (HBTs) are among the most advanced semiconductor devices today. Two-dimensional device simulation proved to be valuable for understanding the underlying device physics [1] and for investigating the device reliability [2]. Nevertheless, effects like leakage currents at low bias could not be explained. Three-dimensional simulation of such devices have not been reported so far, maybe due to the high length-to-width ratio of the emitter causing very high computational expense of such simulations. In this work we investigate the leakage currents in III-V HBTs by means of three-dimensional simulations.

## WHERE AND WHY DOES COLLECTOR-EMITTER LEAKAGE HAPPEN – A HYPOTHESIS

Conventional two-dimensional simulations of HBTs employ a cut in direction A-A (see Fig. 1). Thus, three-dimensional effects which typically occur at the edges of a real structure and typical non-homogeneous material in z-direction (cut B-B of Fig. 1) resulting in non-homogeneous electrical performance and operating temperature of the device are neglected.

Good agreement between two-dimensional simulation and measurement is achieved for medium and high bias [3], but not for low bias where high leakage currents exist ($\approx$nA). The base-emitter (BE) leakage current can be reproduced by including certain generation/recombination mechanisms [4]. However, the collector-emitter (CE) leakage current cannot be explained with two-dimensional analysis as there is no direct path between emitter and collector. Note, such a path exists only in the third dimension (see Region A in Fig. 1).

It is known from Silicon technology, that mechanical stress can occur at several steps in the manufacturing of ICs, for example, due to sharp corners of the shallow trench insulation or due to nitride deposition. In many cases, stress results in undesirable negative effects on device performance. Many authors investigated these effects for Si-based devices [5]-[7] and attributed the increased generation current to stress-induced bandgap narrowing. A locally varying stress-dependent bandgap model was implemented in MINIMOS-NT [8] and applied to III-V HBTs to allow with fully three-dimensional simulation the verification of the hypothesis.

## THREE-DIMENSIONAL DEVICE SIMULATION

During the past two decades several three-dimensional device simulators have been developed. Many of them have strong limitations (for details see the next section). Typical applications have been narrow channel effects in MOS devices or studies on leakage current in memory cells.

The demands on state-of-the-art device simulators are high and the development of a three-dimensional device simulator is a challenging task. MINIMOS-NT has been extended to a multi-dimensional device simulator to allow both two- and fully three-dimensional simulations. Moreover, for the controlling of such a complex simulator, a control system mandatory for state-of-the-art TCAD simulators has been developed and applied, and several investigations on three-dimensional effects have been performed.

MINIMOS-NT solves Poisson's equation, both carrier continuity equations, the carrier energy balance equation, and the lattice heat flux equation coupled and decoupled. Moreover, transient and AC-small signal analysis can be performed. Mixed-mode simulations allow to combine physical devices and compact models in a circuit.

The numeric module consists of a direct and two different iterative linear solvers where one iterative solver is applied on complex numbers which enhances AC-small signal analysis dramatically. For the solving process the user can choose among several iteration schemes to speed up the simulation and improve the convergence of the simulation.

Several grid types are supplied in MINIMOS-NT with number of grid nodes only limited by the memory of the computer. The simulated device structures can be of arbitrary shape and complexity.

MINIMOS-NT handles different III-V materials, such as GaAs, AlAs, InAs, InP, GaP, GaN, AlN, and InN, their ternary alloys, and non-ideal dielectrics. Various important physical effects, such as band gap narrowing, surface recombination, transient trap recombination, self-heating, and hot electron effects are taken into account. The models are based on experimental or Monte Carlo simulation data and employ analytical functional forms which cover the whole material composition range. Special attention is paid to bulk and heterointerface carrier transport. The model parameters are checked against several independent HEMT and HBT technologies to obtain one concise set used for all simulations. A model server allows user-defined physical models to be included.

## PROBLEMS AND DEMANDS ON THREE-DIMENSIONAL DEVICE SIMULATION

Three-dimensional device simulation is mandatory for investigations on real three-dimensional structures which cannot be described by two-dimensional cuts. Nevertheless, today more than 95% of all device simulations are two-dimensional ones. One reason for this is the lack of adequate and affordable simulation tools. Other issues are the handling of three-dimensional data and the high computational costs.

### Computational Effort

The computational effort of a numerical problem grows approximately linearly with the size of the problem which mainly depends on the complexity of the equation set to solve and the size of the grid (number of grid points). For a tensor-product grid with an equivalent number of grid points in every direction the number of points rises with the exponent of 3/2 when extending from two to three dimensions. This means, that a typical two-dimensional grid with 3.000 to 10.000 points leads to a three-dimensional grid using about 160.000 to 1.000.000 points for the same resolution, which causes a memory consumption far beyond the limits of the affordable computers today.

### Geometric Description

Compared to the generation of two-dimensional geometries the generation of three-dimensional ones is a much more complex task which requires a powerful tool with sophisticated user interface.

### Grids

Grid generation is a crucial factor in device simulation since the number of grid points directly affects memory consumption and the simulation time. Furthermore, the grid has a direct impact on the condition of the system matrix and therefore on the accuracy and also on the convergence of the numerical solution procedure.

The density of the grid must vary locally inside the device to meet the simulation requirements. The grid must be dense enough to keep the discretization error small and to describe properly the geometry of the device.

MINIMOS-NT uses the box integration method as discretization scheme. Therefore, the resulting grid has to meet the Delaunay Criterion and the criterion of the smallest sphere [9] at the boundary.

In three dimensions it is hardly possible and tedious to manually specify criteria for grid generation or the place of grid points. Therefore, an automatic tool is necessary.

### Numerics

The grid sizes rise dramatically in three dimensions. The discretization produces coupling between grid points where only neighboring points of a certain point are of interest – all connected by grid lines. Compared with the large matrix sizes this coupling is very small resulting in very sparsely filled equation systems.

Direct solvers cannot be used for three-dimensional simulations [10]. Iterative solvers used in device simulation are based on the conjugate gradient method (CG) [11] which strongly relies on good pre-conditioning algorithms which are responsible for the condition of the linear system and thus for the convergence of the solving process. As non-symmetric equation systems are solved in MINIMOS-NT, an improved version of the iterative solver Bi-CGSTAB [12] is used in combination with an ILU pre-conditioner, which is capable to calculate systems with complex numbers and is therefore also well suited for AC-small signal analysis.

### Visualization

For the visualization of three-dimensional data a four-dimensional space would be necessary. Therefore, such data can only be visualized on the surface of the device, by two-dimensional cuts through the device, or on discrete values on a specific grid. Several algorithms for presentation of data must be available, like iso-surfaces and iso-lines, cuts, multiple cuts or projections.

### Control System

State-of-the-art device simulator must be able to handle a huge amount of information of different kind and type and arbitrary hierarchically structured data. The user must have the possibility to modify this information in a simple and efficient way. To obtain a maximum of flexibility and a complete control of MINIMOS-NT, a specialized control system called Input Deck database has been developed. This includes, e.g., the control of the input and output files, the simulation modes, the iteration schemes, the physical models to use, the physical parameters, the material database, or circuit descriptions.

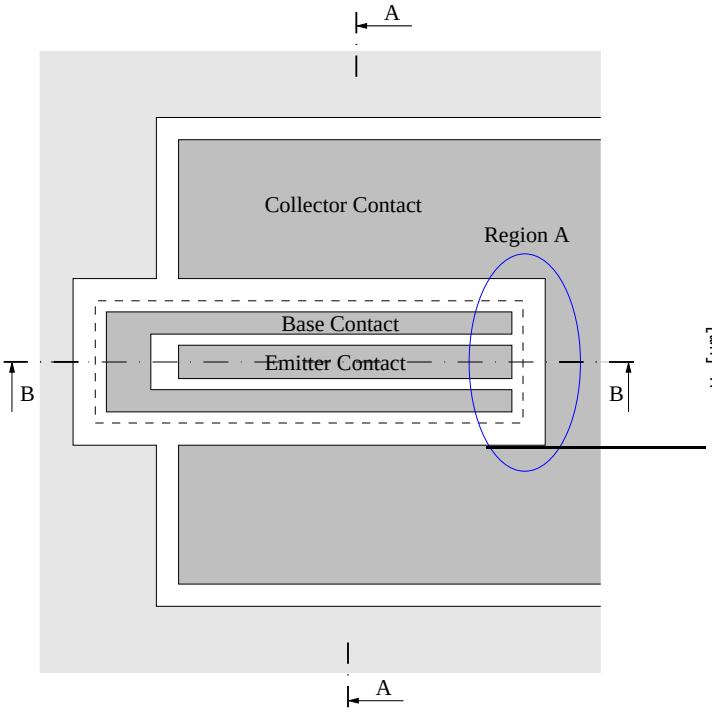


**Figure 1: Top view of a three-dimensional HBT.**

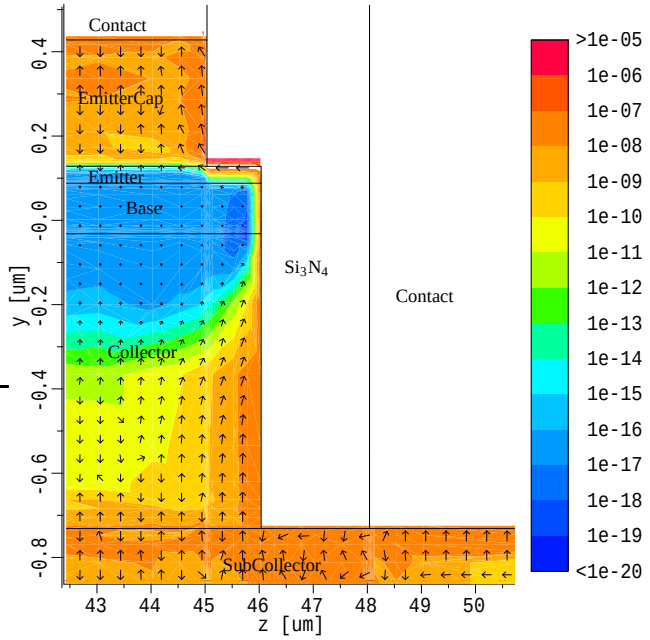


**Figure 2: Electron current density [A/cm$^2$] in Region A of the HBT using a cut in B-B direction.**

## SIMULATION EXAMPLE

As an example, by means of three-dimensional (3D) device simulation we studied the influence of process-induced stress and thermal/electrical aging on a one-finger InGaP/GaAs HBT with emitter area of 3 $\mu$m $\times$ 30 $\mu$m. Fig. 1 shows the top view of the device. We investigated the possibility of leakage in the third dimension. As a first step two-dimensional (2D) simulations of the cut B-B of Fig. 1 were performed. Special attention was paid on Region A where the emitter is not surrounded by the C-shaped base. This region was identified to be very sensitive to variations of the doping profile, surface charges and traps, and the simulation results proved that CE leakage can occur there.

So, while in A-A direction a reasonable base current can be achieved, the B-B direction enables investigation of the collector current. Fig. 2 shows a cut in B-B direction of the result of a 3D simulation at $V_{BE}$ = $V_{CE}$ = 0.5 V. Even for low voltages a high emitter current flows from the collector to the emitter without control by the base. Fig. 3 shows the potential distribution of Region A.

MINIMOS-NT was applied for both 3D and 2D simulations. For the shown device a grid with more than 150.000 points was used which requires about one hour of CPU time on a 1 GHz Pentium Linux computer for a given bias point.

## DISCUSSION

Fig. 4 shows measured, 2D-simulated, and fully 3D-simulated forward Gummel plots for a one finger GaAs HBT both before and after aging. It has been already shown in [1] that the electrical performance of the unstressed device in its active region (i.e. $V_{BE}$ >1.0 V) can be modeled with high accuracy by means of solely 2D-simulations. By incorporating surface charges on the InGaP-ledge the 2D-approach allows even to describe the high base leakage current (see Fig. 4 and [2]), which happens below $V_{BE}$ = 1.0 V and which is known to be the major degradation effect of HBTs. However, as can be taken from the 2D-result for the collector current of Fig. 4, $I_C$(2D), this approach does not give any collector leakage. This is in strong discrepancy to the measurement, which delivers collector leakage currents in the range of 10 nA.

Our hypothesis was to search for this leakage in the Region A (Fig. 1), which required fully 3D-simulation of the device. It turned out, as can be taken from the $I_C$(3D)-curve in Fig. 4, that now a considerable collector leakage in the order of nA is possible. This leakage is due to the surface current flowing from emitter contact to the collector contact as shown in Fig. 2.

However, the collector leakage current is still below the actually measured one. We currently assume the missing leakage current contribution in the non-ideal isolation of the pads. In our case they are located on the subcollector layer with no dielectric isolation in between. This technology is not able to give a perfect isolation.

To distinguish between the intrinsic leakage happening at the surface of the device, and the extrinsic one, occurring between the pads, one might consider, on one hand, incorporating also the pads into the 3D-simulation. But due to the huge dimension of the pads and their large distance to the device in comparison to the tiny active device geome-

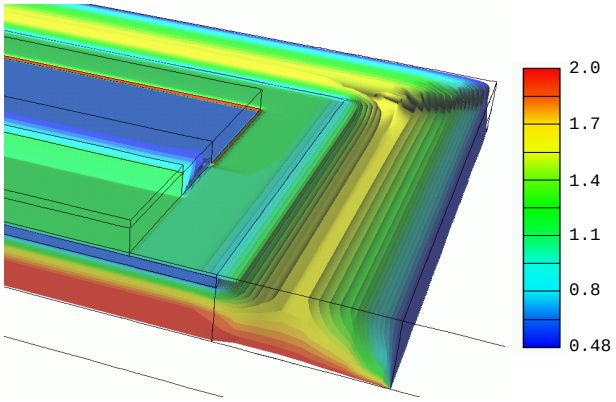


**Figure 3: Iso-surfaces of the potential [V] in Region A at $V_{BE}$ = $V_{CE}$ = 0.5 V.**

try this would lead to an unacceptable computational task. On the other hand, the straightforward experimental solution would be to measure the leakage of a so-called "open-test-structure". This test structure is quite well known for equivalent-circuit modeling purposes. This structure has an absolutely identical setup as the active transistor structure, but only the electrical contacts directly on the semiconductor material are missing. Such kind of a structure is typically used for extraction of parasitic capacitances [13]. Unfortunately, our available test-structure delivered a collector leakage, which was even larger than the one of the device. By further investigations we verified that this unexpected result was due to the fact that the open-test-structure had a somewhat different pad-environment compared to the active transistor structure. In conclusion, we are at present not able to exactly separate intrinsic and extrinsic leakage current contributions. On the other hand, the simulated intrinsic collector leakage current was definitely shown to be within the limits given by the current experimental uncertainties.

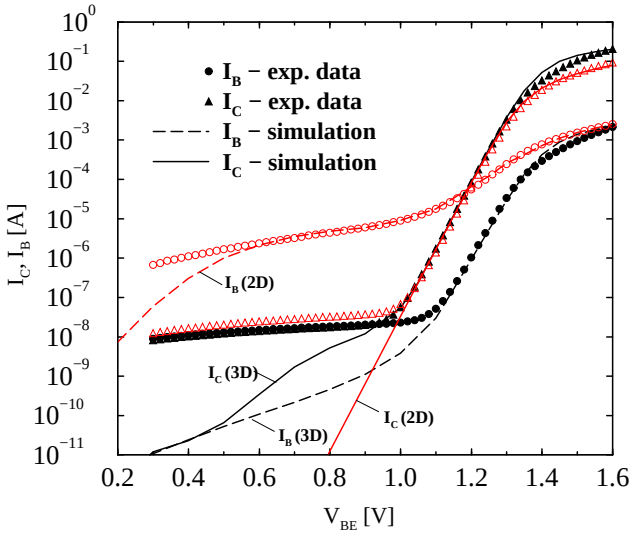


**Figure 4: Forward Gummel plots at $V_{CB}$ = 0 V: Comparison between measurements (symbols) and 3D- and 2D-simulations (lines) before (filled) and after (open) HBT aging.**

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