

MODELING AND SIMULATION OF SiC MOSFETs

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ABSTRACT

We perform a numerical simulation in order to get an insight into the physics and the behavior of silicon carbide MOSFETs. A new device structure for a lateral DMOSFET has been proposed. Material-specific models for surface-scattering, impact ionization, and incomplete ionization have been implemented into the device simulator MINIMOS-NT to investigate device characteristics. The key parameters that alter the device performance have been optimized. The relationship between blocking and driving capability was closely examined. Excellent I-V characteristics with significant improvement on the reduction of the gate bias voltage, and a fairly large advantage on electrical performance and device reliability were achieved.

KEY WORDS

SiC MOSFET; ACCUFET; Inversion layer mobility; Physically-based modeling; Simulation-based comparison.

1 Introduction

Silicon (Si) has long been the dominant semiconductor of choice for electronic device applications [1]. However, recently, wide bandgap semiconductors, particularly silicon carbide (SiC) has attracted much attention, because it offers tremendous benefits over other available semiconductor materials in a large number of industrial and military applications [2]. The physical and electronic properties of SiC make it the foremost semiconductor material for short wavelength optoelectronic, high temperature, radiation resistant, and high-power/high-frequency electronic devices [3].

SiC-based electronic devices can operate at extremely high temperatures without suffering from intrinsic conduction effects (20 orders lower than Si) because of the wide energy bandgap of 3 - 3.3 eV [4]. Devices formed in SiC can withstand an electric field of 10 times greater than Si without undergoing avalanche breakdown [5]. SiC is an excellent thermal conductor. Heat will flow more readily through SiC than other semiconductor materials. It has 3 times higher thermal conductivity than Si. SiC devices can operate at high frequencies (RF and microwave) because of the larger saturated electron drift velocity of 2 times compared to Si [6].

SiC is the only semiconductor material besides Si on which a thermal oxide can be grown, thus enabling MOS-based devices. Due to the lack of material development and design, most SiC MOSFETs suffer from surface problems such as step-bunching and non-uniform doping density [7]. This leads to poor inversion layer electron mobility and oxide reliability, which will degrade the on-state performance and the breakdown voltage. To minimize these problems accumulation-mode MOSFETs (ACCUFET) have been demonstrated recently for vertical DMOS transistors [8] which reveal the significant advantage of this type of structure.

We propose a new design of an accumulation-mode structure for a LDMOSFET (Lateral DMOSFET). The key parameters that alter the overall device performance have been optimized using the general-purpose device simulator MINIMOS-NT [9]. We implemented accurate models for surface-scattering, incomplete ionization, impact ionization, and other models that assess to investigate problems related with the device design. We utilized published material data to drive physical models. By adjusting model parameters close agreement to experimental data was achieved. The potential future performance of the proposed structure has been evaluated. The relationship between blocking and driving capability of our structure has been analyzed, and a simulation based comparison of the proposed accumulation-mode device with the conventional inversion-mode LDMOSFET has been performed.

2 Device Structure and Operation

The principal difference between the proposed SiC accumulation-mode LDMOSFET depicted in Fig. 1 and the conventional inversion-layer structure is the presence of a thin n-channel region (accumulation-layer) below the gate oxide using a buried p-well region formed by ion-implantation. The thickness, length, and n-doping of this accumulation-layer are carefully chosen so that it is completely depleted by the built-in potential of the p/n junction. This causes a potential barrier between the n+ source and the n-drift regions resulting in a normally-off device with the entire drain voltage supported by the n-drift region. Thus it can block high forward voltages at zero gate bias with low leakage currents. When a positive gate bias is

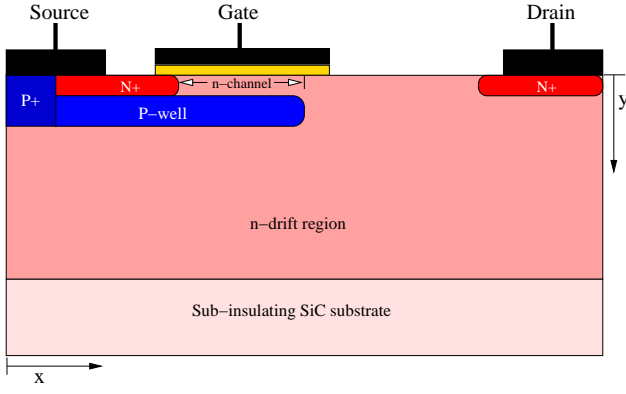


Figure 1. Schematics of the proposed SiC accumulation-mode LD MOSFET.

applied, an accumulation channel of electrons at the SiO_2 -SiC interface is created and hence a low resistance path for the electron current flow from the source to the drain can be achieved. This structure offers the possibility of moving the channel away from the oxide interface, thereby removing the consequence of the interface quality on the channel mobility. The structure also utilizes the buried p-well region as a shield to the influence of a high SiC bulk electric field on the gate oxide.

3 Physical Models

The choice of appropriate physical models is fundamental for any comparative study that involves numerical simulation. Among the SiC polytypes commercially available, for this work 6H-SiC is preferred owing to its higher inversion layer electron mobility and breakdown field strength [10]. A model that takes into account the mobility degradation due to surface scattering has been incorporated with [11] and implemented in our simulator MINIMOS-NT:

$$\mu_{n,p}^{\text{low}} = \mu_{n,p}^{\text{min}} + \frac{\mu_{n,p}^{\text{T}_0} \cdot \left(\frac{T}{T_0}\right)^{\delta_{n,p}^{\mu}} - \mu_{n,p}^{\text{min}} \cdot (1 - M(y))}{1 + M(y) \cdot \left(\frac{N_D + N_A}{N_{n,p}^{\mu}}\right)^{\gamma_{n,p}^{\mu}}} \quad (1)$$

$$M(y) = \frac{2 \cdot \exp\left(-\left(\frac{y}{y^{\text{ref}}}\right)^2\right)}{1 + \exp\left(-2 \cdot \left(\frac{y}{y^{\text{ref}}}\right)^2\right)} \quad (2)$$

where the function $M(y)$ depends on the surface distance y , and the parameter y^{ref} describes a critical length.

At high electric field the drift velocity $v_{n,p}$ of the carriers saturates due to increasing optical phonon scattering and finally reaches the saturation velocity $v_{n,p}^{\text{sat}}$, leading to the field dependent mobility as described by [12]

$$\mu_{n,p} = \frac{\mu_{n,p}^{\text{low}}}{\left[1 + \left(\frac{\mu_{n,p}^{\text{low}} \cdot E_{\parallel}}{v_{n,p}^{\text{sat}}}\right)^{\beta_{n,p}^{\text{sat}}}\right]^{\frac{1}{\beta_{n,p}^{\text{sat}}}}} \quad (3)$$

We take the component of the electric field parallel to the electron motion as driving force. The temperature dependence of $v_{n,p}^{\text{sat}}$ has been modeled by

$$v_{n,p}^{\text{sat}} = v_0^{\text{sat}} \cdot \left(\frac{T}{T_0}\right)^{\delta_{n,p}^{\text{sat}}} \quad (4)$$

and

$$\beta_{n,p}^{\text{sat}} = \beta_0^{\text{sat}} \cdot \left(\frac{T}{T_0}\right)^{\sigma_{n,p}^{\text{sat}}} \quad (5)$$

Several temperature-dependent Hall measurements have been reported, regarding the carrier concentration, and hence, the donor (E_D) and acceptor (E_A) energy levels in SiC. A function to describe ionized shallow donor and acceptor substitutional impurities is given by [13]

$$N_D^+ = \frac{N_D}{1 + g_D \frac{n}{N_C} \exp\left(\frac{E_D}{kT}\right)} \quad (6)$$

$$N_A^- = \frac{N_A}{1 + g_A \frac{p}{N_V} \exp\left(\frac{E_A}{kT}\right)} \quad (7)$$

Because of these deep levels, the dopants are not fully ionized even at higher temperatures so that we obtain an explicit relation for the ionization degree of a single donor level in n-type material

$$\xi_D = \frac{N_D^+}{N_D} = \frac{-1 + \sqrt{1 + 4g_D \frac{N_D}{N_C} \exp\left(\frac{E_D}{kT}\right)}}{2g_D \frac{N_D}{N_C} \exp\left(\frac{E_D}{kT}\right)} \quad (8)$$

and similarly in p-type material

$$\xi_A = \frac{N_A^-}{N_A} = \frac{-1 + \sqrt{1 + 4g_A \frac{N_A}{N_V} \exp\left(\frac{E_A}{kT}\right)}}{2g_A \frac{N_A}{N_V} \exp\left(\frac{E_A}{kT}\right)} \quad (9)$$

One of the most important parameters of a SiC device is its breakdown voltage. In order to obtain a clear understanding of its breakdown characteristics, it is important to have an exact knowledge of the impact ionization coefficients for SiC, which are modeled according to [14], where the dependence of the impact ionization rate on the electric field and temperature is given by

$$\alpha_{n,p} = a_{n,p} \gamma_a \exp\left(-\frac{b_{n,p} \gamma_a}{E_{\parallel}}\right) \quad (10)$$

$$\gamma_a = \frac{\tanh(\hbar\omega_{\text{op}}/2kT_0)}{\tanh(\hbar\omega_{\text{op}}/2kT)} \quad (11)$$

In these expressions α_n and α_p are the impact ionization coefficients for electrons and holes, respectively. The factor γ_a as a function of the optical phonon energy $\hbar\omega_{\text{op}}$ expresses the temperature dependence of the phonon gas against which the carriers are accelerated.

Models which account for generation and recombination have been employed. The Shockley-Read-Hall recombination is given by

$$GR_{SRH} = \frac{n_{ie}^2 - np}{\tau_p(n + n_{ie}) + \tau_n(p + n_{ie})} \quad (12)$$

where the life time $\tau_{n,p}$ can depend on a doping level as experimentally observed in Si technology [15] and is empirically modeled by the so-called Scharfetter relation:

$$\tau_{n,p} = \frac{\tau_{n0,p0}}{1 + \left(\frac{N_D + N_A}{N_{n,p}^{SRH}}\right)^{\gamma_{n,p}^{SRH}}} \quad (13)$$

Additionally, the Auger recombination rate is given by [16]

$$R_{Au} = (C_n n + C_p p) (np - n_{ie}^2) \quad (14)$$

Here, C_n and C_p denotes the Auger coefficient of electrons and holes, respectively.

4 Numerical Simulation

For numerical simulation we have utilized published material data listed in Table 1. Six parameters that alter the device performance have been investigated to optimize the device: The doping concentration of the n-drift region; the depth and the concentration of the implanted p-well; the doping concentration and the thickness of the n-channel (accumulation-layer); and the gate oxide overlap length. The p-well region has a Gaussian profile buried between 0.3 and 1.0 μm , which has to be optimized because it determines the thickness of the accumulation-layer region which in turn affects the gate oxide field, breakdown voltage, and on-resistance.

species	$\mu_{n,p}^{T_0}$ [cm ² /Vs]	$\mu_{n,p}^{\min}$ [cm ² /Vs]	$N_{n,p}^{\mu}$ [cm ⁻³]	$\gamma_{n,p}^{\mu}$
n	415	0.0	1.1×10^{18}	0.59
p	99	6.8	2.1×10^{19}	0.31
$\delta_{n,p}^{\mu}$	$v_0^{T_0}$ [cm/s]	β_0^{sat}	$\delta_{n,p}^{\text{sat}}$	$\sigma_{n,p}^{\text{sat}}$
-1.8	1.9×10^7	1.7	-1	1.25
E_D [meV]	E_A [meV]	g_D	g_A	y^{ref} [nm]
100	200	2	4	50
a_n [cm ⁻¹]	b_n [V/cm]	a_p [cm ⁻¹]	b_p [V/cm]	$\hbar\omega_{\text{op}}$ [meV]
1.66×10^6	1.27×10^7	5.18×10^6	1.4×10^7	106
τ_{n0} [s]	τ_{p0} [s]	$N_{n,p}^{\text{SRH}}$ [cm ⁻³]	$\gamma_{n,p}^{\text{SRH}}$	$C_{n,p}$ [cm ⁶ /s]
1×10^{-7}	2×10^{-8}	3×10^{17}	0.3	3×10^{-29}

Table 1. Model parameters used for simulating 6H-SiC.

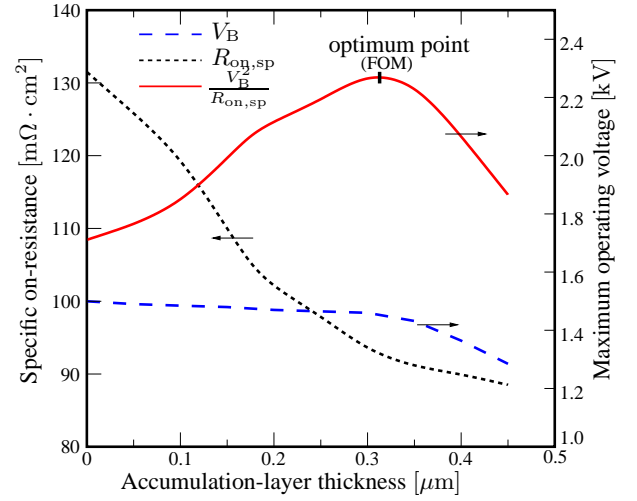


Figure 2. Effect of the accumulation layer thickness on maximum operating voltage and specific on-resistance.

For the desired breakdown voltage of 1500 V, the proposed structure is optimized to have a 33 μm cell pitch, a 10 μm thick n-drift region doped at $5.0 \times 10^{15} \text{ cm}^{-3}$ and an n+ polysilicon gate electrode with a 50 nm thick gate oxide. When the buried p-well depth is larger, the built-in potential is unable to fully deplete the n-channel which causes high leakage currents. Therefore, its depth and implanted peak concentration of 0.5 μm (between 0.3 – 0.8 μm) and $1.0 \times 10^{18} \text{ cm}^{-3}$ respectively was found to give the optimum accumulation layer thickness at which the criterion for the device optimization (figure of merit, FOM) [17] can be satisfied. It is given by

$$\frac{V_B^2}{R_{\text{on,sp}}}|_{\text{opt}} = \mu_n \epsilon_s \left(\frac{2E_c}{3}\right)^3 \quad (15)$$

where V_B is the breakdown voltage, $R_{\text{on,sp}}$ is the specific on resistance, E_c is the critical electric field, μ_n is electron mobility parallel to the c axis and ϵ_s is the SiC dielectric constant.

Values of the accumulation layer thickness, length and concentration of 0.3 μm , 4 μm and $5.0 \times 10^{15} \text{ cm}^{-3}$, respectively, have been established to achieve the desired on- and off-state characteristics. At these optimum values and room temperature, a specific on-resistance of 93.2 $\text{m}\Omega \cdot \text{cm}^2$ and a breakdown voltage of 1460 V with the corresponding small leakage current was achieved. The effect of the accumulation layer thickness on the maximum operating voltage, specific on-resistance and criterion for the device optimization obtained by simulation is illustrated in Fig. 2.

The gate oxide overlap was varied from 4 to 7 μm , and its influence on the surface field and operating voltage was analyzed. According to Gauss' law the field in the oxide is approximately 2.5 times higher than the peak field in the SiC bulk. Therefore, the oxide breakdown must not take place before the avalanche breakdown occurs in the SiC bulk. Simulation predicted that a gate oxide overlap length of 6 μm is optimal.

5 Result and Discussion

The proposed accumulation-mode LDMOSFET shows a fairly large advantage in terms of electrical performance compared to its standard inversion-mode LDMOSFET counterpart. Excellent I-V characteristics were obtained with good current saturation and gate control as depicted in Fig. 3. In addition to its superiority in the logic level gate bias voltage operation, the proposed structure has also shown significant improvement on the higher gate bias voltage characteristics as shown in Fig. 4.

One of the important areas of improvement for the SiC MOSFET device is the decrease in its conduction losses which is governed by its specific on-resistance. This on-resistance depends on the channel and the n-drift resistance of the device. An estimate of the on-resistance contribution indicates that 90% of the on-resistance is due to the large channel resistance, owing to the low inversion layer mobility. The proposed structure is able to minimize this resistance and improve the mobility. A simulated accumulation layer mobility of $120 \text{ cm}^2/\text{Vs}$ compared to the $18 \text{ cm}^2/\text{Vs}$ for the inversion-layer was observed, which is in good agreement with experimental results extracted at a different temperature [10]. Significant improvement on the reduction of the gate bias voltage (a logic level gate bias of 5 V) has been achieved to obtain good on-state conduction as shown in Fig. 5. The device is normally off with a threshold voltage of only 1 V compared to that of 3 V for the inversion-mode structure.

In addition to moving the channel away from the oxide interface and removing the effect of interface quality on the channel mobility, the proposed structure offers the possibility of serving as a shield to the influence of high SiC bulk electric field on the gate oxide. The peak surface electric field at the maximum blocking voltage has been kept

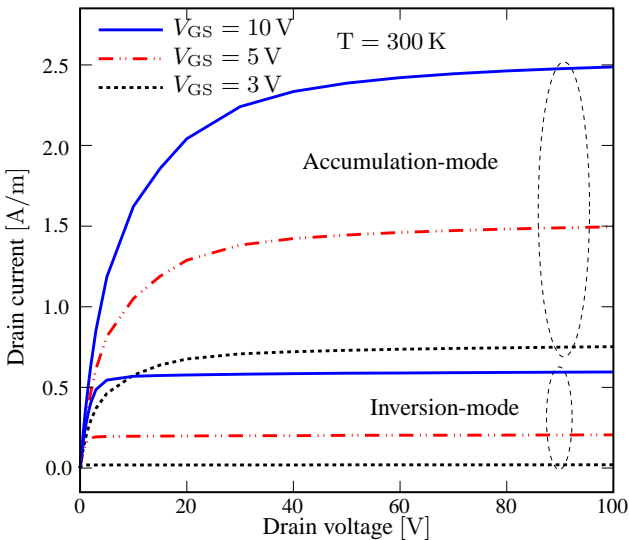


Figure 3. Comparison of output characteristics at a logic level gate bias voltage.

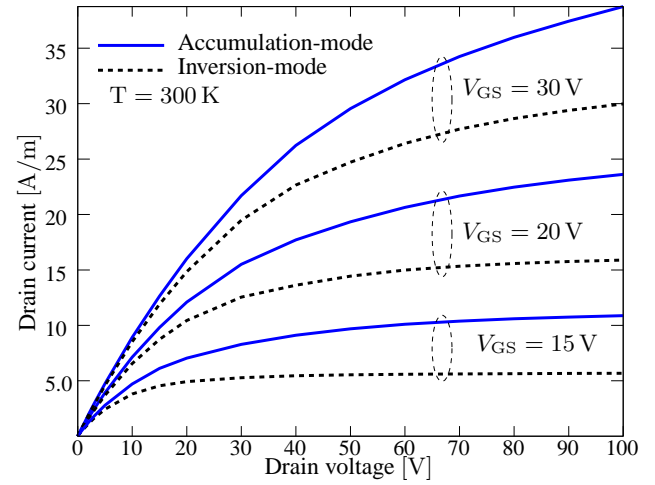


Figure 4. Comparison of on-state characteristics.

below 1.5 MV/cm . That is equivalent to the oxide field of 3.75 MV/cm , and considerably lower than the practical limit of the electric field strength in the oxide. Therefore, the proposed structure improves the reliability of the device while utilizing the high breakdown electric field strength of SiC.

A breakdown voltage of 1460 V with a leakage current comparable to that of standard inversion-mode LDMOSFET was achieved as shown in Fig. 6. The off-state leakage current caused by the built-in potential of the p/n junction is ten orders of magnitude less than the on-state current for the same structure, but one order of magnitude greater than the inversion-mode structure. This can effectively be suppressed by calibrating parameters which enable a fully depleted accumulation-layer. High temperature causes an increase in the leakage current due to the increased intrinsic carrier concentration.

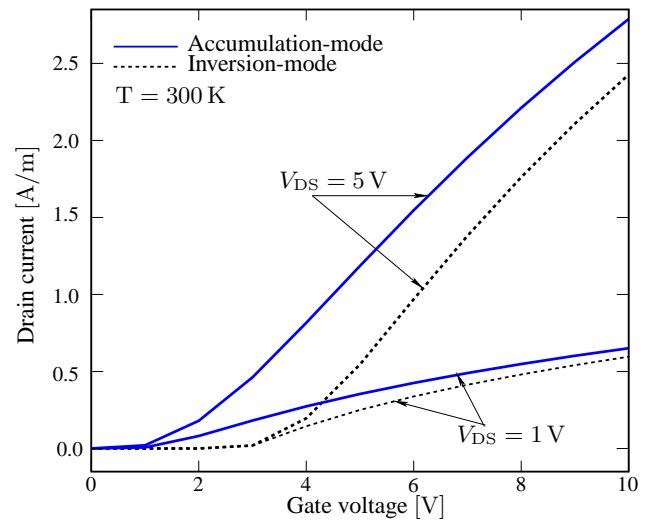


Figure 5. Comparison of transfer characteristics.

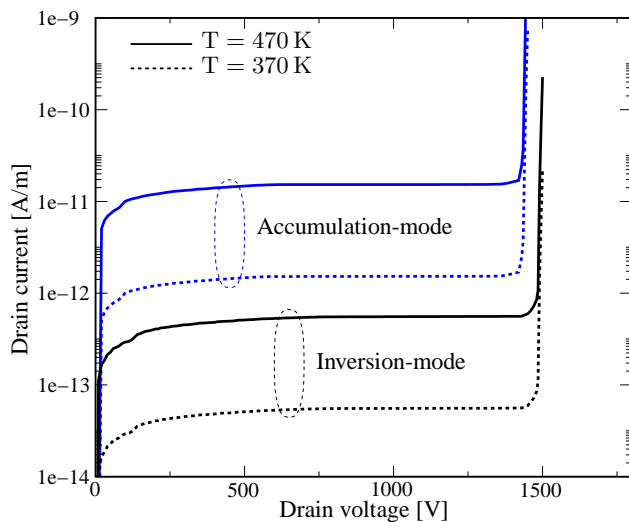


Figure 6. Comparison of off-state characteristics.

6 Conclusion

Numerical device simulation has been performed in order to get an insight into the physics and the behavior of silicon carbide MOSFETs. A new structure for a lateral DMOSFET that minimizes problems caused by lack of material development and design has been proposed. Key design parameters were optimized and analyzed. The models describing the electrical properties have been driven by the parameters reported in recent literature. Simulation based comparisons were conducted between the proposed device and the standard structure using the same condition and parameters. It turns out that the proposed structure shows a fairly large advantage in terms of electrical performance. A remarkable improvement on the reduction of the gate bias voltage to obtain good on-state conduction has been achieved. Excellent transfer characteristics were obtained with the output current increased by five times. The device also exhibits a blocking voltage of 1460 V with an oxide field below 3.75 MV/cm which is considerably lower than the practical limit of the oxide breakdown field.

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