Physics of Semiconductor Devices
(IWPSD-2003)
Editors K N Bhat and A DasGupta

Numerical Simulation of High-Speed High-Breakdown Indium Phosphide HBTs

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We present state-of-the-art results of two-dimensional numerical simulations of Indium Phosphide (InP) Double Heterojunction Bipolar Transistors (DHBTs) in comparison with experimental data. The rigorous device and circuit simulator MINIMOS-NT has been equipped with all required capabilities to simulate such advanced heterostructures.

I. INTRODUCTION

InP-based HBTs bear a number of advantages over the GaAs material system for many applications. They offer performance advantages [1] for high-speed low-power fiber optic communication applications, for millimeter-wave and even for wireless applications due to the high gain $\times$ breakdown voltage product. InP-based HBTs have demonstrated excellent cut-off frequencies f_{T} and maximum oscillation frequencies $f_{\max}$, but due to the narrow bandgap collector only low collector breakdown voltages BV_{CE0} (typically below 2.0 V) are found.

In order to increase the breakdown voltage, a second heterojunction and, thus, double heterojunction bipolar transistors have been introduced. Promising results with cut-off frequencies up to 341 GHz [2] and breakdown voltages in the order of 9 V have been demonstrated. Wide bandgap materials such as InP allow a higher BV_{CE0} due to the reduced collector fields and thus a reduced impact ionization rate.

In addition, the thermal conductivity of InP is higher than that of GaAs, and the electron saturation velocity v_{sat} of InP is about two times higher with a maximum occurring at higher fields than in GaAs or InGaAs resulting in a short collector transit time at high breakdown voltages [3]. The DHBT is limited by collector current blocking due to the conduction band discontinuity. Thus, the design of the second (base-collector) heterojunction is of utmost importance. Quaternary materials such as a linearly or step graded InGaAsP, dipole doping, or launcher structures are frequently used to lower the conduction band energy spike.

II. PHYSICAL MODELING

The two-dimensional device simulator MINIMOS-NT [4] can deal with various semiconductor materials and complex geometrical structures. Previous experience gained in the area of III-V HBT modeling and simulation which lead to successful results [5] was a prerequisite to use MINIMOS-NT also for the simulation of InP HBTs.

Important issues which have been solved in the course of our work are proper modeling of the en-

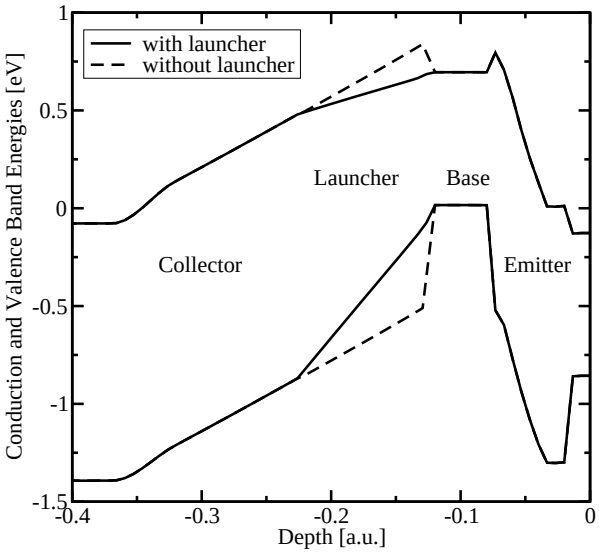

Fig. 1: Band diagram of layer structures of a DHBT with and a DHBT without an InGaAsP launcher under thermal equilibrium.

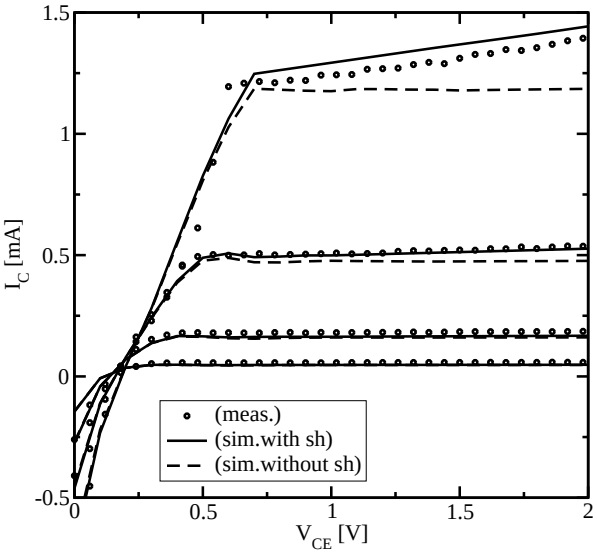

Fig. 2: Comparison of measured and simulated output characteristics for V_{BE} stepped by 0.05 V from 0.65 V to 0.80 V with and without self-heating (sh).

ergy bandgaps and bandgap alignments between InGaAs and InP, and the bandgap narrowing effect at high doping concentrations, especially in p^+ InGaAs.

Fig. 1 shows the effective bandgap energies in the conduction and the valence band in a vertical cut of the device structure under investigation. As can be seen, tunneling mechanisms dominate electron transport between the emitter and the base, and in the case of a DHBT without launcher also between the base and the collector. These tunneling effects must be properly described in the modeling of the interface. In addition, high-field/high-energy electron transport in InGaAs and InP (respectively the quarternary InGaAsP), which determines both the steady-state and small-signal device behavior, has been carefully modeled.

Details about the material parameters used for InP, $In_{0.53}Ga_{0.47}As$, and the spacer material InGaAsP can be found in [6].

III. Investigated Device Structure

We investigated a nominally self-aligned 1×8 μm^2 InP/InGaAs/InGaAsP/InP DHBT structure. The layers were grown by Metal Organic Chemical Vapor Deposition (MOCVD) on 3-inch InP substrates. The InGaAs emitter cap is followed by an InP emitter and an $In_{0.53}Ga_{0.47}As$ base carbon-doped at 2×10^{19} cm^{-3}. A quaternary graded spacer is used to connect the base and the collector. Typical characteristics are a peak cut-off frequency about 130 GHz and a breakdown voltage of BV_{CE0} = 5.5 V.

IV. Simulation Results

A proper DC calibration was performed, as can be seen, for example, in Fig. 2 showing the output characteristics. The base-emitter voltage V_{BE} is stepped by 0.05 V from 0.65 V to 0.80 V. The quality of the simulation results is proven by comparison with experimental data. Despite the good thermal conductivity of InP, the output characteristics are critically influenced by self-heating, due to the small feature size of the device and the resulting high current densities. Therefore, self-heating must be included in the simulation, especially at higher voltages ($V_{\mathrm{CE}} \geq 1$ V).

In addition, high-frequency small-signal simulation results were obtained. MINIMOS-NT provides an efficient linear small-signal AC mode,

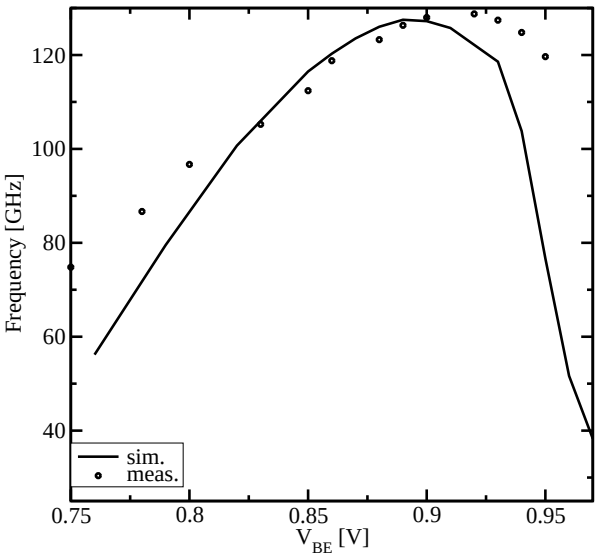

Fig. 3: Comparison of simulated and measured peak cut-off frequency f_{T} curves at $\mathrm{V_{CE}}$ = 1.1 V and V_{BE} stepped from 0.76 V to 0.97 V.

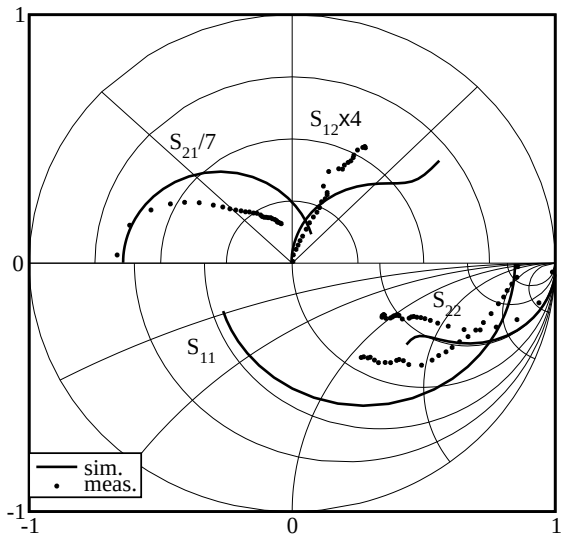

Fig. 4: Intrinsic S-parameters in a combined Smith-polar chart from 250 MHz to 120 GHz at $\mathrm{V_{CE}}$ = 1.1 V and $\mathrm{V_{BE}}$ = 0.91 V.

which is based on the $\mathrm{S^3A}$ approach from [7].

Fig. 3 gives a comparison of simulated and measured cut-off frequencies f_{T} at V_{CE} = 1.1 V and V_{BE} stepped from 0.76 V to 0.97 V. Fig. 4 shows a comparison of intrinsic S-parameters at V_{CE} = 1.1 V and V_{BE} = 0.91 V in a frequency range between 250 MHz and 120 GHz. For frequencies below 40 GHz the agreement is good for all four S-parameters and confirms the intrinsic DC modeling of the device. However, for higher frequencies the extrinsic passive environment of such a small high-speed device appears to be more complicated than the one-shell approach [6] we used.

V. Conclusion

The current results demonstrate the ability of analyzing InP DHBTs by means of numerical device simulation. With the confirmation of the modeling parameters at frequencies below 40 GHz, further analysis is possible with respect to the high-speed design trade-offs for the base and the collector regions.

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