



# EXTRACTION OF MATERIAL PARAMETERS BASED ON INVERSE MODELING OF THREE-DIMENSIONAL INTERCONNECT STRUCTURES

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## ABSTRACT

*We present an approach for extracting thermal coefficients of higher order for different materials. Based on inverse modeling and using transient electrothermal simulations thermal investigations of complex layered polycrystalline silicon (Polysilicon) fuses are performed by a three dimensional interconnect simulator. This method is well suited to optimize different material compositions and geometries as well as for achieving an optimum of speed and reliability.*

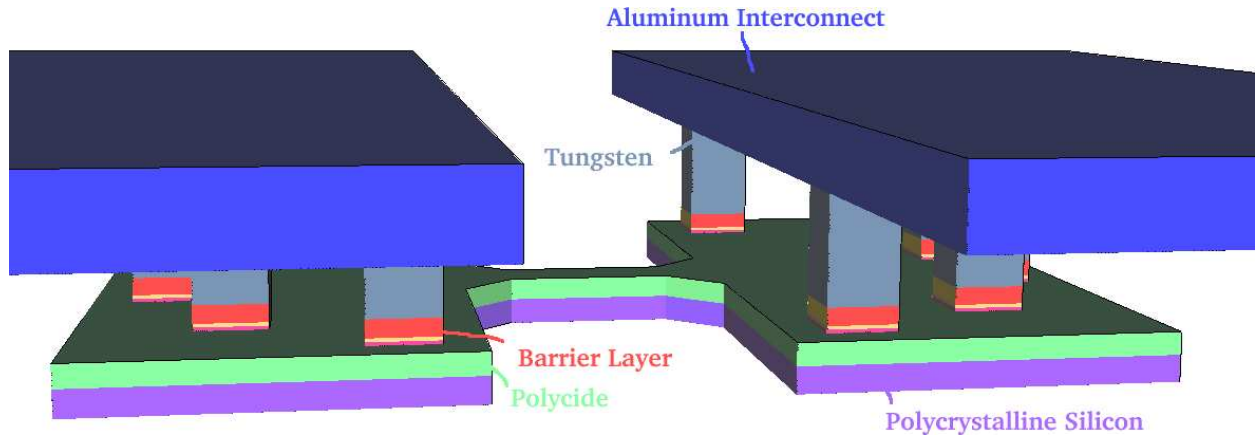
## 1. INTRODUCTION

State-of-the-art submicron semiconductor process technology nodes use Polysilicon fuses as one-time programmable devices which provide memories up to several kilobits and offer a cheap, efficient, and area-saving alternative to small non-volatile memories for System-on-a-Chip solutions. Approaches to increase the memory density by using 3-state fuses of layered materials have been reported [1]. Another important application is in simple field programmable gate arrays or for trimming CMOS circuits to obtain a specific analog performance [2]. Furthermore, the fuses are used to provide variable elements as trimable resistor or capacitor arrays [3]. Finally, the fuses may act as the classical protective elements for improved protection and replacement of critical components before actual failures [4].

Programming is performed by sending a current pulse through the fuse, resulting in opening the Polysilicon

film after transition to a second-breakdown state. The transition occurs when parts of the Polysilicon layer reach the silicon melting point, and the molten silicon is transported from the negative end through drift of ions in the applied field [5]. Fuses implemented in deep submicron technologies become more and more attractive in terms of power and area consumption, and hybrid approaches using other materials are getting less important [6]. Nevertheless, going to smaller ground rules below 350 nm implies decreasing supply voltages to 1.5 V and below [7]. This constraint requires a careful optimization of the fuse layout, ensuring an efficient and reliable programming mechanism [8] and minimizing the necessary power consumption of the fusing process. As the fusing process takes place in a short time interval (between a couple of nanoseconds up to the microsecond range), direct thermal measurements of this process are hard to obtain. Previously carried out work [9] already shed some light on the physics behind the fusing mechanism, but the optimization of the fuse structure for reliable and fast fusing was only possible via expensive experimental work by using test chips.

This work focuses on gaining better insight into the materials characteristics used in the structure, to enable a layout optimization through simulation. Since the electrical and thermal properties of Polysilicon are a complex function of Polysilicon film doping, grain size, and grain morphology [10], the average electrical and thermal properties as a function of temperature were obtained by experimentally measuring the transient resistivity response of the fuse through Joule self-heating and subsequent inverse modeling this measured data to fit the observed behavior.



**Figure 1:** Device structure showing the variety of included materials

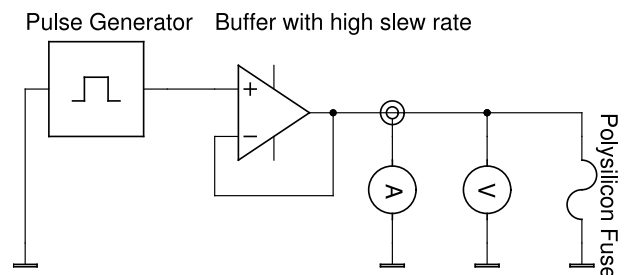
The electro-thermal self-heating simulations were carried out with the Smart-Analysis-Package (SAP) for three-dimensional interconnect simulation [11] in combination with SIESTA, a TCAD optimization framework combining gradient based and genetic optimizers [12].

This approach enabled the optimization of the fuse layout of such devices by significantly saving costs normally spent in design and production of layout test chips. Furthermore, a better insight into the transient electro-thermal effects occurring in the first couple of microseconds was gained.

## 2. EXPERIMENT

An industry standard deep submicron Polycide gate CMOS process is used for fabrication of the investigated Polysilicon fuse devices. On a specialized test chip multiple different layout variations were placed to find the optimum layout for fast and reliable fusing. A more complicated example of a fuse structure is shown in Fig. 1. The first experiments were performed with rectangular pulses. Nevertheless, due to the steep slope of the fuse terminal voltage the initial fuse heating is not well resolved. Furthermore, the initial transient behavior of the measurement circuit yields high errors in the measured current. To overcome these problems a voltage ramp was applied and the resulting fusing resistance was calculated by assuming ohmic behavior. The Polysilicon layer in the fuse is doped to solid solubility, and therefore its conductivity may be considered to be approximately ohmic. Since all materials in the fuse except the Polysilicon layer are metallic, this assumption shall give a reasonable estimate for the fuse resistivity. The devices were stressed with different triangular voltage ramps for a few microseconds. A pulse generator was used to define the length of the pulse. As the generator has a typical output impedance of  $50 \Omega$  and the

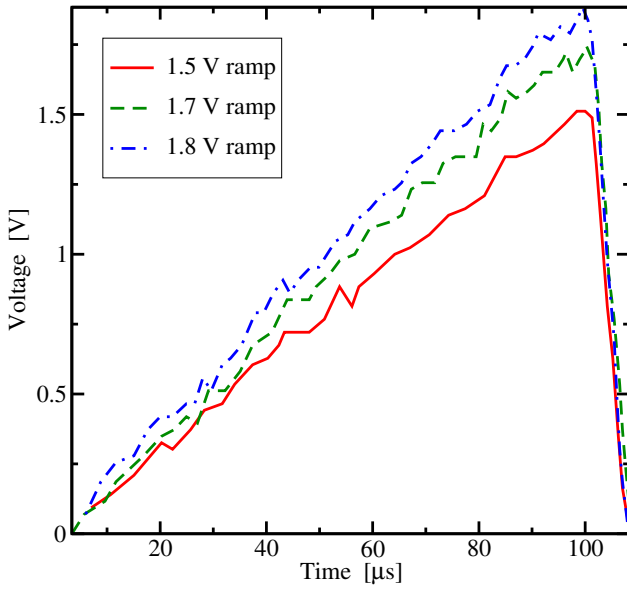
resistor of the Polysilicon fuse is lower than that, the source has to be buffered by an operational amplifier with a high slew rate to get a stable voltage. To avoid an additional voltage drop on a serial resistor a current probe was used. In addition, the voltage on the fuse was monitored by an oscilloscope to calculate the right resistor value. The measurement principle can be seen in Fig. 2.



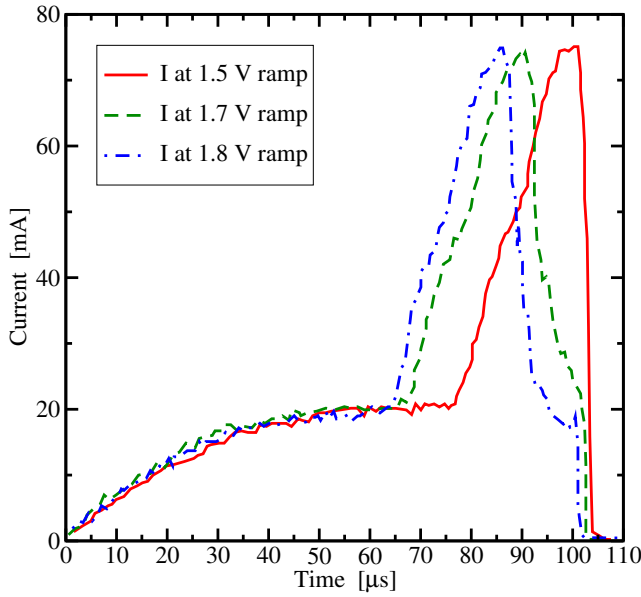
**Figure 2:** Schematic of the measurement circuit of a Polysilicon fuse

The measurement data for three different source voltages and the corresponding currents through the fuse as functions of time are given in Fig. 3 and Fig. 4, respectively. The current diagram shows a significant increase over  $65 \mu\text{s}$  due to melting processes which speed up heating the fuse structure. The current peak in Fig. 4 indicates the presence of plasma threads in the fuse structure which reduce the resistivity dramatically before the fuse structure is completely molten.

The negative temperature coefficient of the electrical conductivity in all three curves is caused by the combined Joule self-heating of the Polysilicon/Polycide layer sandwich (see Fig. 1). The high noise in the data during the first  $10 \mu\text{s}$  is due to the low voltage level in this time regime and the resulting low signal-to-noise ratio.



**Figure 3:** Voltage ramps applied at the fuse terminals as a function of time



**Figure 4:** Measured fuse current as a function of time

### 3. SIMULATION AND INVERSE MODELING

#### 3.1. Mathematical Models

For numerical calculation of Joule self-heating effects two partial differential equations have to be solved. Poisson's equation

$$\operatorname{div}(\gamma_E \operatorname{grad} \varphi) = 0 \quad (1)$$

gives the electric potential  $\varphi$  where  $\gamma_E$  denotes the electric conductivity. The power loss density  $p$  is obtained by computing

$$p = \gamma_E (\operatorname{grad} \varphi)^2. \quad (2)$$

The heat conduction equation

$$c_p \rho_m \frac{\partial T}{\partial t} - \operatorname{div}(\gamma_T \operatorname{grad} T) = -p \quad (3)$$

is solved to obtain the temperature distribution where  $\gamma_T$  represents the thermal conductivity,  $c_p$  the specific heat, and  $\rho_m$  the mass density. The temperature dependence of the thermal and the electrical conductivities is modeled as

$$\gamma(T) = \frac{\gamma_0}{1 + \alpha(T - T_0) + \beta(T - T_0)^2} \quad (4)$$

where  $\gamma_0$  is the thermal or electrical conductivity at the temperature  $T_0 = 300$  K, and  $\alpha$  and  $\beta$  are the linear and quadratic temperature coefficients of the specified materials.

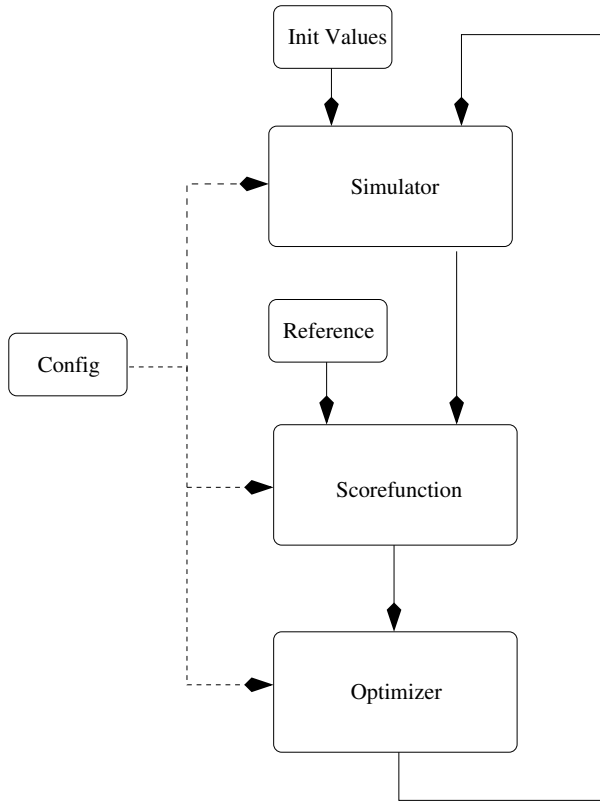
#### 3.2. Simulation Setup

The layout of the fuse was transformed into a three-dimensional representation of the device using a detailed process description of the interconnect deposition and etch steps. Using the well known electrical conductivity of the interconnect and barrier layers the structural setup was calibrated by calculating the overall resistance of the structure excluding self-heating effects. The Polysilicon conductivity was determined from the observed overall resistance and the resulting value was compared to independently measured sheet resistances of the polycrystalline layer in fabrication. Excellent agreement between simulation and measurements has been achieved. The subsequent transient simulations were set up including the thermal coefficients of the electrical conductivity, the thermal conductivity, and the heat capacity of all layers in the structure. The initial values of these parameters were taken from literature data.

#### 3.3. Inverse Modeling

State-of-the-art simulation frameworks like SIESTA [12–15] offer a wide range of optimizers, simulators, and optimization strategies. In contrast to commercially available software, e.g. [16] and [17], the simulation framework SIESTA provides numerous types of optimizers which can be chosen for a particular problem.

Reference data for the optimization presented here are measurements of the resistance derived from Fig. 3 and Fig. 4.



**Figure 5:** Internal data flow of SIESTA

A brief overview of the structure and the data flow of SIESTA is given in Fig. 5. At start time SIESTA guesses the initial values of the free parameters within the user defined constraints for the three-dimensional interconnect simulator STAP of the SAP package, as introduced in [11]. The output of the simulation is parsed by SIESTA in order to compare it with the reference data. It produces a score value that indicates how good these two data sets match. This value is submitted to the optimizer which generates corresponding to the score value the next n-tuple of free parameters. This improves the next score value that will be evaluated after the next simulation run with the currently produced values.

The optimizer mainly used in SIESTA is a genetic optimizer that relies on the theory of evolutionary computation and generic algorithms described in [12] and [15]. The population of the n-tuples of free parameters are chosen randomly with respect to a Gaussian normal distribution. Several distribution and generation parameters can be configured and tuned to fit for special needs. Furthermore, the simulation of the population

can be distributed on a computer cluster to significantly decrease the optimization time.

Large intervals of free parameters can result in convergence problems because of non-physical parameter values which would result in negative resistance or negative doping. To avoid these problems, the simulation framework SIESTA provides a divergence detection where it is signaled when the simulator has problems to converge. This feature allows the user to expand the intervals of the free parameters in a wider range as before.

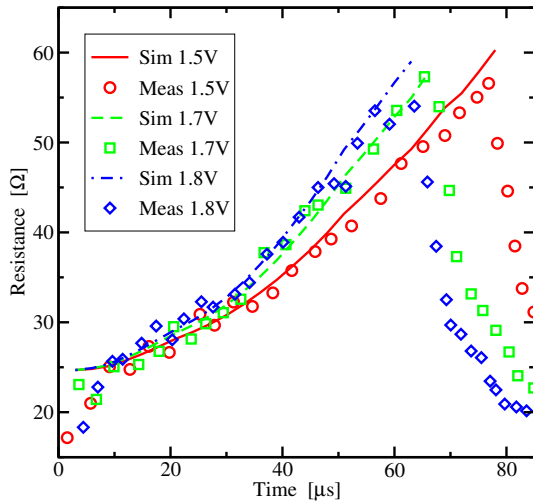
## 4. RESULTS AND DISCUSSION

With the simulation framework SIESTA the thermal coefficients of the conductivities have been computed in order to minimize the difference between the reference data and the simulation results. To check the consistency of the setup, all thermal and electrical parameters were used for the automated simulation run, resulting in a total of 10 parameters. The resulting best fit to the measured reference data is given in Table 1. The electrical and thermal conductivities  $\gamma_{0,E}$  and  $\gamma_{0,T}$  as well as the linear temperature coefficient of the thermal conductivity  $\alpha_T$  for Polysilicon are in excellent agreement compared to data reported in [10]. The electrical conductivity of the Polysilicon/tungsten silicide sandwich as a function of temperature is comparable to data measured electrically by external heating of the layers.

**Table 1:** Parameters of electrical and thermal conductivity for materials used in the fuse structure

	Poly Si	WSi <sub>2</sub>
$\gamma_{0,E}$ [1/ $\mu\Omega\text{m}$ ]	0.12	1.25
$\alpha_E$ [1/K]	$9.1 \times 10^{-4}$	$8.9 \times 10^{-4}$
$\beta_E$ [1/K <sup>2</sup> ]	$7.9 \times 10^{-7}$	$8.1 \times 10^{-7}$
$\gamma_{0,T}$ [W/Km]	45.4	119.4
$\alpha_T$ [1/K]	$2 \times 10^{-2}$	$2.98 \times 10^{-2}$

The optimized parameter set results in resistance characteristics as shown in Fig. 6 where an excellent match with the measurements is obtained. The strong increase of the resistance as a function of time due to self-heating is evident. After a certain critical temperature is reached the resistance drops dramatically and the ohmic approximation loses its validity. To generalize this result for other fuse geometries this critical temperature has to be extracted. As expected, the critical temperatures of all the three samples are at about 1150 K (cf. Fig. 7). This value is much smaller than the silicon melting point of 1414 °C and the tungsten silicide (WSi<sub>2</sub> phase) melting point of 2015 °C [18]. The



**Figure 6:** Comparison of measured and simulated resistance as a function of time

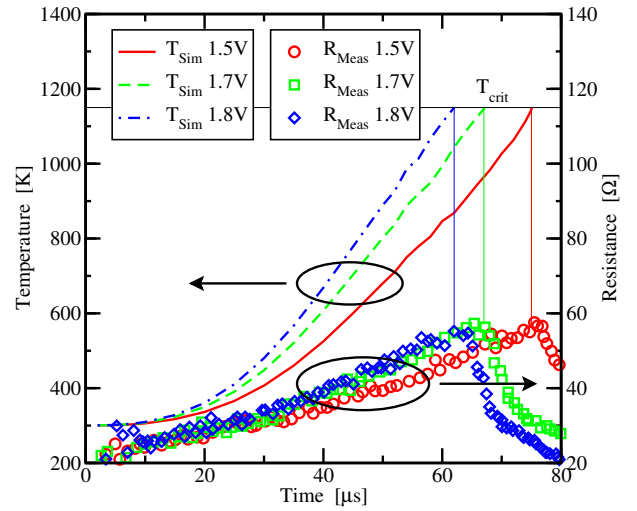
maximum temperature of the Polysilicon fuse is observed in the center of the tungsten silicide layer as shown in Fig. 8.

Several mechanisms for this low critical temperature are possible. First, the disordered region between the tungsten silicide and the silicon may have a stoichiometry closer to the eutectic point of the tungsten silicide system and therefore a lower melting point. But since the lowest eutectic temperature of the W-Si system is 1389 °C [18], this is not likely for pure alloys. Second, the high doping concentration of the Polysilicon layer reduces the melting temperature as reported for silicon glasses with high Boron and Phosphorus contents. And finally, the assumption that all materials show ohmic behavior over the full temperature range between 300 K and 1200 K does not hold for higher temperatures.

The intended target for getting the possibility to optimize fuse layouts for better performance is not affected since it is obvious from Fig. 7 that the melting begins always at approximately the same temperature. Therefore the method should be applicable for other geometries as well. The agreement between experiment and simulation is excellent and provides a reliable base for carrying out predictive simulations of the transient temperature distribution during the initial heating phase of the fusing.

## 5. CONCLUSION

We have presented a method to obtain important material parameters by inverse modeling using transient finite element simulations of complex interconnect structures. This method is capable of describing the electric



**Figure 7:** Simulated temperature and measured resistance showing the critical temperature

cal behavior of interconnect materials over a significant temperature range. Furthermore, it uses the transient thermal self-heating effect to separate different materials and their electrical and thermal properties. Nevertheless, the exact conduction mechanism inside the Polysilicon layer is still not well reflected in this analysis. The impact of the grain boundary barriers and their behavior at high temperature could be addressed by implementing a more accurate model like the model of Mandurah [19]. However, we have demonstrated that our method is consistent and gives an excellent match to experimental results. With the extracted critical temperature, where the material loses its ohmic properties, the geometry can be optimized in terms of reliability and speed.

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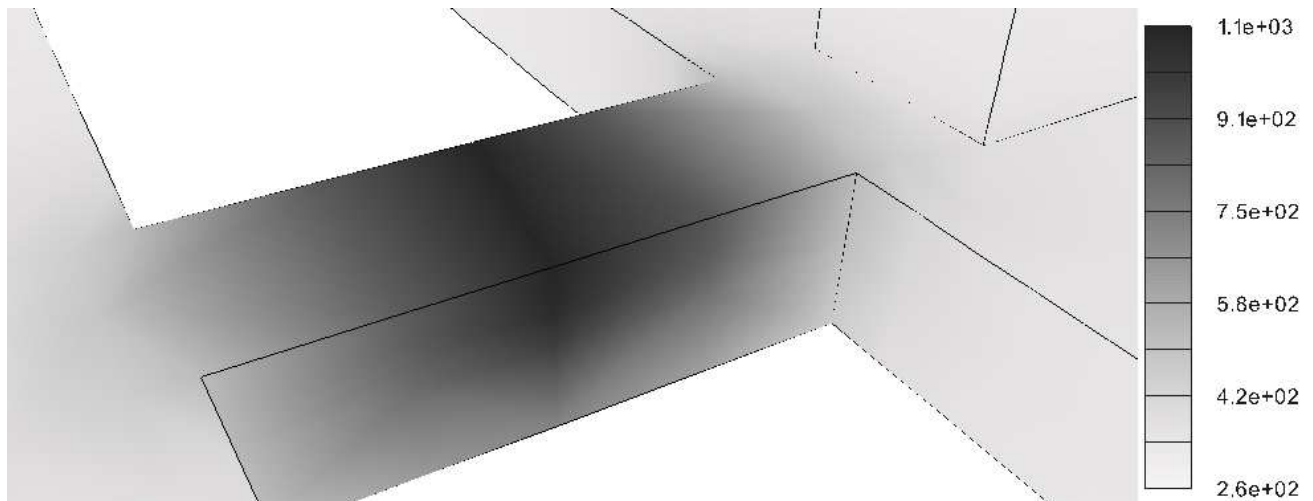


Figure 8: Temperature distribution [K] in the interconnect structure at  $65 \mu\text{s}$  and 1.7 V

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