Mobility Enhancement in Strained CMOS Devices

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ABSTRACT

Performance improvement in CMOS technology can be achieved by further down-scaling and alternatively by the introduction of new device structures and materials. One of the most promising candidates is strained Si, since it provides mobility enhancement both for electrons and holes. This paper reviews theoretical and experimental achievements reported in recent years. Special focus is put on the gain in carrier mobility in strained Si layers. The Monte Carlo method is well suited to analyze of the transport properties of the strained Si/SiGe material system and for providing models for TCAD applications.

Keywords: strained Si, SiGe, MOSFET, carrier transport, mobility enhancement, Technology CAD, Monte Carlo simulation

1 INTRODUCTION

In the last years, there has been enormous research in the area of materials compatible with Si technology and device structures for improving the speed of VLSI circuits. Strained Si has emerged as a promising material, since it offers both higher electron and hole mobility than unstrained Si. Improvement by a factor of more than two was both theoretically predicted and experimentally confirmed.

A strained Si FET structure typically consists of a SiGe buffer layer grown on Si substrate. The buffer is sufficiently thick to allow for strain relaxation. A Si layer grown on top of the SiGe buffer is strained and therefore has different material properties, making it a suitable choice as a channel material. There are two major types of strained Si FETs, namely modulation-doped buried channel devices (MODFET CMOS) and surface channel devices (Strained Si CMOS or SSCMOS). The MODFET has a more complex structure and shows a somewhat higher improvement in carrier mobility in comparison to surface channel devices.

Strained Si/SiGe FETs exhibit superior performance for RF applications. Major developments have been reported by IBM [1, 2, 3, 4, 5, 6, 7, 8] and DaimlerChrysler (DC) [9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20], both for p- and n-type devices. Fig. 1 summarizes reported values for the cut-off frequencies f_T and f_{max} in the last years.

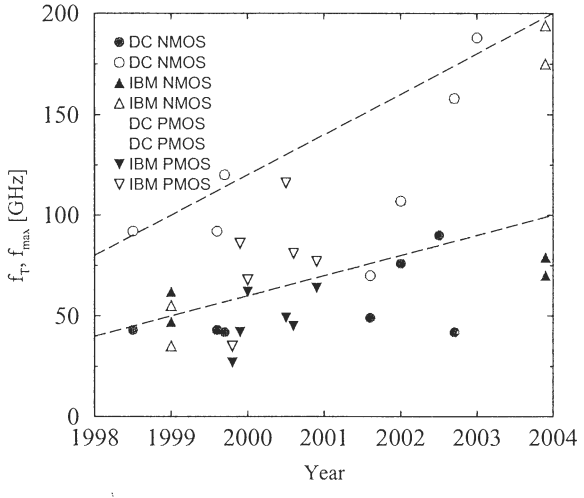

Figure 1: Cut-off frequencies f_T (filled symbols) and f_{max} (open symbols) of strained-Si FETs.

2 PHYSICAL BACKGROUND

Strained Si layers are achieved by growth on SiGe buffers. Due to the lattice mismatch, a pseudomorphically grown Si layer on a relaxed SiGe buffer experiences a biaxial tensile strain, provided that the layer thickness is below a critical value to prevent strain relaxation. This strain leads to a modification of both the conduction and valence bands, as shown in Fig. 2. In the conduction band, the 6-fold degenerate Δ_6-valleys in Si are split into 2-fold degenerate Δ_2 valleys (lower in energy) and 4-fold degenerate Δ_4 valleys (higher in energy). The lower in-plane effective mass of electrons in the Δ_2 valleys and the reduction of inter-valley phonon scattering lead to an enhanced electron mobility. Similarly, the strain lifts the degeneracy of the light and heavy hole bands and lowers the spin-orbit band. The change in the valence band structure results in a reduction of inter-band scattering between the light and heavy hole bands, and therefore improves the hole mobility. Fig. 3 shows the band alignment of strained Si relative to relaxed SiGe and unstrained Si. The figure shows the strain-induced splitting of the conduction and valence bands, together with the band edge discontinuities, as a function of the germanium content y in the relaxed SiGe buffer. In the calculations, a linear dependence of the discontinuities on y has been assumed which gives a good agreement with reported data [21].

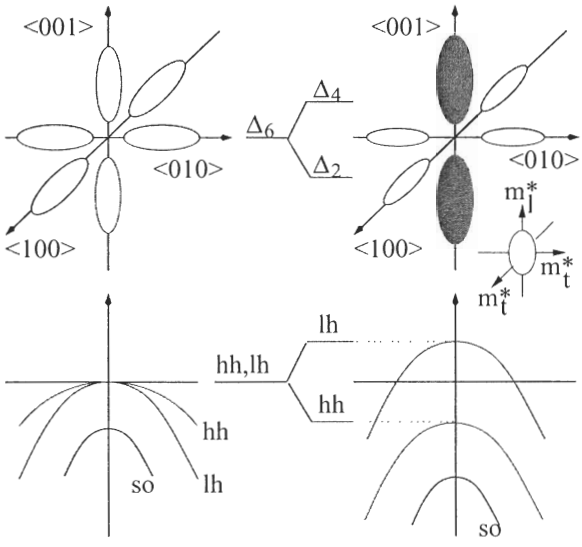

Figure 2: Conduction and valence band splitting in tensile-strained Si (right) compared to unstrained Si (left).

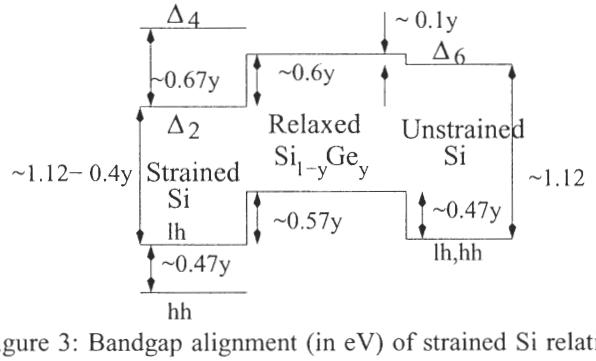

Figure 3: Bandgap alignment (in eV) of strained Si relative to relaxed $Si_{1-y}Ge_y$ and Si.

3 CARRIER MOBILITY ENHANCEMENT

The benefit of using strained-Si for n-MOSFETs is demonstrated in Fig. 4. The mobility enhancement factor is defined as the ratio between the mobility in strained Si MOSFETs and the mobility in conventional Si MOSFETs. Fig. 4 shows the mobility enhancement ratio for electrons as a function of the germanium content y in the SiGe buffer layer. The figure compares experimental data from Stanford University [22, 23, 24], MIT [25, 26, 27, 28], IBM [29, 30, 31, 32], Hitachi [33], ERSO/ITRI [34], TSMC [35], Toshiba [36, 37, 38, 39] and Monte Carlo calculations from Vogelsang et al. [40], Rashed et al. [41], Takagi et al. [42], and from [43]. As can be seen in the figure the enhancement of the electron mobility increases gradually with the Ge content y for $y < 0.2$ and tends to saturate for higher values.

It is remarkable that electron mobility enhancement of more than 50% is observed in a wide range of effective fields (up to 2 MV/cm) and doping concentrations (up to 6×10^{18} cm^{-3}) found in modern CMOS devices. Fig. 5 summarizes selected data from Stanford University [23, 24], MIT

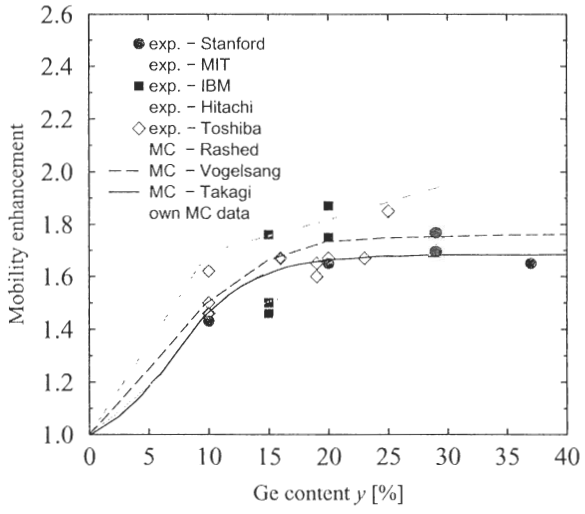

Figure 4: Mobility enhancement ratio for electrons as a function of the Ge content y in the $Si_{1-y}Ge_y$ buffer layer.

[25, 26, 28, 44], IBM [29, 30, 31, 32], Hitachi [33], Toshiba [37, 45, 46, 47, 48] for the effective electron mobility in strained Si as a function of the effective field. The upper figure shows data for Ge content $y \leq 0.15$ in the $Si_{1-y}Ge_y$ buffer layer. The universal mobility curve for electrons in Si [49] is depicted with a solid line. The dotted line represents an enhancement ratio of 1.7. The lower figure presents data for Ge compositions in the range $0.2 \leq y \leq 0.4$ and compares it again to the universal mobility curve (solid) and to the same curve multiplied by 2.0.

Fig. 6 shows the mobility enhancement ratio for holes as a function of the Ge content of the $Si_{1-y}Ge_y$ buffer layer. The figure compares experimental data from Stanford University [50], MIT [51], IBM [30, 31, 32], Hitachi [33], Toshiba [36, 39, 46, 47] to Monte Carlo calculations from Oberhuber et al. [52] and Bufler [53]. As can be seen the enhancement of the hole mobility increases gradually with the Ge content y for $y \leq 0.4$.

The hole mobility enhancement is observed in a wide range of effective fields. Fig. 7 summarizes selected data from IITKGP [54], MIT [25, 51], IBM [31, 32], Hitachi [33], Toshiba [39, 46, 47, 48, 55], for the effective hole mobility in strained Si as a function of the effective field. The universal mobility curve for holes in Si [49] is depicted with solid line. The dotted line represents an enhancement ratio of 2.0.

4 MODELING AND SIMULATION

To enable predictive simulations using Technology CAD (TCAD) tools a reliable set of models for the Si/SiGe material system is required. Such set has to include models for the band structure parameters and deformation potentials. Pseudopotential calculations have been reported in [56, 57]. The transport properties of strained Si or SiGe layers have

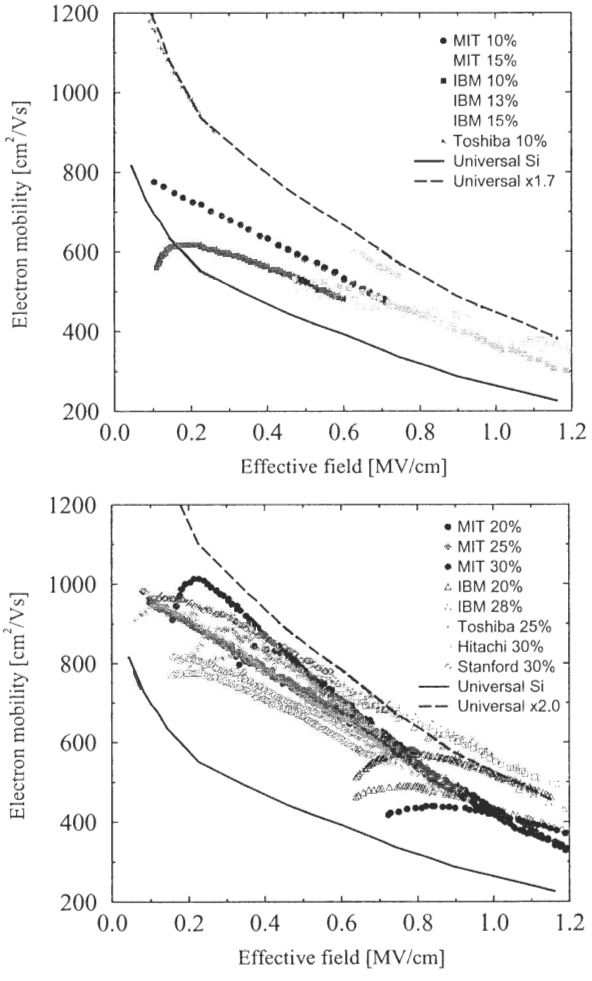

Figure 5: Effective electron mobility in strained Si as a function of the effective field for Ge content $y \leq 0.15$ (upper figure) and $0.2 \leq y \leq 0.4$ (lower figure) in the $Si_{1-y}Ge_y$ buffer layer.

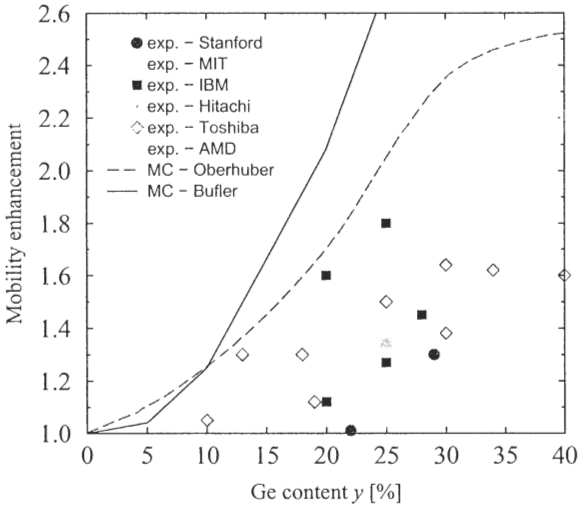

Figure 6: Mobility enhancement ratio for holes as a function of the Ge content y in the $Si_{1-y}Ge_y$ buffer layer.

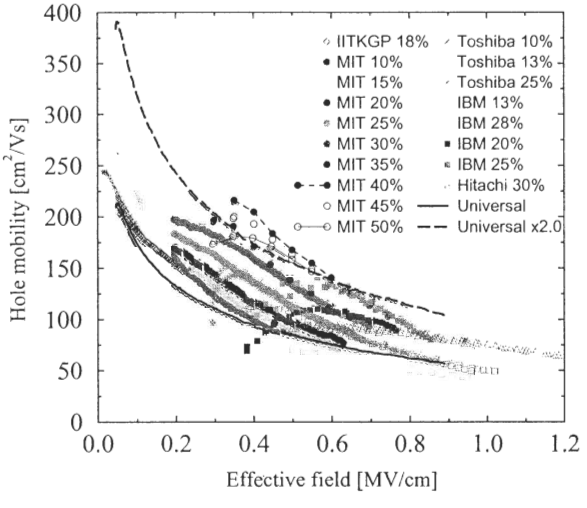

Figure 7: Effective hole mobility in strained Si as a function of the effective field for different Ge contents in the $Si_{1-y}Ge_y$ buffer layer.

been theoretically investigated using Monte Carlo calculations [40, 43, 58, 59, 60] or near equilibrium solutions to the Boltzmann equation [56]. A comprehensive set of strain-dependent models for parameters such as the low-field, high-field and the surface mobility, energy relaxation time and carrier life times for Technology CAD purposes is yet to be developed. Possible approaches are to further use analytical models [61] or tabulated Monte Carlo data in a device simulator [62]. Strain effects on the device characteristics can be most comprehensively studied by full Monte Carlo device simulation [63], however, at the expense of increased CPU-time requirements as compared to conventional TCAD simulation [64].

5 CONCLUSION

This work reviews carrier transport in strained Si CMOSFETs. Device performance is increased due to enhancement of both electron and hole mobilities compared to conventional Si MOSFETs. Improvements by factors of more than two have been reported. TCAD simulation tools need correct models of the strained Si/SiGe material system, especially with respect to carrier transport. Experimental data remain a basic input for verification of analytical TCAD models. However, Monte Carlo simulation data with confirmed accuracy can deliver information which is still experimentally missing.

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