



The state-of-the-art in simulation for optimization of SiGe-HBTs

V. Palankovski*, S. Selberherr

Institute for Microelectronics, Technical University Vienna, Gusshausstrasse 27-29, A-1040 Vienna, Austria

Abstract

We present the state-of-the-art in simulation for industrial application of heterostructure devices based on the SiGe/Si material system. The work includes a detailed comparison of device simulators and current transport models to be used, and addresses critical modeling issues. Results from two-dimensional hydrodynamic analyses of SiGe-heterojunction bipolar transistors (HBTs) with MINIMOS-NT are presented in good agreement with measured data. The examples are chosen to demonstrate technologically important issues which can be addressed and solved by device simulation.

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1. Introduction

SiGe-heterojunction bipolar transistors (HBTs) progressively replace III–V devices for their typical applications, such as low noise amplifiers and frequency dividers up to 99 GHz [1], and are considered essential for 40 Gb/s optical communication systems. Values of 380 GHz V for $f_T \times BV_{CE0}$ and ring oscillator delays of 4.3 ps have been achieved [2]. Transit frequencies, f_T , of 288 GHz [3] and maximum oscillation frequencies, f_{max} , of 285 GHz [4] were recently reported. The devices are fully compatible with the existing state-of-the-art 0.13 μm CMOS technology [4,5]. Digital application-specific integrated circuits (ASICs) are combined with SiGe-HBT circuits in the so-called SiGe BiCMOS technology and are in volume production.

Several questions during device fabrication, such as performance optimization and process control, can be addressed by simulation. The choice of a given simulation tool or a combination of tools depends to a larger extent on the complexity of the particular task, on the desired accuracy of the problem solution, and on the available human, computer, and time resources.

Optimization of geometry, doping, materials and material composition profiles targets at high power, high breakdown voltage, high speed (high f_T , f_{max}), low leakage, low noise, and low power consumption. This is a challenging task that can be significantly supported by device modeling.

We present a methodology for characterization and optimization of SiGe-HBTs. It involves two-dimensional process and device simulation calibration and automated optimization. The simulation results show very good agreement with experimental data. In particular, we perform an optimization of the collector doping for specific requirements (high speed or high breakdown voltage).

* Corresponding author. Tel.: +43-1-58801-36017;

fax: +43-1-58801-36099.

E-mail address: palankovski@iue.tuwien.ac.at (V. Palankovski).

2. Device simulators

The continuously increasing computational power of computer systems allows the use of TCAD tools on a very large scale. Several commercial device simulators, e.g. [6–11], company-developed simulators, e.g. [12,13], and University developed simulators, e.g. [14–19], claim the capability to handle SiGe devices. These simulators differ considerably in dimensionality (one-, quasi-two-, two-, quasi-three-, or three-dimensional), in the choice of carrier transport model (drift–diffusion, energy-transport, or Monte Carlo statistical solution of the Boltzmann equation), and in the capability of including electrothermal effects. The drift–diffusion transport model [20] is by now the most popular model used for device simulation. With down-scaling feature sizes, non-local effects become more pronounced and must be accounted for by applying an energy-transport or hydrodynamic transport model [21]. During the last two decades Monte Carlo methods for solving the Boltzmann transport equation have been developed [22] and applied for device simulation [23,24]. However, reduction of computational time is still an issue and, therefore, Monte Carlo device simulation is still not feasible for industrial application on every day basis. An approach to preserve accuracy at lower computational cost is to calibrate lower order transport parameters to Monte Carlo simulation data.

In addition, quantum mechanical effects are often neglected or accounted for by models for quantum corrections [25,26], since solving the Schrödinger or the Wigner equation is extremely expensive in terms of computational resources.

A common drawback is the limited feedback from technological state-of-the-art process development to simulator development. The quality of the physical models can be questioned as the model parameters for SiGe are often simply inherited from parameters for silicon. Critical issues concerning simulation of heterostructures are frequently not considered, such as interface modeling at heterojunctions and at silicon/poly-silicon interfaces. Hydrodynamic and high-field effects, such as carrier energy relaxation, impact ionization, and self-heating effects, are often ignored.

The two-dimensional device simulator PISCES [14], developed at Stanford University, incorporates modeling capabilities for SiGe-based devices, e.g. silicon/poly-silicon interface. One of its versions,

PISCES-HB, includes harmonic balance for large signal simulation.

The device simulator MEDICI from Synopsis [11], which is also based on PISCES, offers simulation features for SiGe/Si HBTs. Advantages of this simulator are hydrodynamic simulation capabilities and the rigorous approach to generation/recombination processes. In addition, it includes a module treating anisotropic material properties. This simulator has weaknesses in the capability of mixed-mode device/circuit simulation.

At the quantum level, among others, a one-dimensional Schrödinger–Poisson solver NEMO [13], based on non-equilibrium Green’s functions, is offered for sub-0.1 μm SiGe structures.

The two- and three-dimensional device simulator DESSIS from ISE [9] has demonstrated a rigorous approach to semiconductor physics modeling. Some critical issues, such as extensive trap modeling, are solved.

Quasi-two-dimensional approaches using a simplified one-dimensional current equation are demonstrated, among others, by BIPOLE3 from BIPSIM [8] which additionally features good models for poly-silicon.

The two-dimensional Blaze from Silvaco [7] has capabilities of simulation of heterostructure devices. Simulations of SiGe-HBTs were announced, based on a simulator originally developed at the University of Ilmenau, PROSA [19]. In the latter no material interfaces are considered.

Several good optimization results for SiGe-HBTs were achieved with another University developed simulator, SCORPIO [27].

Previous experience gained in the area of III-V HBT simulation which lead to successful results [28] was a prerequisite to use MINIMOS-NT [29] also for simulation of SiGe-HBTs.

Table 1 summarizes features of SiGe device simulators discussed in this paper.

3. Critical issues of modeling SiGe devices

Our three-dimensional device simulator MINIMOS-NT can deal with different complex structures and materials, such as SiGe and various III–V binary and ternary compounds, with arbitrary material composition profiles in a wide temperature range.

Table 1
Comparison of different device simulators

Simulator	Dimension	Model	Features
NEMO	1D		Schrödinger–Poisson solver
BIPOLE	Quasi-2D	DD	Poly-silicon model
ATLAS	2D	DD, ET	TE heterojunction model
APSYS	2D	HD	Optical, interfaces
GALENE	2D	DD, HD	Rigorous transport modeling
PISCES	2D	DD, ET	Poly-silicon model
PISCES-HB	2D	DD	Harmonic balance
MEDICI	2D	DD, HD	Anisotropic properties, TFE model
FIELDAY	2D, 3D	DD	Electrothermal
MINIMOS	2D, 3D	DD, HD	See Section 3
DESSIS	2D, 3D	DD, HD	Trap modeling, TFE model

DD: drift–diffusion, ET: energy-transport, HD: hydrodynamic, TE: thermionic emission, TFE: thermionic field emission.

Considering the nature of SiGe devices which include abrupt junctions, heterointerface modeling is a key issue. Thermionic emission and field emission effects critically determine the current transport parallel and perpendicular to the heterointerfaces. A distinction between majority and minority carriers is made for the low field mobility based on Monte Carlo simulation results verified with experimental data.

All the important physical effects, such as band gap narrowing, anisotropic electron minority mobility in strained SiGe, Shockley–Read–Hall recombination, surface and Auger recombination, and impact ionization are taken into account. SiGe is known to have a reduced heat conductivity in comparison to silicon [30]. Self-heating effects are accounted for by solving the lattice heat flow equation self-consistently with the energy-transport equations.

Advanced device simulation allows a precise physics-based extraction of small-signal parameters. Measured bias-dependent S -parameters serve as a valuable source of information when compared at different bias points to simulated S -parameters from a device simulator, such as MINIMOS-NT. This procedure reflects the full RF-information contained in the S -parameters and allows process control beyond the comparison of DC-quantities.

4. Device fabrication and process calibration

The influence of the selectively-implanted-collector (SIC) implant on device performance was studied both

experimentally and by means of process simulation using DIOS [9], followed by two-dimensional device simulation. The double-base SiGe-HBT test-structures with emitter areas of $6 \mu\text{m} \times 0.8 \mu\text{m}$ are epitaxially grown by a chemical vapor deposition process. An implanted n-well, similar to the one used in the standard CMOS technology, is used. The buried layer is connected to a sinker to conduct the electron current from the buried layer to the collector contact. The base consists of an intrinsic base (below the emitter window) and an extrinsic base. The germanium content has a triangular shape. The base–emitter junction is formed by rapid thermal processing which causes out-diffusion of arsenic from the poly-silicon emitter layer into the crystalline silicon.

The process simulation starts from the blank wafer to the final device and reflects real device fabrication as accurately as possible. The implant profiles as well as annealing steps were calibrated to one-dimensional SIMS profiles. The simulated device structure with the phosphorus SIC implant are shown in Fig. 1. To save computational resources the simulation domain covers only one half of the real device which is symmetric and the collector–sinker is not included in the structure. This allows to use a very precise simulation grid in areas of interest (Fig. 2).

In order to obtain an optimal device, four structures have been investigated. The only process step in which the four HBTs (hereafter referred to as Dev. 1, Dev. 2, Dev. 3, Dev. 4) differ is the combination of energy and dose used for SIC implants, as summarized in Table 2. The phosphorus doping profiles in vertical cuts under

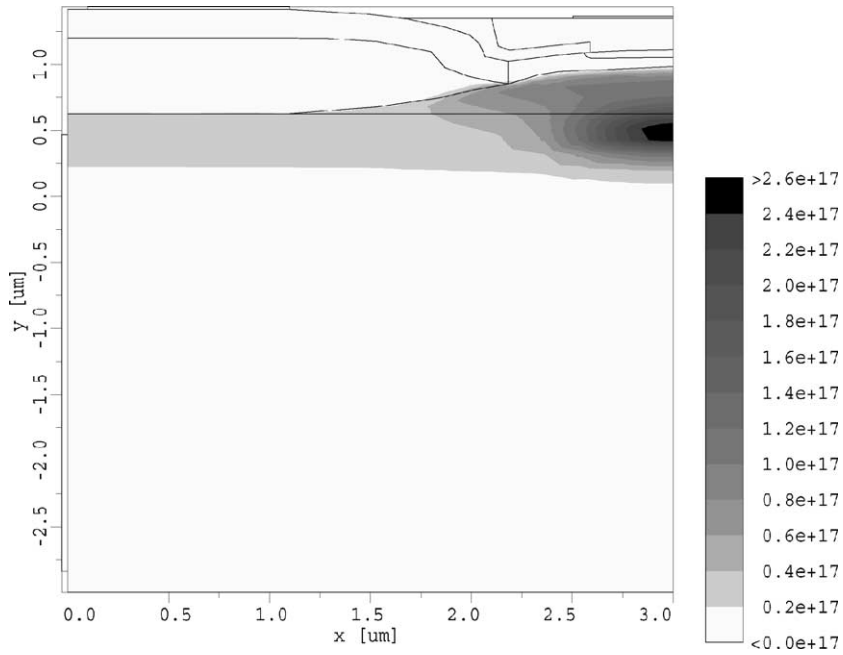


Fig. 1. Simulated device structure and phosphorus collector implant (cm³).

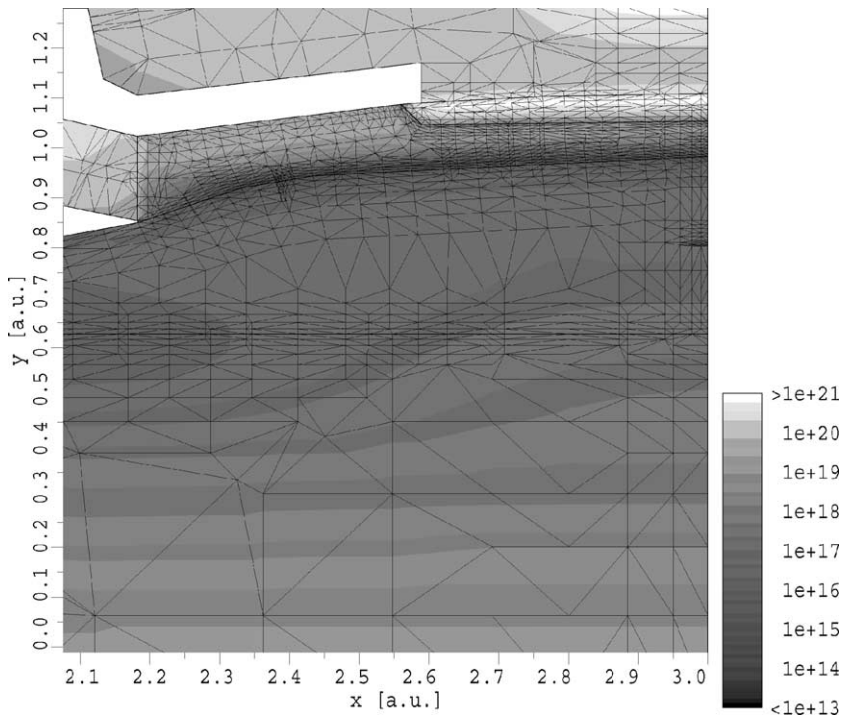


Fig. 2. Gridding example from the active device area.

Table 2
Summary of key process and device parameters

Device	Energy (keV)	Dose (cm ⁻²)	f_T (GHz)	BV_{CE0} (V)	$f_T \times BV_{CE0}$ (GHz V)
Dev. 1	480	7e12	32	4.0	128
Dev. 2	480	3e13	40	3.7	148
Dev. 3	300	7e12	33	3.1	102
Dev. 4	300	3e13	42	2.3	97

the emitter windows of the four devices as resulting from process simulation are shown in Fig. 3. A comparative Monte Carlo simulation of ion implanta-

tion [31] of phosphorus in silicon and SiGe was performed to check the accuracy of the process simulation in respect to SiGe (see Fig. 4).

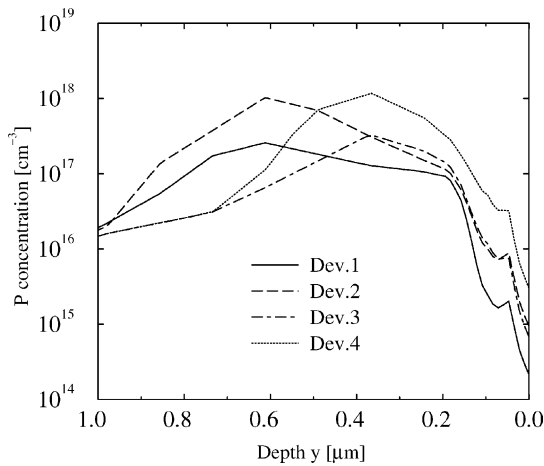


Fig. 3. Phosphorus doping profile under the emitter contact for all four devices resulting from process simulation.

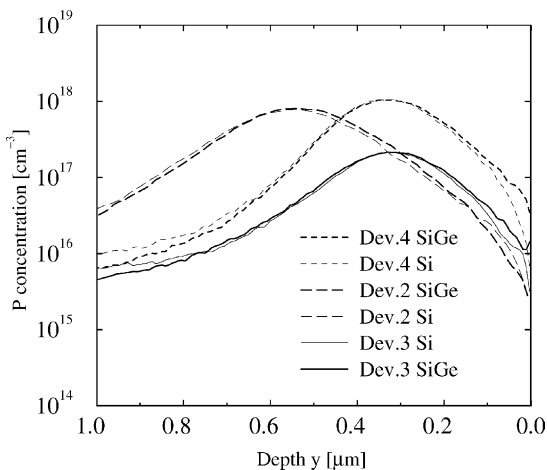


Fig. 4. Comparative simulation of Monte Carlo ion implantation of phosphorus in Si and SiGe.

5. Device simulation example

The physical models in MINIMOS-NT are well calibrated [32]. The same is true for DESSIS, used for comparison. Both device simulators correctly reproduce the measured forward Gummel plot at 300 K (see Fig. 5) with default models. The slight increase of collector current I_C with dose and energy at high bias is due to the differences in the base push-out effect. We use small-signal AC-analysis to extract f_T .

However, as can be seen in Figs. 6 and 7, both DESSIS and MINIMOS-NT failed to explain the experimentally observed similarity in peak f_T for Dev. 1 and Dev. 3 and, respectively, for Dev. 2 and Dev. 4. This again turned our attention to the SIC implant. An automated device calibration with our

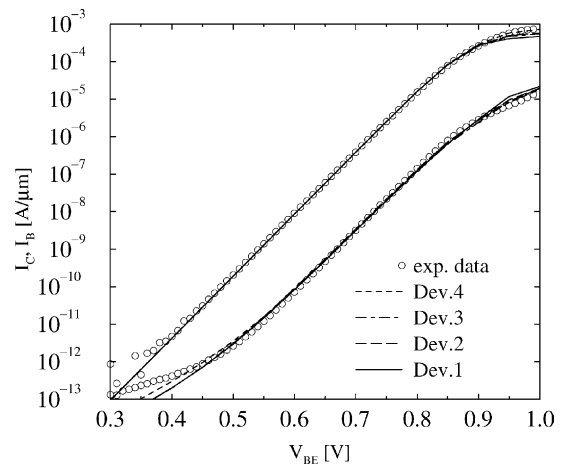


Fig. 5. Forward Gummel plots at $V_{CB} = 0$ V. Comparison between measurement and simulation.

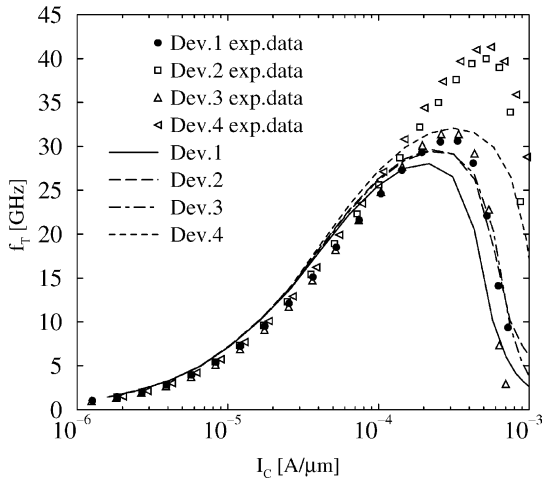


Fig. 6. f_T vs. I_C at $V_{CE} = 1.5$ V. Comparison between measurement and drift-diffusion simulation with DESSIS.

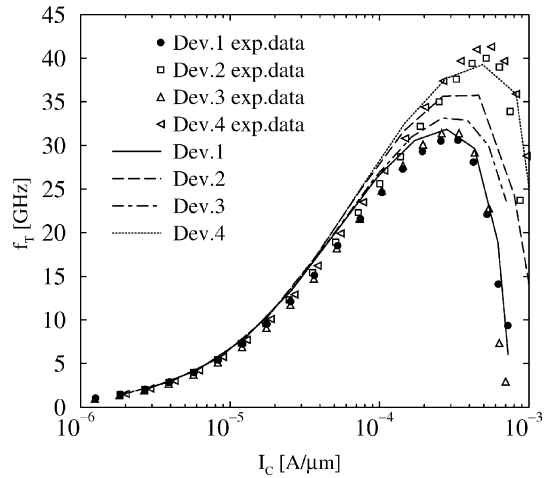


Fig. 8. f_T vs. I_C at $V_{CE} = 1.5$ V. Comparison between measurement and hydrodynamic simulation with MINIMOS-NT.

TCAD framework [33] was performed. It turned out that 50% more phosphorus in the collector of the two low-dose devices (Dev. 1 and Dev. 2) already gives an acceptable qualitative agreement.

It is known that with shrinking device dimensions non-local effects, such as velocity overshoot, become more pronounced. Neglecting these effects can be a reason for underestimating f_T [34]. For that purpose, we performed simulations with the hydrodynamic transport model to improve quantitatively the results

(see Fig. 8). Fig. 9 shows the velocity overshoot over the greater part of the base region which is about twice the saturation velocity limit in the drift-diffusion case (10^7 cm/s). This correlates to the higher electron energy (see Fig. 10) in the collector and explains the increase of f_T in comparison to drift-diffusion simulations (see Figs. 6 and 7). The good agreement at low currents is very important since HBTs typically operate at much lower frequencies than at the maximum f_T . The simulations prove that in this range

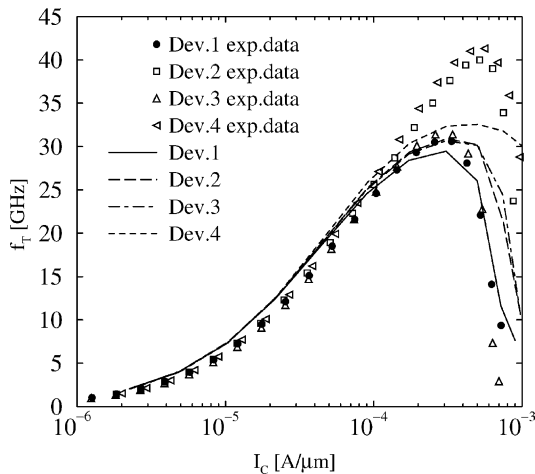


Fig. 7. f_T vs. I_C at $V_{CE} = 1.5$ V. Comparison between measurement and drift-diffusion simulation with MINIMOS-NT.

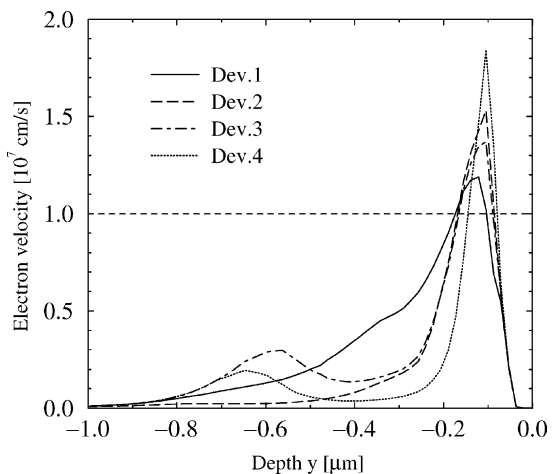


Fig. 9. Electron velocity overshoot in the base-collector space charge region at $V_{CE} = V_{BE} = 0.88$ V.

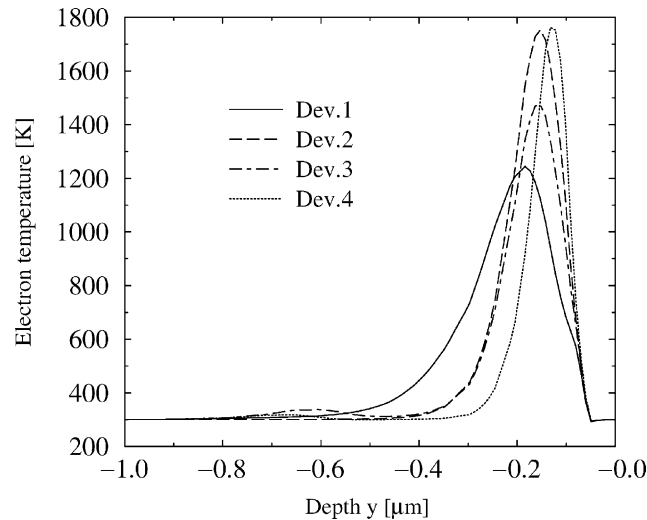


Fig. 10. Electron temperature distribution in the four simulated devices at $V_{CE} = V_{BE} = 0.88$ V.

optimizations of the SIC implant do not have an influence on f_T , i.e. the base–emitter capacitance and not the base–collector capacitance is dominating. The maximum f_T was found to have a stronger dependence on the dose than on the energy of the implants.

Furthermore, the important figure of merit $BV_{CE0} \times f_T$ (see Table 2) reaches a maximum for high SIC implant energies (deep implant) and high SIC doses. We found that the higher f_T for high-dose/low-energy SIC implants is due to a smaller base width and a delayed onset of the base push-out effect due to the higher collector doping.

6. Conclusion

A brief overview of the state-of-the-art of simulation tools for SiGe-HBTs has been given. We have presented experiments and simulations of SiGe-HBTs. Good agreement was achieved both with experimental DC-results (forward and output characteristics) and with high-frequency data. With an increasing number of stable and reliable heterostructure technologies available, a meaningful comparison between simulation results and statistically analyzed data is possible and delivers on the one hand side model verification, and on the other hand side valuable process information.

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References

- [1] J. Böck, H. Schäfer, H. Knapp, D. Zöschg, K. Aufinger, M. Wurzer, S. Boguth, M. Rest, R. Schreiter, R. Stengl, T. Meister, Sub 5 ps SiGe Bipolar Technology, in: *IEDM Tech. Dig.*, 2002, pp. 763–766.
- [2] B. Heinemann, H. Rücker, R. Barth, J. Bauer, D. Bolze, E. Bugiel, J. Drews, K.-E. Ehwald, T. Grabolla, U. Haak, W. Höppner, D. Knoll, D. Krüger, B. Kuck, R. Kurps, M. Marschmeyer, H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, W. Winkler, D. Wolansky, H.-E. Wulf, Y. Yamamoto, P. Zaumseil, Novel Collector Design for High-Speed SiGe:C HBTs, in: *IEDM Tech. Dig.*, 2002, pp. 775–778.
- [3] J.-S. Rieh, B. Jagannathan, H. Chen, K. Schonenberg, D. Angell, A. Chinthakindi, J. Florkey, F. Golan, D. Greenberg, S.-J. Jeng, M. Khater, F. Pagette, C. Schnabel, P. Smith, A. Stricker, K. Volant, D. Ahlgren, G. Freeman, K. Stein, S. Subbanna, SiGe HBTs with cut-off Frequency Near 300 GHz, in: *IEDM Tech. Dig.*, 2002, pp. 771–774.
- [4] B. Jagannathan, M. Khater, F. Pagette, J.S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D.R. Greenberg, R. Groves, S.J. Jeng, J. Johnson, E. Mengistu, K.T. Schonenberg, C.M. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K.

- Stein, S. Subbanna, Self-aligned SiGe NPN transistors with 285 GHz f_{\max} and 207 GHz f_T in a manufacturable technology, *IEEE Electron. Device Lett.* 23 (5) (2002) 258–260.
- [5] T. Hashimoto, Y. Nonaka, T. Saito, K. Sasahara, T. Tominari, K. Sakai, K. Tokunaga, T. Fujiwara, S. Wada, T. Udo, T. Jinbo, K. Washio, H. Hosoe, Integration of a 0.13- μm CMOS and a High Performance Self-Aligned SiGe HBT Featuring Low Base Resistance, in: *IEDM Tech. Dig.*, 2002, pp. 779–782.
- [6] APSYS, <http://www.crosslight.com/downloads/downloads.html>.
- [7] ATLAS/Blaze, <http://www.silvaco.com/products/vwv/atlas/atlas/atlasbr.html>.
- [8] BIPOLE3, <http://www.bipsim.com/mainframe.html>.
- [9] DESSIS and DIOS, <http://www.ise.com/products/index.html>.
- [10] G-PISCES-2B, <http://www.gateway-modeling.com/products.htm>.
- [11] MEDICI, <http://www.synopsys.com/products/avmrg/device-simds.html>.
- [12] E. Buturla, P. Cottrell, B. Grossman, K. Salsburg, Finite-Element Analysis of Semiconductor Devices: The FIELDAY Program, <http://www.research.ibm.com/journal/rd/441/buturla.pdf>.
- [13] NEMO, <http://www.cfdrc.com/nemo/>.
- [14] PISCES-ET, <http://www-tcad.stanford.edu/tcad.html>.
- [15] FLOODS and FLOOPS, <http://www.tec.u.edu/ooxs/>.
- [16] C. Jungemann, B. Neinhüs, B. Meinerzhagen, Full-band Monte Carlo device simulation of a SiGe/Si HBT with a realistic Ge profile, *IEICE Trans. Electron.* E83-C (8) (2000) 1228–1234.
- [17] DEVICE, <http://www.uv.ruhr-uni-bochum.de/>.
- [18] Nextnano3, <http://www.webplexity.de/nextnano3.php>.
- [19] J. Geßner, F. Schwierz, H. Mau, D. Nuernbergk, M. Roßberg, D. Schipanski, Simulation of the frequency limits of SiGe HBTs, in: *Proceedings International Conference on Modeling and Simulation of Microsystems, Puerto Rico, 1999*, pp. 407–410.
- [20] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*, Springer, Wien, New York, 1984.
- [21] T. Grasser, T. Tang, H. Kosina, S. Selberherr, Energy-transport models for semiconductor device simulation, *Proc. IEEE* 91 (2) (2003) 251–274.
- [22] C. Jungemann, B. Meinerzhagen, *Hierarchical Device Simulation: The Monte-Carlo Perspective*, Springer, Wien, New York, 2003.
- [23] H. Kosina, M. Nedjalkov, S. Selberherr, Theory of the Monte Carlo method for semiconductor device simulation, *IEEE Trans. Electron. Devices* 47 (10) (2000) 1898–1908.
- [24] M. Fischetti, S. Laux, Performance degradation of small silicon devices caused by long-range Coulomb interactions, *Appl. Phys. Lett.* 76 (16) (2000) 2277–2279.
- [25] W. Hänsch, T. Vogelsang, R. Kircher, M. Orlowski, Carrier transport near the Si–SiO₂ interface of a MOSFET, *Solid State Electron.* 32 (10) (1989) 839–849.
- [26] K. Dragosits, V. Palankovski, S. Selberherr, Two-dimensional modeling of quantum mechanical effects in ultra-short CMOS devices, in: N. Mastorakis, V. Kluev, D. Koruga (Eds.), *Proceedings of the International Conference on Nanoelectronics and Electromagnetic Compatibility, Advances in Simulation, Systems Theory and Systems Engineering*, WSEAS Press, 2002, pp. 113–116.
- [27] D. Richey, J. Cressler, A. Joseph, Scaling issues and Ge profile optimization in advanced UHV/CVD SiGe HBT's, *IEEE Trans. Electron. Devices* 44 (3) (1997) 431–440.
- [28] V. Palankovski, R. Schultheis, S. Selberherr, Simulation of power heterojunction bipolar transistors on gallium arsenide, *IEEE Trans. Electron. Devices* 48 (6) (2001) 1264–1269.
- [29] MINIMOS-NT, <http://www.iue.tuwien.ac.at/software/minimos-nt>.
- [30] V. Palankovski, S. Selberherr, Thermal models for semiconductor device simulation, in: *Proceedings of the European Conference on High Temperature Electronics, Berlin, 1999*, pp. 25–28.
- [31] A. Hössinger, S. Selberherr, Accurate three-dimensional simulation of damage caused by ion implantation, in: *Proceedings of the International Conference on Modeling and Simulation of Microsystems, Puerto Rico, 1999*, pp. 363–366.
- [32] S. Selberherr, W. Hänsch, M. Seavey, J. Slotboom, The evolution of the MINIMOS mobility model, *Solid-State Electron.* 33 (11) (1990) 1425–1436.
- [33] T. Grasser, R. Strasser, M. Knaipp, K. Tsuneno, H. Masuda, S. Selberherr, Device simulator calibration for quartermicron CMOS devices, in: K. De Meyer, S. Biesemans (Eds.), *Proceedings of the SISPAD, Leuven, Springer, Wien, New York, 1998*, pp. 93–96.
- [34] C. Jungemann, B. Neinhüs, B. Meinerzhagen, Comparative study of electron transit times evaluated by DD, HD, and MC device simulation for a SiGe HBT, *IEEE Trans. Electron. Devices* 48 (10) (2001) 2216–2220.