Feature-Scale Process Simulation and Accurate Capacitance Extraction for the Backend of a 100-nm Aluminum/TEOS Process

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***Abstract*—One of the challenges that technology computer-aided design must meet currently is the analysis of the performance of groups of components, interconnects, and, generally speaking, large parts of the IC. This enables predictions that the simulation of single components cannot achieve. In this paper, we focus on the simulation of backend processes, interconnect capacitances, and time delays. The simulation flows start from the blank wafer surface and result in device information for the circuit designer usable from within SPICE. In order to join topography and backend simulations, deposition, etching, and chemical mechanical planarization processes in the various metal lines are used to build up the backend stack, starting from the flat wafer surface. Depending on metal combination, line-to-line space, and line width, thousands of simulations are required whose results are stored in a database. Finally, we present simulation results for the backend of a 100–nm process, where the influence of void formation between metal lines profoundly impacts the performance of the whole interconnect stack, consisting of aluminum metal lines, and titanium nitride local interconnects. Scanning electron microscope images of test structures are compared to topography simulations, and very good agreement is found. Moreover, charge-based capacitance measurements were carried out to validate the capacitance extraction, and it was found that the error is smaller than four percent. These simulations assist the consistent fabrication of voids, which is economically advantageous compared to low-κ materials, which suffer from integration problems.**

***Index Terms*—Capacitance extraction, chemical vapor deposition (CVD), dry etching, integrated circuit interconnections, level-set method, topography simulation.**

I. INTRODUCTION

INTERCONNECTS are becoming increasingly important as the shrinking of semiconductor technologies continues, since the timing delays due to metal lines contribute more to the overall delay. Therefore it is imperative for predictive technology computer-aided design (TCAD) applications that capacitance and resistance of interconnect lines are modeled as accurately as possible.

Most resistance and capacitance extraction (RCX) tools assume rectangular metal profiles, either planar or conformal dielectrics, and use simplistic void models. Even if the metal slope is modeled, it is mostly assumed constant and independent of space. While these idealizing assumptions may be sufficient for past technologies, they are insufficient for today's technologies like the 100–nm process considered in Section V, where interconnects show a number of special features which are nowhere close to ideal.

In order to model capacitance correctly, one has to know the metal profile, e.g., bottom and top critical dimensions and metal slope, the profile of the deposited layer with and without chemical mechanical planarization (CMP), and the profile of the void, in case it is formed. Generally, these three profiles depend heavily on deposition process conditions, metal thickness, and line-to-line space, and less strongly on metal width.

In this paper, we present the results of a rigorous simulation approach. In order to provide predictive simulations of the overall capacitance, the shapes and positions of the voids must be known precisely. Here, feature-scale topography simulations serve as input to the subsequent capacitance extraction. The entirety of simulations and extracted capacitances characterize a specific technology, and are made accessible to the circuit designer via a database.

II. ELSA SIMULATOR AND ITS LEVEL-SET ALGORITHM

Every feature-scale topography simulation must take into account the following three main steps. First, the transport of particles in the boundary layer above the wafer must be simulated. This can happen in the radiosity or diffusion regime. Second, the fluxes of particles at the wafer surface found in the previous step determine the chemical reactions that take place at the wafer surface. Third, the surface of the substrate moves according to the fluxes found in the second steps.

The enhanced level-set applications (ELSA) simulator consists of a level-set module [1]–[3], a transport module, including the two cases of radiosity and diffusion, and a surface reaction module. Hence, the simulation flow can be summarized as follows:

1) construct the initial level-set function as the signed distance function;
2) perform a radiosity or diffusion time step;
3) allow the chemical reactions to yield the speed function on the surface;
4) construct signed distance function, extend the speed function to the whole narrow band, and determine the new narrow band;
5) perform a finite difference step in narrow band; go to step 2 until a certain time or layer thickness is reached;
6) extract the final surface.

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The simulation stops when a prescribed time is reached or when a layer of prescribed thickness has been deposited. In this section, we focus on the third step, i.e., the level-set algorithm used.

A. Narrow Banding and Extending the Speed Function

The idea leading to fast level-set algorithms stems from observing that only the values of the level-set function near its zero level-set are essential, and, thus, only the values at the grid points in a narrow band around the zero level-set must be calculated. As the zero level-set moves, the signed distance function in the narrow band must be maintained in order to ensure good numeric accuracy. The usual approach to determining the current active narrow band points is to reinitialize whenever the zero level-set reaches the boundary of the narrow band. Reinitialization, however, introduces errors and hence it is generally avoided. This level-set algorithm traces the active narrow band points dynamically in each time step at no additional computational cost.

Combining narrow banding and extending the speed function into a single algorithm provides several benefits. First, the level-set function is retained as the signed distance function throughout the simulation, which assures good accuracy until the end of the simulation. Second, narrow banding reduces the number of active points that have to be updated from $O(n^2)$ to $O(n)$ in two dimensions, and from $O(n^3)$ to $O(n^2)$ in three dimensions. By retaining the signed distance function, the width of the narrow band can be kept down to two points on each side without decreasing accuracy. Third, time-consuming calculations (cf. [4]) are reduced to a minimum by intertwining the computations necessary for narrow banding and extending the speed function. Furthermore, the width of the narrow band can be adjusted in this algorithm.

The algorithm works as follows. First, the initial points near the zero level-set (where the speed function is known) and the neighboring trial points, are determined. The main loop is checked if there is still a trial point to be considered in the narrow band. All trial points are stored in a heap ordered by their distance to the zero level-set. If there is a point to be considered, its distance is approximated, its extension speed is calculated, and its neighbors are updated accordingly. Finally, after the main loop, bookkeeping information for the narrow band points is updated using distance information just computed.

The detailed steps are the following, where several auxiliary functions are used. Concerning the data structures, the information about the level-set grid, the distance function, the extended speed function, and the tags for the fast marching method are stored in arrays. The trial points are stored in a heap.

1) First, find the grid points whose speed function values are initially known. These values are computed in the physical simulation step and translated to the grid. Then compute the distance for the initial points, tag them as known, and initialize the corresponding grid points of the speed function. Find the trial points, which are the neighbors of the initially known points, and compute their tentative distance values. All other points are far points.

2) While there are trial points, do the following.
    a) Remove the first point from the heap and call it a. It has the smallest distance from the zero level-set of all points in the heap.
    b) If narrow banding is used and the maximum width of the narrow band is smaller than the distance of a, return from the loop.
    c) Mark a as known.
    d) For all neighbors b of a, do the following:
        i.) If b is a far point, recompute its distance and speed function values and mark it as a trial point.
        ii.) If b is a trial point, recompute its tentative distance and speed function values, unless it was computed in the previous step.

3) If narrow banding shall be used, set the distance values of all points, which are not marked as known, to the width of the narrow band. Set the sign of the distance function.

4) Finally, return two objects, namely the grid containing the new signed distance function, and the grid containing the extended speed function.

A second-order space convex finite difference scheme [1] is used for updating the level-set grid. The main level-set function must perform the bookkeeping for the narrow band considering the old narrow band from the previous iteration and the new narrow band. The points which are outside the old narrow band but inside the current narrow band are initialized to the signed distance function just computed.

We close this section with a remark on the computed expense. Moving a curve $(d := 2)$ or a surface $(d := 3)$ in d dimensions demands a computational expense of $O(n^d)$ since each point of the surface must be touched at least once. The above algorithm for tracking boundaries is optimal in the sense that it requires an effort of $O(n^d)$, due to using narrow banding and a fast marching algorithm.

B. Surface Coarsening

Because of the large number of topography simulations required to characterize a backend technology (cf. Section IV), simulation time cannot be neglected. When using radiosity models for simulating the transport of particles above the wafer, two operations consume the most part of the computation time. The first operation is determining the visibility between all surface elements, which requires $\binom{n}{2}$ visibility tests, where n denotes the number of surface elements extracted from the level-set grid. The second operation is solving a certain system of linear equations, which leads to calculating the inverse of a dense $n^2 \times n^2$ matrix.

Hence, it is mandatory to keep the number of surface elements as low as possible. Yet high resolution is needed, e.g., near the trench opening and the bottom of the trench. One approach is to devise a refinement and coarsening strategy for unstructured grids at the level of the level-set implementation and the algorithms working on it. This, however, complicates the fast marching algorithm necessary for extending the speed function. In this paper, a different approach was taken by coarsening the surfaces after they have been extracted from the level-set grid.

The coarsening algorithm works by walking down the list of surface elements extracted as the zero level-set and calculating the angle α between two neighboring surface elements. Whenever $|\pi - \alpha|$ is below a certain threshold value of a few degrees, the neighboring elements are coalesced into one. After one sweep through the list, the algorithm can be reapplied for further coarsening. After k coarsening sweeps, at most 2^k surface elements are coalesced into one. The resulting longer surface elements are used for the radiosity calculation, after which the fluxes are translated back from the coarsened elements to the original ones. This is a heuristic approach and works excellently in practice.

III. Feature Scale Simulation

Having described the handling of moving boundaries in the preceding section, this section focuses on the transport of particles by radiosity and the chemical surface reactions. Starting from a plain substrate, the principal topography simulation steps are etching trenches, depositing thin films, and CMP (cf. Fig. 1). Finally, we outline how the single topography simulations are integrated to yield larger backend structures.

A. Transport by Radiosity and Luminescent Reflection

A formulation of the radiosity method for the case of luminescent reflection, pertaining to low energy particles [1], will be used in the deposition simulations in Section III. The flux reaching the surface elements obtained in the surface extraction step may be written as a vector, i.e.,

$$\begin{aligned}\text{Flux} &= \beta_0 I_S + \beta \Psi L I_R \\ &= \frac{\beta - \beta_0}{1-\beta} I_S + \frac{\beta(1-\beta_0)}{1-\beta} \underbrace{L^{-1}\left(L^{-1}-(1-\beta)\Psi\right)^{-1}}_{T:=} I_S.\end{aligned}$$

Here, I_S is the vector of fluxes coming from the sources to the surface elements, I_R is the vector of fluxes that arrive because of reflections, β_0 is the sticking coefficient for particles coming directly from the source, β the one for secondary bounces, L is the diagonal matrix containing the lengths of the surface elements, and

$$\Psi_{ij} = \frac{n_i \cdot (t_j - t_i) n_j \cdot (t_i - t_j)}{\pi |t_j - t_i|^3} [i \text{ visible } j]$$

where t_i are the centroids of the surface elements, n_i their unit normal vectors, and $[i \text{ visible } j]$ is 1 or 0 if the surface element j is visible from i or not.

The second line in the equation above is obtained from the first one, and the relationship $I_R = (1-\beta_0)I_S + (1-\beta)\Psi L I_R$ results from straightforward algebraic manipulations. In the case of multiple, low-energy species, the calculation of the visibility matrix and the inverse T only depend on topographic information and, thus, do not have to be repeated for each species.

B. Deposition

In the backend process considered, the deposited films are silicon nitride and silicon dioxide (cf. Section V). Here, the transport of particles happens in the radiosity regime and the deposition processes are governed by luminescent reflection.

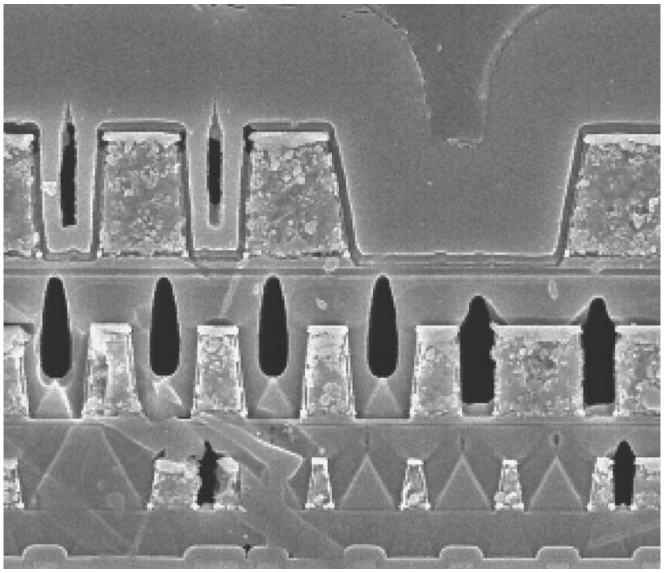

Fig. 1. SEM image of a whole backend stack comprised of three Al metals and a Ti-nitride local interconnect.

The silicon nitride films were deposited by from silane and NH_3 and were not doped. The reaction is $SiH_4 + NH_3 \rightarrow SiNH + 3H_2$ [5]. For simulation purposes this was considered the essential reaction, where a detailed model of triaminosilane condensation can be found in [6].

The silicon dioxide films were deposited by pyrolytic decomposition of in a process. In order to calculate the thickness Δd of the film deposited during a time interval of length Δt, we observe that Δd is proportional to Δt, to an Arrhenius term, and to the deposition rate R corresponding to the deposition model chosen. This implies $\Delta d = \Delta t \cdot k_e \mathrm{e}^{-E/kT} \cdot R$. Here $k_e \mathrm{e}^{-E/kT}$ is the Arrhenius term with activation energy E, absolute temperature T, and pre-exponential constant k_e, and R is the deposition rate [7].

When modeling topography processes it is generally possible to write down complicated reaction paths and list dozens of possible surface reactions. However, it is not straightforward to determine the vital reactions and their constants. Thus, it is important to reduce the possible reaction paths to an essential minimum which reproduces the observed phenomena.

C. Etching

For simulating etching of materials with different properties with respect to the etchant, a multiregion level-set algorithm was developed. The main moving boundary, namely the wafer surface, is superposed by regions with different speed functions and, hence, this extension enables the description of complicated geometries. Examples are masks on the wafer, etch stop layers, or selective etching. In these regions, the incoming fluxes are translated to the etching speed according to the different material properties.

The ion angular distribution function entering the simulation domain and the location of the ion sources are determined by the plasma. Afterwards, this information enters the feature scale simulation as physical boundary condition. The ions at the wafer surface are reflected in a specular manner in addition to a cosine law around the angle of the reflection.

In the examples, the etchant was chlorine and, thus, $Cl^{+}{}_{(g)} + S \rightarrow Cl_{(s)}$, $Si_{(s)} + 4Cl_{(s)} \rightarrow SiCl_{4(g)} + 4S$ (S denotes a surface site) was used as the dominating reaction path [8].

D. CMP

On the feature-scale level, the simulation of CMP can be performed in a straightforward manner, since the thickness of the remaining part of the layer is known. In this simulation step, the boundary is modified so that all parts above the given thickness are removed, and the remaining points are joined accordingly.

E. Integration

Simulations of single features, performed by the above steps, are duplicated using affine transformations $\mathbf{x} \mapsto A\mathbf{x} + \mathbf{b}$. For example, to arrive at the structures shown in Figs. 3–5, it is necessary to simulate the processes for a single feature including etching and subsequent deposition. The resulting boundaries are duplicated by affine transformations. At the left and right boundaries, other simulations must be performed, as there only half a trench can be considered. The results for the lefthand boundary are mirrored to yield the righthand boundary.

IV. Backend Simulation

The coordinates of the structures simulated by ELSA serve as input to a field solver. For the following simulations, we used RAPHAEL [9]. Depending on the resolution required, ELSA may yield a large number of points describing ILD and voids. Since this number of surface elements determines the number of RAPHAEL grid points, and simulation time is an important factor, a significant reduction is necessary. Otherwise, simulation times would be orders of magnitude larger than those for equivalent simplified structures. Hence, we use a surface-coarsening algorithm for reworking the output and reducing the number of points supplied to the field solver [2].

A. Capacitance Types

In order to model capacitances, we assume that a signal line is at high voltage, and surrounded by two lines on the left, two lines on the right, a plane underneath, and, if necessary, a plane above. The surrounding lines and planes are assumed to be at ground voltage. For example, an M2 signal line could be surrounded by M2 grounded lines above the M1 plane, and underneath the M3 plane. This skeleton is shown in Fig. 2.

B. Capacitance Models

Capacitance simulations are performed depending on three variables. First, they depend on metal combination, For a six-layer technology the combinations can be more than one hundred.

Second, they depend on line-to-line space. Simulations start from the minimum allowed space (e.g., 0.14 μm) and end in the range of a few microns (e.g., 6 μm). Generally, initial space increments are fine to capture strong dependence of capacitance on space and final increments are coarse to capture capacitance saturation.

Third, capacitance simulations depend on line width. Simulations start from the minimum allowed width to approximately 60 times the minimum width. Since the dependence on width is well behaved, only a few intermediate widths are usually needed.

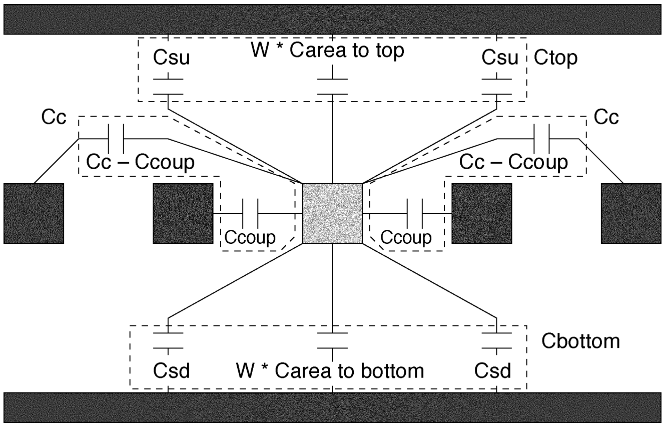

Fig. 2. Two-dimensional schematics of a signal line (middle) surrounded by grounded lines and planes. The total capacitance equals the sum of twice the coupling capacitance plus top and bottom capacitances.

C. Interfacing to Circuit Design

First, the designer instantiates a capacitance element, e.g., for an M3 line above the substrate. The designer must specify the metal name and the surrounding planes as well as metal width, length, and space. Then, the designer creates a SPICE program file. Finally, the TCAD flow reads the database and designer options, locates the capacitor of interest, interpolates or extrapolates for space and width, and replaces the capacitance instance with a numeric value for the capacitance at that node. Now, the designer can run the SPICE netlist and observe circuit performance. If timing requirements are not met, the designer changes the properties of the capacitance, e.g., makes it narrower for lower capacitance, and repeats the process.

V. Example, Simulation Results, and Discussion

As a leading example, we consider the case of M3 lines (which are the top metal lines in this example) above the M2 plane. These backend stacks are part of a 100-nm aluminum/TEOS process [cf. the scanning electron microscope (SEM) image shown in Fig. 1]. The films deposited are silicon nitride and silicon dioxide and the interconnect lines are made of aluminum. The experiments performed during development of a RAM process were performed in a LAM 9600 reactor.

The M3 lines are at 0.50 μm width and at a line-to-line space, which varies between 0.45 and 1.9 μm. Fig. 3 shows the RAPHAEL structure constructed from ELSA coordinates at minimum space. Note that at minimum space, the metal lines are vertical and voids are maximum in size. For a line-to-line space of 0.9 μm as shown in Fig. 4, the side walls are sloped and the voids considerably smaller.

Next, we build the structure at 1.5-μm space. Fig. 5 shows the corresponding RAPHAEL structure again constructed from ELSA simulation results. Note that in this case, however, metal lines have a larger slope, which duplicates the real process geometry, and voids are quite. At 1.9-μm space, the metal slope has saturated and no voids are formed.

The middle-line capacitance was simulated as described in Section IV for the above structures and compared to the charge-based capacitance measurement (CBCM). The simulations and measurements are compared in Fig. 6. Simulation results show

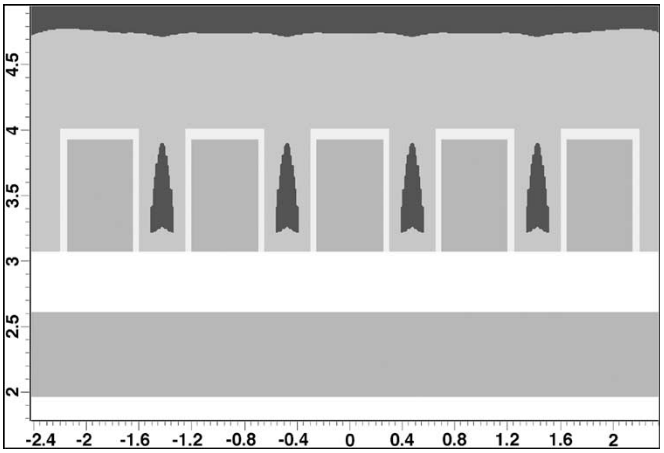

Fig. 3. M3 lines (0.5 μm top width) at a 0.45 μm space above the M2 plane. Cap oxide was deposited (thin layer surrounding M3 lines) before the top nitride (thick layer) was deposited. Void formation occurs between the lines.

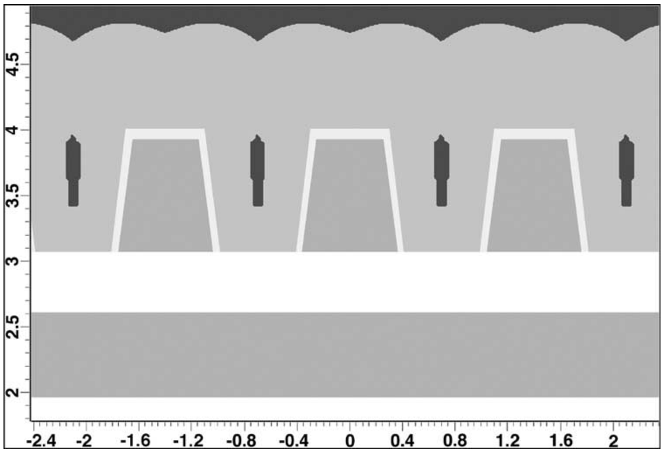

Fig. 4. M3 lines (0.5-μm top width) at 0.90-μm space above the M2 plane. The voids are smaller than in Fig. 3.

very good agreement with measurements with an error below 4%.

As a second example, we compare the capacitances extracted after silicon dioxide deposition in the M2 plane to s. Simulations were performed for line-to-line spaces of 0.3, 0.6, 1.0, and 2.0 μm. The simulated and measured capacitances are shown in Fig. 7 and again, the error is below 4%.

These examples, i.e., two-dimensional models for lines surrounded by other lines, are important since there is an abundance of cases where they appear on a chip. One of the most important cases are the last metal lines which are used as paths from one side of the chip to the other. Such an example is a time clock to out (TCO) path whose length is 22 000 μm in a 72-M chip, which is 1 cm in length. The TCO path is divided into eight portions, and each portion has a different width, and different space to adjacent lines. It is very important that this path is accurately modeled and optimized, as it is used to bin the product into a larger megahertz of operation frequency. To predict and optimized the performance of this line, accurate models are needed and this motivated this paper.

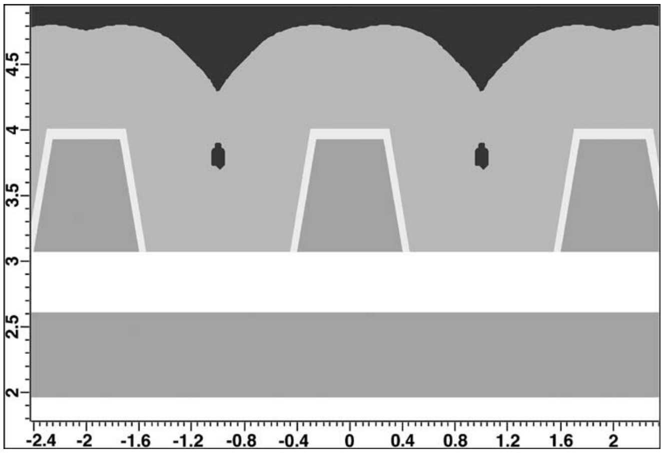

Fig. 5. M3 lines (0.5-μm top width) at 1.50-μm space above the M2 plane. In this case, the voids formed are quite small.

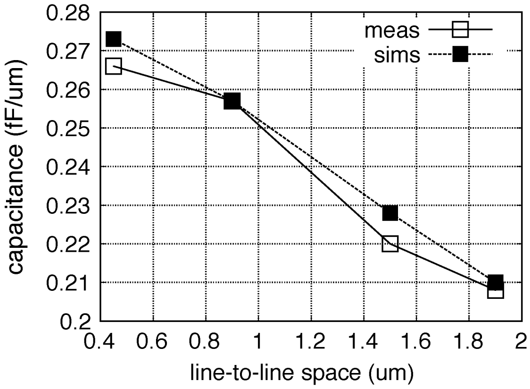

Fig. 6. Comparison of M3 middle line capacitance as a function of line-to-line spaces between simulations and measurement.

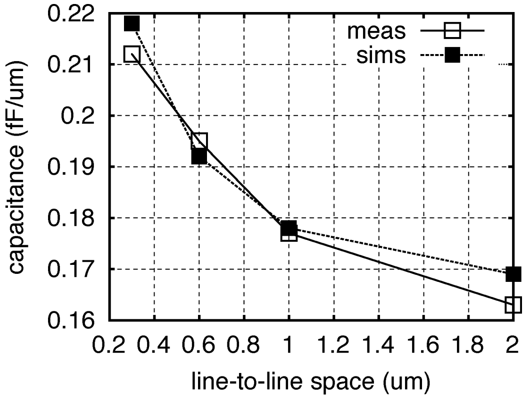

Fig. 7. Comparison of M2 middle line capacitance as a function of line-to-line spaces between simulations and measurement.

VI. Conclusion

In this paper, topography and RCX simulation were joined to predict the timing delays in the backend stacks of a 100-nm CMOS process for memory cells currently under development. A rigorous simulation approach like the one presented is indispensable for today's technologies, since timing delays become increasingly important due to shrinking. Starting from the flat wafer surface, the topography simulation steps of etching, deposition, and CMP are performed at the feature-scale level. The ELSA simulator can handle all common etching and deposition processes, and is based on an advanced level-set algorithm.

The complex interconnect structures are built from the structures at the feature scale yielding many configurations depending on metal combination, line-to-line space, and line width. The interconnect structures serve as input to the field solver, in this case RAPHAEL, whose capacitance simulations are stored in a database. The circuit designer accesses the results of this simulation flow and uses them in SPICE circuit simulations.

The significant influence of void formation on the capacitances was quantified, as using voids in a controlled and reproducible manner can be an economically advantageous substitute for low-k materials. The simulations show very good agreement with CBCMs and, hence, they played a significant role during the development of the backend process and circuit design.

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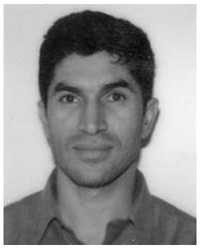

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