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SiC Power Rectifier With Improved Switching Performance "Numerical Analysis of Merged PiN Schottky Diode"

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We present numerical simulation results of SiC power rectifiers with improved switching performance. SiC's power rectifiers are categorized into three classes: Schottky diodes which offer extremely high switching speed, but suffer from high leakage current; PiN diodes which offer low leakage current but show reverse recovery charge during switching and have a large junction forward voltage drop due to the wide band gap of SiC; merged PiN Schottky (MPS) diodes which offer Schottky-like on-state and switching characteristics, and PiN-like off-state characteristics [1]. Simulation-based analysis to verify the performance of a 4H-SiC MPS diode shown in Fig. 1 has been carried out. The design primarily consists of selecting the optimum Schottky metal, size and spacing of the p^+ implanted regions, and thickness and dopant density of the drift region. It is important to achieve a good quality Schottky interface to obtain a low on-state drop when operated in the Schottky barrier diode mode. The metal-SiC barrier height of the Schottky metal was selected to be low enough to give a low on-state voltage, while still enabling effective pinch-off during the off state. This is achieved by using Ni as the Schottky metal.

The key parameters that alter the overall device performance (Table 1) have been optimized using the general-purpose device simulator MINIMOS-NT [2]. The diode has an epitaxial layer thickness of 10.5 μm over a 4H-SiC n^+ substrate doped at 9×10^{15} cm^{-3} to obtain the desired blocking voltage capability of 1500 V. The relative area and geometrical layout of the p^+ implanted region are fundamental design parameters that affect the device characteristics. A large p^+ implanted area is resulting in a higher on-state voltage due to a smaller Schottky conducting area, but offers lower leakage due to a more effective pinch-off of the Schottky portion. The optimized diodes have a 2 μm wide p^+ implanted region with 4 μm spacing.

parameter	value
p+ length, thickness, and concentration	2 μm, 1.5 μm, 1.0×10^{17} cm^{-3}
n- epilayer thickness and concentration	10.5 μm, 9×10^{15} cm $^{-3}$
spacing between p+ implanted regions	4.0 μm

Table 1: Summary of optimized device parameters used for a simulation of MPS diode.

Fig. 2 illustrates the on-state characteristics of the MPS diode for different temperatures. The result shows very good agreement between the simulated and measurement results obtained from [3]. The result is also indicative of an excellent rectifier ability of the MPS diode. The on-state characteristics of the MPS and Schottky diodes are almost identical, indicating excellent current spreading and minimal increase in the on-state voltage due to the introduction of the p^+ implanted grid. The current flow in the MPS diode occurs primarily across the Schottky region as shown in Fig. 3. A high current density of 600 A/cm^2 for an on-state voltage drop of only 3 V was obtained. The reverse bias characteristics of the MPS diode displayed in Fig. 4 is much more similar to the PiN diode than to the Schottky diode. A blocking voltage of 1350 V which is 90% of the desired value with negligible leakage current density was achieved for the MPS diode operating at room temperature. To evaluate the effectiveness of the p^+ region on the reverse bias operation, the ratio of the electric field at the Schottky interface to the peak electric field (at the bottom of the p^+ region) is analyzed by simulation. For the optimized device geometry shown in Table 1 this ratio is found to be only 26% as depicted in Fig. 5. When the space between the p^+ regions is increased, this ratio also increases and the reverse blocking characteristics becomes poor due to Schottky barrier lowering effect as obviously observed in the case of Schottky rectifiers.

REFERENCES

[1] R. Singh *et al.*, in *Proceedings of the 12th International Symposium on Power Semiconductor Devices and ICs* (2000), pp. 101–104.

[2] *Minimos-NT, Device and Circuit Simulator, User's Guide*, Institute for Microelectronics, TU Vienna, Austria, 2002, http://www.iue.tuwien.ac.at/mmnt/.

[3] A. Hefner Jr. *et al.*, in *Conference Record of the 2000 IEEE Industry Applications Conference* (2000), Vol. 5, pp. 2948–2954.

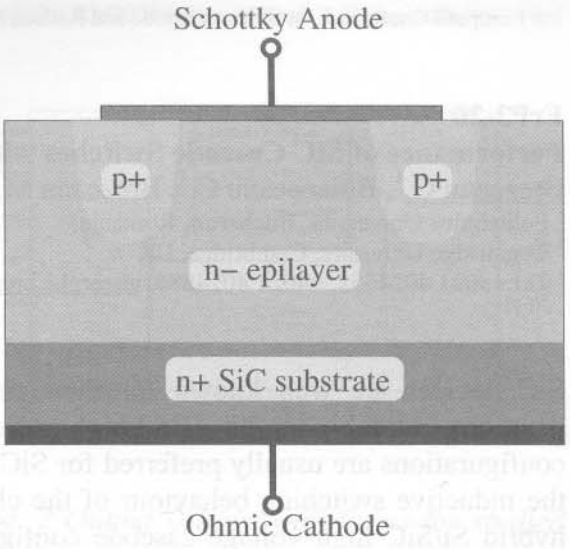

Figure 1: Cross section of a 4H-SiC MPS diode.

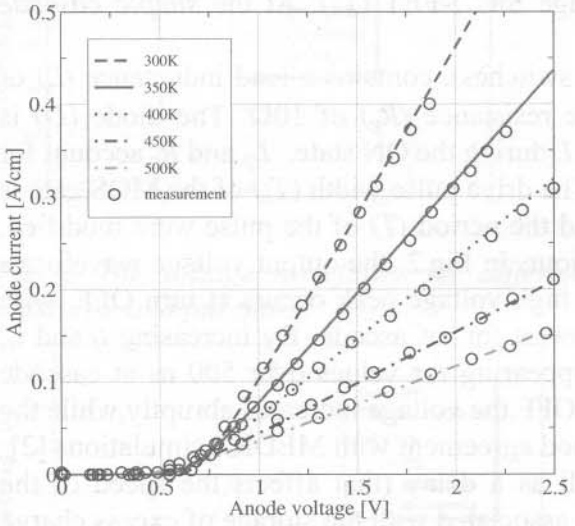

Figure 2: Comparison of measured and simulated forward characteristics of a 4H-SiC MPS diode at different temperatures.

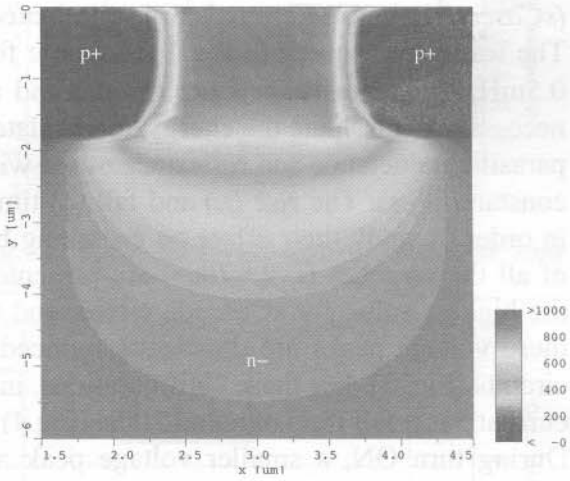

Figure 3: Current density in the 4H-SiC MPS diode in forward bias operation.

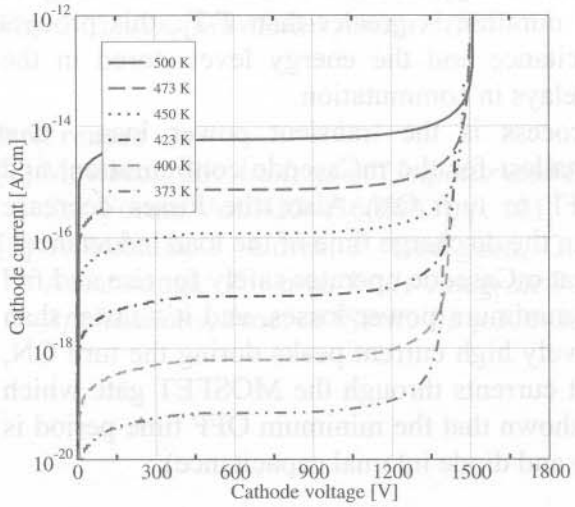

Figure 4: Reverse voltage characteristics of 4H-SiC MPS diode at different temperatures.

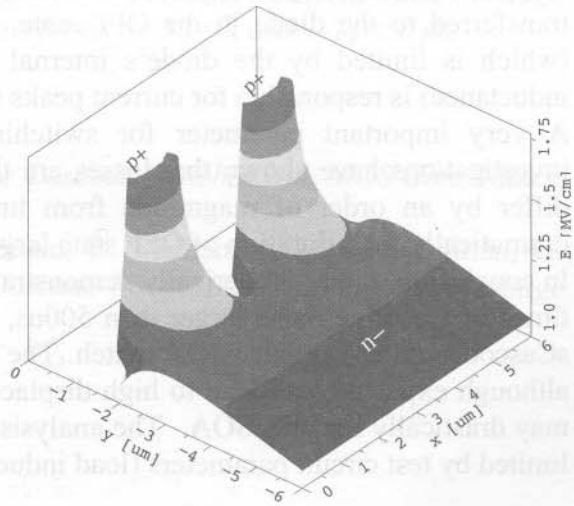

Figure 5: Profile of the electric field in a 4H-SiC MPS diode at 1000 V reverse voltage operation.