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Numerical Simulation and Optimization for 900V 4H-SiC DiMOSFET fabrication

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Silicon Carbide has been around for over a century. However, only in the past two to three decades has its semiconducting properties been sufficiently studied and applied, especially for high-power and high-frequency devices. We present a numerical simulation-based optimization of DiMOSFET using the general-purpose device simulator MINIMOS-NT [1].

The simplified schematic cross section of the simulated DiMOSFET cell is shown in Fig. 1. For simulation, a 10μm thick drift layer with doping concentration of $5x10^{15}cm^{-3}$ was chosen for a 1000V blocking voltage design. The p-type well is created by experimental data of multiple energy boron implants and p-well junction depth is 0.6μm. Then a 0.2um deep p+ region for an ohmic contact was formed with a box profile concentration of $5x10^{19}cm^{-3}$. Nitrogen implants are used for n+ source region, and the peak concentration and junction depth are $5x10^{19}cm^{-3}$ and 0.15μm, respectively. A 50nm gate oxide is formed. For device simulation, we have utilized published material data listed in Table 1.

The simulation results were used to calculate Baliga's figure of Merit (BFOM) as the criterion structure optimization and comparison. BFOM is given by [2] and [3]

$$BFOM = V_B^2/R_{ON}$$

where R_{ON} is the on-resistance and V_B is the breakdown voltage. Fig. 2 shows the simulated results of BFOM depending on the p-well spacing. As shown in Fig. 2, the best trade-off between breakdown voltage and on-resistance in terms of BFOM is achieved with a p-well spacing 5μm.

In order to achieve acceptable device performance, the maximum electric field in the oxide must be limited. For the desired breakdown voltage of 900V, the proposed device structure is optimized to have a 25μm half cell pitch and a 10μm thick n-drift region doped at $5x10^{15}cm^{-3}$. The doping concentration and the thickness of the p-well region are very important. If we decrease the p-well doping concentration below $3x10^{17}cm^{-3}$, the blocking voltage decreases because of a punchthrough. If we increase it further, the maximum operating voltage becomes limited by the maximum oxide field. The best trade-off between these relations has been achieved by setting the p-well doping concentration to $5x10^{17}cm^{-3}$. The specific on -resistance, $R_{ON,\,sp}$, simulated with V_{GS}=10V and V_{DS}=1V at room temperature, is around $22.76m\Omega cm^2$. The specific on-resistance depends on the gate bias. A high gate bias was required to turn the device fully on. This means that the on-resistance is dominated by the MOS channel resistance at room temperature[4]. So that reducing the on-resistance results in increasing high channel mobility. In this simulation, the device has an MOS channel mobility of $84cm^2/Vs$ and a threshold voltage of around 6V. The drain characteristics are shown in Fig. 3. Fig. 4 shows the breakdown voltage characteristics according to the termination structures. In this figure, an ion-implanted edge termination structure improved the breakdown voltage from 720V to 900V compared with the field plate structure.

Acknowledgement
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References

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[2] B. J. Baliga, Power Semiconductor Devices, PWS Publishing Company, 1996.

[3] Handoko Linewih, Sima Dimitrijev, IEEE Transaction on Electron Devices, Vol. 48, No. 8, 1711-1717, 2001.

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Table 1. Model parameter used for simulating 4H-SiC DIMOSFET

Electron mobility μ_n $N_D = 10^{16}$ cm $^{-3}$	Hole mobility μ_p $N_A = 10^{16}$ cm $^{-3}$	Donors & Ionization Energy (meV)	Acceptors & Ionization Energy (meV)	Saturated Electron Velocity v [10^7 cm / s]
$\parallel$ c-axis : 900 $\perp$ c axis : 800	115	N : 50, 92 P : 54, 93	Al : 200 B : 285	2

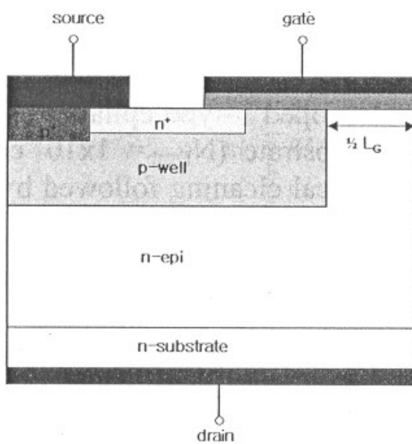

Fig. 1. Basic cell structure of simulated DiMOSFET.

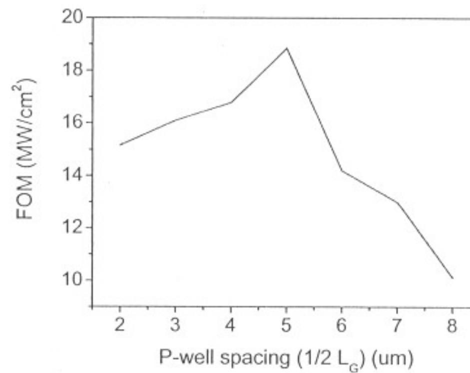

Fig. 2. Effects of the p-well (1/2 L_G) spacing on the Baliga's Figure of Merit.

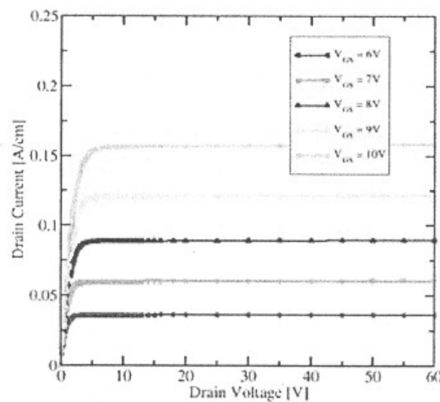

Fig. 3. Drain current characteristics of simulated DiMOSFET devices.

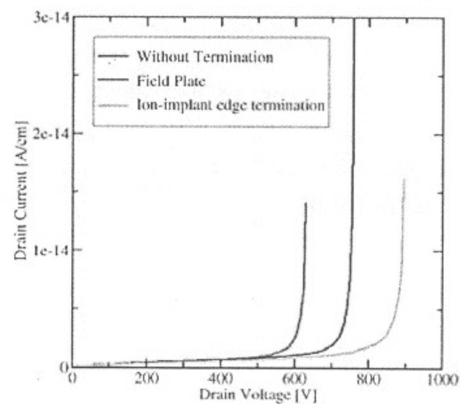

Fig. 4. Comparison of the breakdown Voltage depending on the termination structures.