Level Set Method Based General Topography Simulator and its Applications in Interconnect Processes

A. Sheikholeslami°, E. Al-Ani°, R. Heinzl△, C. Heitzinger°, F. Parhami⋆, F. Badrieh⋆, H. Puchner⋆, T. Grasser△, and S. Selberherr°

° *Institute for Microelectronics, Technical University Vienna, Gußhausstraße 27-29/E360, A-1040 Vienna, Austria, E-mail: sheikholeslami@iue.tuwien.ac.at*

⋆ *Cypress Semiconductor Corporation, San Jose, CA 95314, USA*

△ *Christian Doppler Laboratory for TCAD in Microelectronics at the Institute for Microelectronics*

Abstract— **The application of level set and fast marching methods to the fast simulation of surface topography especially in three dimensions for semiconductor processes is presented. Our general purpose topography simulator is based on these methods and has been implemented using many techniques for increasing of its speed.**

I. Introduction

Interconnects are becoming increasingly important with shrinking technologies. Capacitance and resistance of interconnect lines determine the timing delays due to metal lines, which contribute more and more to the overall delays. For proper modeling the capacitances, one has to know the metal profile, e.g., bottom and top *CD* (Critical Dimensions) and metal slope, the profile of the deposited layer with and without *CMP* (Chemical Mechanical Planarization), and the profile of the void, if it is formed. These profiles depend heavily on deposition process conditions, metal thickness, and line-to-line spaces, and less strongly on the metal width. The significant influence of void formation in a controlled and reproducible manner as an economically advantage for substituting expensive low-k materials was studied and simulated in two dimensions using our topography simulator [1].

The availability of a fast topography simulator which generates the metal profile and the profile of deposited layers using simulation of etching and deposition processes, is very important. However, three-dimensional topography simulation still faces many challenges which limit its general applicability and usefulness. In addition, three-dimensional topography simulation tends to be very *CPU* and memory expensive to date.

Based on an efficient and precise level set method including narrow banding and extending the speed function in a sophisticated algorithm, we have developed a general topography simulator in two and three dimensions for the simulation of deposition and etching processes. The simulator is called *ELSA* (Enhanced Level Set Application) and works efficiently concerning computational time and memory consumption. It ensures simultaneously high resolution. Furthermore we have developed *TOPO3D* whose kernel is based on *ELSA*, but in addition, it is linked to a program library for handling objects for full three-dimensional semiconductor process simulations. This program library is called *Wafer State Server*.

The outline of this paper is as follows. First, we present briefly the level set method and related techniques for an efficient implementation. Second, we present shortly some two-dimensional simulation results for the backend of a $100nm$ process. Third, some simulation results of three-dimensional structures applicable in interconnect processes are shown. Finally, we shortly describe the *Wafer State Server*.

II. The level set method

The level set method provides means for describing boundaries, i.e., curves, surfaces or hypersurfaces in arbitrary dimensions, and their evolution in time which is caused by forces or fluxes normal to the surface [2], [3]. The basic idea is to view the curve or surface in question at a certain time t as the zero level set (with respect to the space variables) of a certain function $u(t, \mathbf{x})$, the so called level set function. Thus the initial surface is the set $\{\mathbf{x} \mid u(0, \mathbf{x}) = 0\}$.

Each point on the surface is moved with a certain speed normal to the surface and this determines the time evolution of the surface. The speed normal to the surface will be denoted by $F(t, \mathbf{x})$.

The surface at a later time t_1 shall also be considered as the zero level set of the function $u(t, \mathbf{x})$, namely $\{\mathbf{x} \mid u(t_1, \mathbf{x}) = 0\}$. This leads to the level set equation

$$u_t + F(t, \mathbf{x})\|\nabla_{\mathbf{x}} u\| = 0, \qquad u(0, \mathbf{x}) \quad \text{given},$$

in the unknown variable u, where $u(0, \mathbf{x})$ determines the initial surface. Having solved this equation the zero

ISBN: 88-900847-0-7

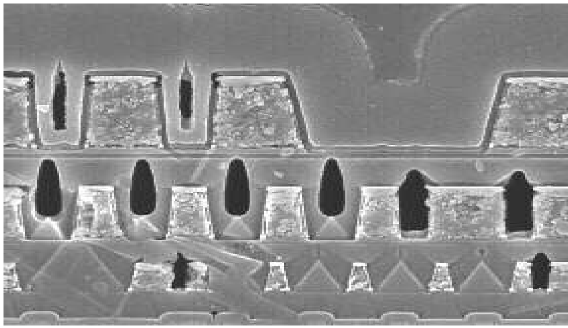

Fig. 1. SEM image of a whole backend stack comprised of three Al metals and a Ti-nitride interconnect.

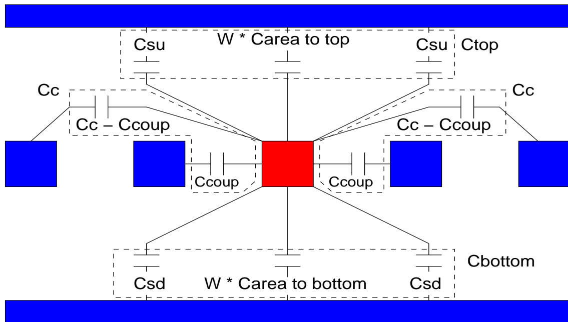

Fig. 2. Two-dimensional schematics of a signal line (middle) surrounded by grounded lines and planes.

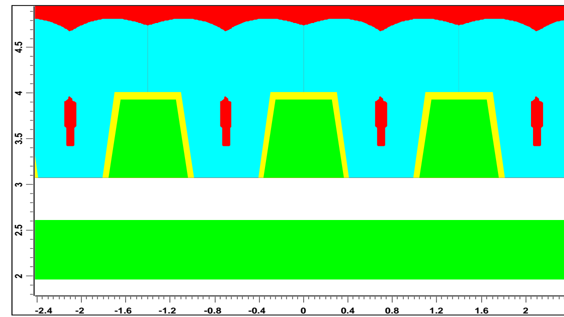

Fig. 3. Simulation of void formation by M3 lines at 0.90μm space above the M2 plane.

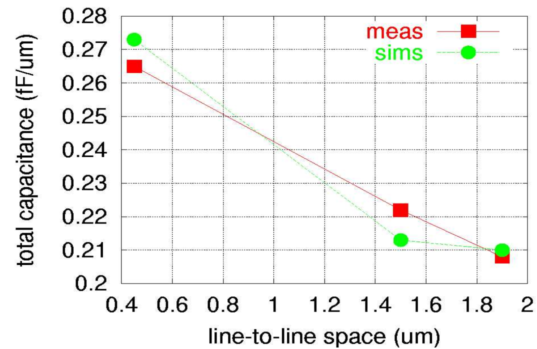

Fig. 4. Comparison between simulation and measurement of M3 middle line capacitance as a function of line-to-line spaces.

level set of the solution is the sought curve or surface at all later times.

Now in order to apply the level set method a suitable initial function $u(0, \mathbf{x})$ has to be determined first. A beneficial choice is the signed distance function of a point from the given surface. After calculation of the initial level set function, the speed function values on the whole grid are used to update the level set function in a finite difference or finite element scheme. Usually the values of the speed function are not determined on the whole domain by the physical models [4], [5] and, therefore, have to be extrapolated suitably from the values provided on the boundary, i.e., the zero level set. This can be carried out iteratively by starting from the points nearest to the surface. The idea leading to fast level set algorithms stems from observing that only the values of the level set function near its zero level set are essential, and thus only the values at the grid points in a narrow band around the zero level set have to be calculated. Both improvements, extending the speed function and narrow banding, require the construction of the distance function from the zero level set in the order of increasing distance. But calculating the exact distance function from a surface consisting of a large number of small triangles is computationally expensive and can be only justified for the initialization. An approximation to the distance function can be computed by a special fast marching method [6], [7].

III. Two-Dimensional Interconnect Capacitance Simulation

In the process considered the films deposited as *ILD* (Interlayer Dielectric) are silicon nitride and silicon dioxide films. For topography simulation of a deposition process, it is generally possible to consider complicated reaction paths. However, it is advantageous to reduce the possible reaction to an essential minimum for reducing the complexity of the simulator. Fig. 1 shows a whole backend stack comprised of three different metal lines M1, M2, and M3, bottom-up, respectively. In order to model capacitances, we assume that a signal line is at high voltage and surrounded by two lines on the left, two lines on the right, a plane underneath, and a plane above. The surrounding lines and planes are assumed to be at ground voltage. For example an M2 signal line could be surrounded by M2 grounded lines above the M1 plane and underneath the M3 plane. This skeleton is shown in Fig. 2. Most resistance and capacitance extraction *RCX* tools have very simplistic void models. Even if the metal slope is modeled, it is mostly assumed constant and independent of space. This is insufficient for today's technologies where interconnects have a large number of special features which are nowhere close to ideal [8], [9].

Fig. 3 shows the simulation result of void formation at 90μm line-to-line spaces where the slopes of metal lines

have been assumed to dependent on line-to-line spaces. A very good agreement between the simulations and measurements of M3 line capacitances with an error of less than 5% has been achieved as shown in Fig. 4.

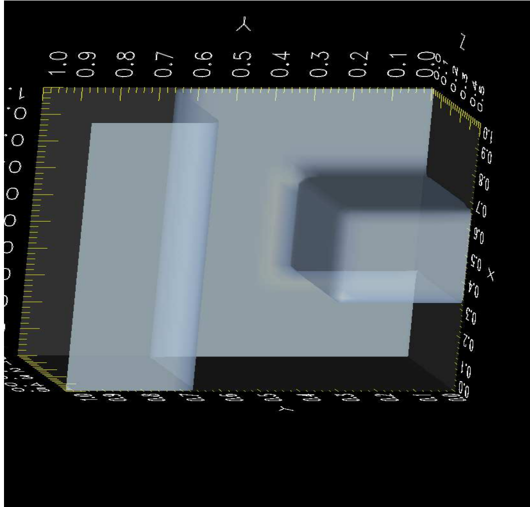

Fig. 5. Three-dimensional initial boundary for the deposition of silicon dioxide and silicon nitride in an interconnect structure.

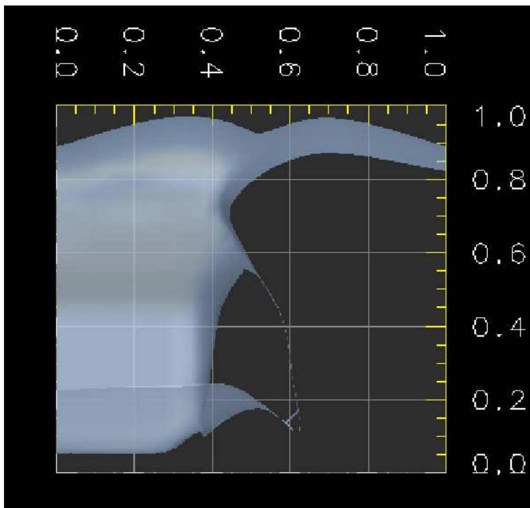

Fig. 6. A y-z point of view of simulation of void formation at $S = 0.72\mu m$ using *ELSA*.

IV. Three-Dimensional Simulation Results

In this section we present three-dimensional simulation results obtained by *ELSA* for detection of void formation in interconnect lines after deposition of *ILD* materials. Fig. 5 shows the three-dimensional structure, with metal width W, line-to-line spaces S, and metal thickness T in x, y, and z direction, labeled with X, Y, and Z, respectively. The deposited layers were silicon dioxide and silicon nitride with thickness of $D1 = 0.1\mu m$ and $D2 = 0.9\mu m$, respectively.

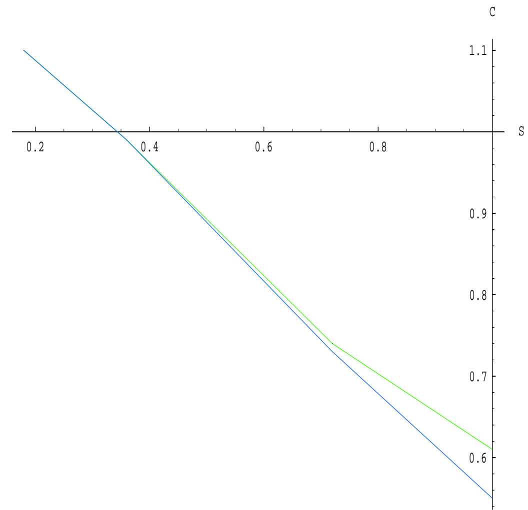

Fig. 7. Dependence of C on S for $T1 = 1.045\mu m$, and $T2 = 0.845\mu m$. The lower and upper curve stands for $T2$ and $T1$, respectively.

The goal of simulation was detecting the void for a set of different S holding the metal thickness one time at $T1 = 1.045\mu m$, and for second time at $T2 = 0.845\mu m$. We introduce a parameter C(T,S) which is calculated as follows:

$$C(S,T) = T + D1 + D2 - H_{void}(S)$$

where H_{void} stands for the z coordinate of the top of a void. In order to know how C(T,S) depends on line-to-line spaces and metal thickness, we have performed four different simulations at $S = 0.18, 0.36, 0.72$, and $1\mu m$, for $T1$ and for $T2$. Fig. 6 shows a y-z point of view of the three-dimensional simulation of void formation of the initial structure shown in Fig. 5 for $S = 0.72\mu m$ and $T1$.

Fig. 7 shows the simulation result for calculating of C for different line-to-line-spaces at $T1$, and $T2$. As expected, the z coordinate of top of void has been greater as we have increased S. Whereas for small line-to-line spaces the metal thickness does not play an important role, the effect of metal thickness will be more important with increasing S. Furthermore, the simulation results have shown that the metal width can not considerably affect the void formation and its dimensions.

V. Wafer State Server

The *Wafer State Server* is a program library and file format for handling three-dimensional objects in semiconductor process simulation developed at the Institute for Microelectronics [10]. It is a solution to the integrated simulation of three-dimensional manufacturing processes. A generic data model suitable for process and device simulations allows for an efficient data exchange between simulators even when they are based on different native file formats. It is able to handle different

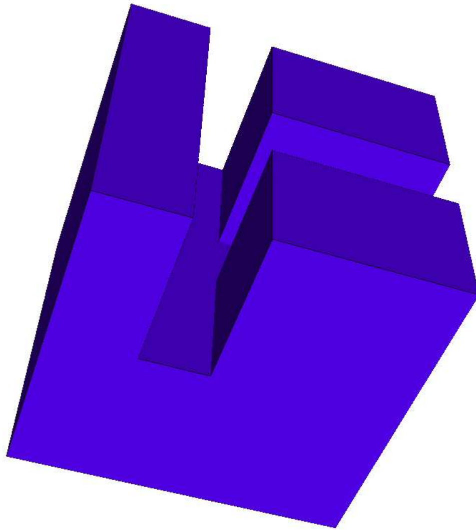

Fig. 8. A T-shape initial boundary for an isotropic deposition process.

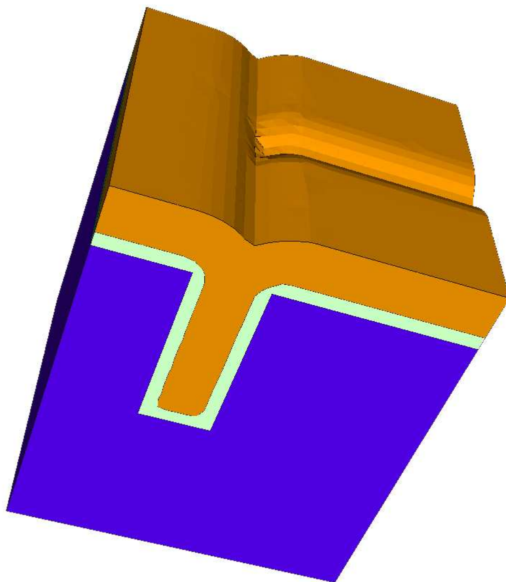

Fig. 9. Simulation result of isotropic deposition of two different materials using *TOPO3D*.

meshes and distributed quantities stored thereon. The program library also defines algorithms to perform geometrical operations for full three-dimensional process simulation as they are used in topography simulations.

Fig. 9 shows the simulation result of an isotropic deposition into a T-shape initial boundary shown in Fig. 8 using *TOPO3D*. The deposition simulation have been done for two different materials.

VI. Conclusion

State of the art algorithms for surface evolution processes like deposition and etching processes in three dimensions have been implemented. A general purpose topography simulator was developed based on the level set method combining narrow banding and fast marching methods for extending the speed function. The application of the simulator has been presented for two and three-dimensional interconnect processes. A very good agreement between the two-dimensional simulation results and measurements of capacitance after deposition of *ILD* materials has been achieved. A set of three-dimensional simulations for different line-to-line spaces and metal thicknesses has been performed. Line-to-line spaces and metal thickness play an important role by void formation and its dimensions. However, the effect of metal thickness on void profile will only be important from a determined line-to-line spaces.

Acknowledgment

The authors acknowledge the support of Infineon Technologies, Austria, and Toshiba Corporation, Japan for this work.

References

[1] C. Heitzinger, A. Sheikholeslami, F. Badrieh, H. Puchner, and S. Selberherr, 'Feature-Scale process Simulation and Accurate Capacitance Extraction for the Backend of a 100-nm Aluminum/TEOS Process,' *IEEE Trans. on Electron Devices*, vol. 51, no. 7, pp. 1129-1134, 2004

[2] J. Sethian, *Level Set Methods and Fast Marching Methods*, Cambridge University Press, Cambridge, 1999

[3] C. Heitzinger, *Simulation and Inverse Modeling of Semiconductor Manufacturing Processes*, Dissertation, Technische Universität Wien, 2002

[4] T.S. Cale, 'Flux Distributions in Low Pressure Deposition and Etch Models,' *J. Vac. Sci. Technol. B*, vol. 9, pp. 2551–2553, 1991

[5] T.S. Cale and G.B. Raupp, 'A Unified Line-of-Sight Model of Deposition in Rectangular Trenches,' *J. Vac. Sci. Technol. B*, vol. 8, pp. 1242–1248, 1990

[6] A. Sheikholeslami, C. Heitzinger, T. Grasser, and S. Selberherr, 'Three-Dimensional Topography Simulation for Deposition and Etching Processes Using a Level Set Method,' *Proc. of International Conference on Microelectronics (MIEL)*, Nis, Serbia and Montenegro, May 2004, pp. 241-244

[7] A. Sheikholeslami, C. Heitzinger, F. Badrieh, H. Puchner, and S. Selberherr, 'Three-Dimensional Topography Simulation Based on a Level Set Method,' *Proc. of Internatonal spring Seminar on Electronics Technolog (ISSE)*, Sofia, Bulgaria, May 2004, pp. 263-265

[8] F. Badrieh, H. Puchner, C. Heitzinger, A. Sheikholeslami, and S. Selberherr, 'From Feature Scale Simulation to Backend Simulation for a 100nm CMOS Process,' *Proc. European Solid-State Device Research Conference (ESSDERC)*, Estoril, Portugal, September, pp. 441-444

[9] A. Sheikholeslami, C. Heitzinger, H. Puchner, F. Badrieh, and S. Selberherr, 'Simulation of Void Formation in Interconnect Lines,' *Proc. of SPIE's first International Symposium on Microtechnologies for the New Millennium: VLSI Circuit and Systems*, Gran Canaria, Spain, May 2003, pp. 445-452

[10] T. Binder, *Rigorous Integration of Semiconductor Process and Device Simulators*, Dissertation, Technische Universität Wien, 2002