High Performance Carbon Nanotube Field Effect Transistor with the Potential for Tera Level Integration

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ABSTRACT

Vertically grown carbon nanotubes have the potential for tera-level integration. However, the well-known ambipolar behavior limits the performance of carbon nanotube field effect transistors. In this work we demonstrate that a double gate structure effectively suppresses the ambipolar behavior. Using the double gate design excellent device characteristics along with the potential for high scale integration are achieved, which are necessary for future nanoelectronic applications.

1 INTRODUCTION

Exceptional electronic and mechanical properties together with nanoscale diameter make carbon nanotubes (CNTs) a candidate for nanoscale field effect transistors. While early devices have shown poor device characteristics, high performance devices were achieved recently [1, 2].

Conventional CNTs are grown laterally [3], which is not optimal for high scale integration. A new method has been developed to grow CNTs vertically [4, 5]. In this method vertically aligned CNTs are selectively grown in nanoholes formed in anodized alumina oxide (AAO) templates, see Fig. 1. Each device is formed by a vertical CNT attached to the bottom (source) and upper (drain) electrodes and a gate electrode, which can be integrated in large arrays with the potential for tera-level density (10^{11} cm^{-2}) [4, 5]. Due to easier fabrication, the top gate structure depicted in Fig. 2 was used to manufacture device arrays, but because of low coupling between the gate and the CNT, poor device characteristics were achieved [4, 5]. The best coupling between the gate and the CNT can be achieved, if the gate surrounds the CNT. We refer to this structure as coaxial Single Gate (SG) structure. In this work we performed a comprehensive numerical study of this structure. Based on the results we propose a new optimized structure, referred to as coaxial Double Gate structure (DG), so that a high-performance device can be achieved.

2 MODELING

The contact between metal and CNT can be of Ohmic [6] or Schottky type [7]. In this work we focus on Schottky contact CNTFETs which operate by modulating the transmission coefficient of carriers through the Schottky barriers at the metal-CNT interface [7, 8]. In order to account for the ballistic transport we have solved the coupled Poisson and Schrödinger equations for the Schottky barrier CNTFET [9].

$$\frac{\partial^2 V}{\partial \rho^2} + \frac{1}{\rho}\frac{\partial V}{\partial \rho} + \frac{\partial^2 V}{\partial z^2} = -\frac{Q}{\epsilon} \tag{1}$$

$$-\frac{\hbar^2}{2\mathrm{m}^*}\frac{\partial^2 \Psi^{\mathrm{n,p}}_{\mathrm{s,d}}}{\partial z^2} + (\mathrm{U}^{\mathrm{n,p}} - \mathcal{E})\Psi^{\mathrm{n,p}}_{\mathrm{s,d}} = 0 \tag{2}$$

We have considered an azimuthal symmetric structure, in which the gate surrounds the CNT, such that the Poisson equation (1) is restricted to two-dimensions. In (1) $V(\rho, z)$ is the electrostatic potential, and Q is the space charge density.

In the Schrödinger equation (2) the effective mass is assumed to be $\mathrm{m}^* = 0.06\mathrm{m}_0$ [8] for both electrons and holes [10]. In (2) superscripts denote the type of the carriers. Subscripts denote the contacts, where s stands for the source contact and d for the drain contact. For example, $\Psi^{\mathrm{n}}_{\mathrm{s}}$ is the wave function associated with electrons that have been injected from the source contact, and U^{n} is the potential energy that is seen by electrons. The Schrödinger equation is just solved on the surface of the tube, and because of azimuthal symmetry, (2) is restricted to one-dimension.

The space charge density in (1) is calculated as:

$$Q = \frac{\mathrm{q}(p-n)\delta(\rho - \rho_{\mathrm{cnt}})}{2\pi\rho} \tag{3}$$

where n and p are total electron and hole concentrations per unit length. In (3) δ/ρ is the Dirac delta function in cylindrical coordinates. Including the source and drain injection components, the total electron concentration in the CNT is calculated as:

$$n = \frac{4}{2\pi}\int f_{\mathrm{s}}|\Psi^{\mathrm{n}}_{\mathrm{s}}|^2 \mathrm{d}k_{\mathrm{s}} + \frac{4}{2\pi}\int f_{\mathrm{d}}|\Psi^{\mathrm{n}}_{\mathrm{d}}|^2 \mathrm{d}k_{\mathrm{d}} \tag{4}$$

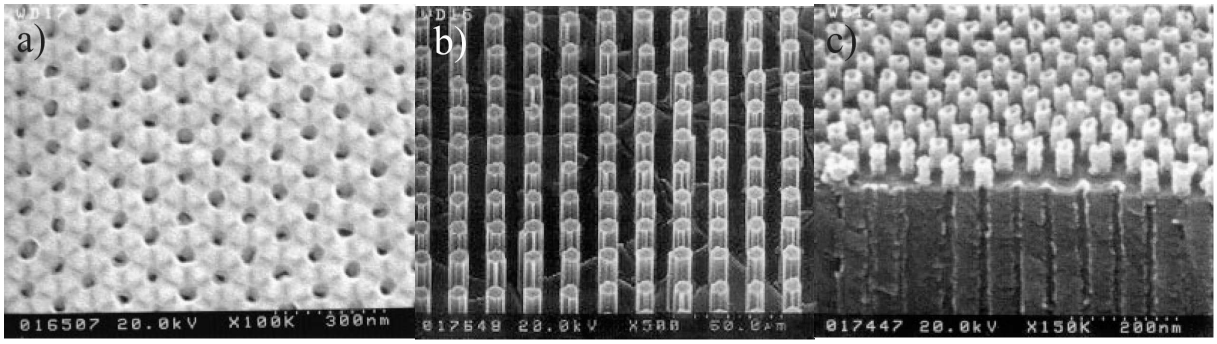

Figure 1: SEM images of porous AAO. a) Top view. b) Cross section of three-dimensional nanotube blocks or towers grown selectively on a 5 μm $\times$ 5 μm pattern. c) Vertically aligned CNTs grown in the patterned nanoprobes [4, 5].

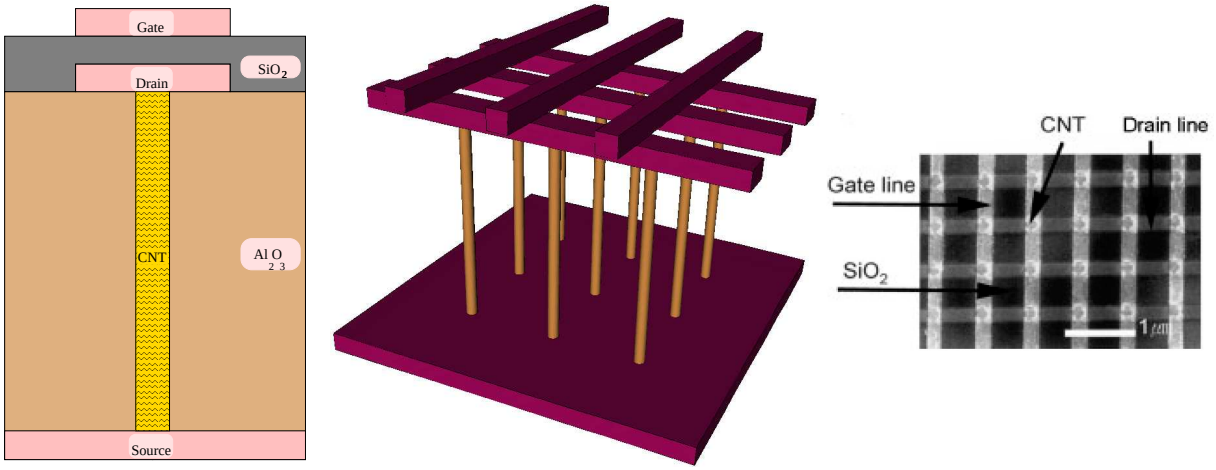

Figure 2: Left: 2D Sketch of top gate device. Middle: Array of top gate devices. Right: SEM image of top gate devices [4, 5].

where $f_{\mathrm{s,d}}$ are equilibrium Fermi functions at the source and drain contacts. All our calculations assume a CNT with 0.6 eV band gap and that the metal Fermi level is located in the middle of the CNT band gap at each contact [4, 5]. The total hole concentration in the CNT is also calculated analogously. Carriers were taken into account by means of a sheet charge distributed uniformly over the surface of the CNT [9].

The current is calculated by means of the Landauer-Büttiker formula [11]:

$$I^{\mathrm{n,p}} = \frac{4\mathrm{q}}{\mathrm{h}} \int [f_{\mathrm{s}}^{\mathrm{n,p}}(\mathcal{E}) - f_{\mathrm{d}}^{\mathrm{n,p}}(\mathcal{E})] TC^{\mathrm{n,p}}(\mathcal{E}) \mathrm{d}\mathcal{E} \quad (5)$$

where $TC^{\mathrm{n,p}}(\mathcal{E})$ are the transmission coefficients of electrons and holes through the device. The factor 4 in (4) and (5) stems from the twofold band and twofold spin degeneracy [7].

MINIMOS-NT is a semiclassical device simulator [12] which has been enhanced to perform quantum simulations by solving the coupled Schrödinger-Poisson equation system. Successive iteration between the Poisson and Schrödinger equations with appropriate numerical damping are carried out until appropriate convergence is reached.

3 Simulation Results

First we consider a coaxial SG structure in which the gate covers the whole CNT as shown in Fig. 3. Current-voltage characteristics of this structure are shown in Fig. 5 and Fig. 7. The ambipolar behavior of this structure is clearly observed, in agreement with experimental results [13, 14]. To understand this behavior the band edge profile is shown in Fig. 6. Applying positive voltages higher than the gate voltage to the drain of n-type devices suppresses the Schottky barrier near the drain contact and consequently increases hole injection at the drain contact. In the off regime this results in a high off-current, see Fig. 5, and in the on regime the drain current increases with respect to the drain voltage instead of saturation, see Fig. 7. The ambipolar behavior limits the performance of the device in both on and off regimes. To avoid this phenomenon, we propose a coaxial DG structure as shown in Fig. 4. While the lower gate controls electron injection at the source contact, the upper gate is connected to the drain and controls the band edge profile near the drain contact. If the drain voltage is applied to the upper gate, the band edge profile near the drain contact will be flat at any drain voltage, see Fig. 6. In consequence the tunneling current of

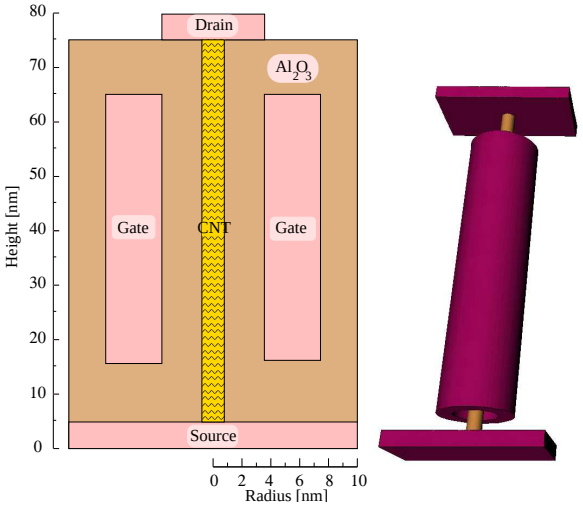

Figure 3: Coaxial SG structure.

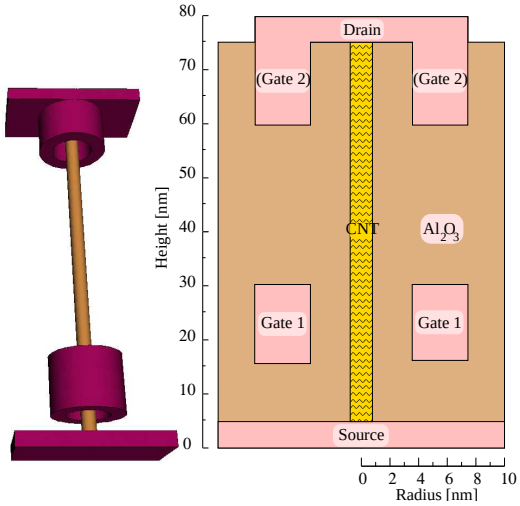

Figure 4: Coaxial DG structure.

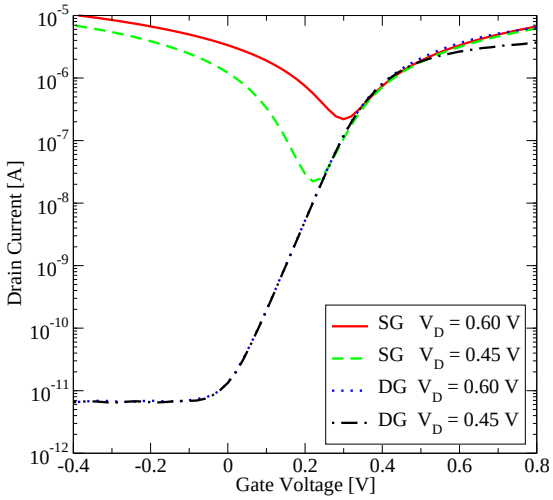

Figure 5: I-V characteristics of the coaxial SG and DG structures.

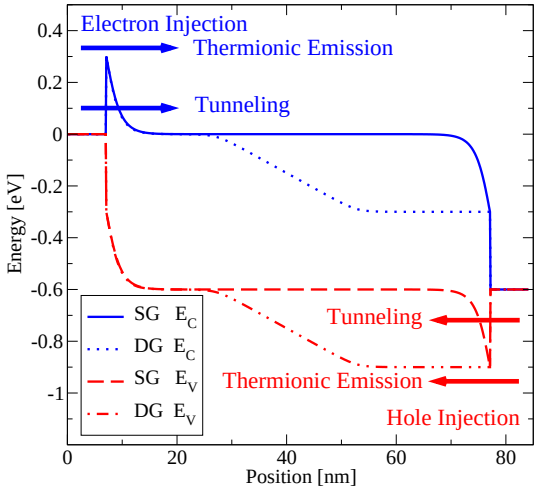

Figure 6: Band edge profi le of the coaxial SG and DG structures.

holes at the drain contact is suppressed, and there is just some negligible thermionic emission current of holes, see Fig. 5. While electron injection at the source contact can be controlled via the lower gate, the upper gate suppresses parasitic hole current at the drain contact.

The same discussion holds for p-type devices. By applying negative voltages to the lower gate, hole injection at the source contact can be controlled and the upper gate, which is connected to the drain contact, suppresses parasitic electron current at the drain contact. The advantage of this structure is that it can be used for n- or p-type devices by changing the polarity of the applied voltages.

As seen in Fig. 5 and Fig. 8, the proposed DG structure shows improved device characteristics in comparison with the SG structure. Possessing excellent device characteristics and the potential of high-scale integration, the DG structure can be used for device arrays. One advantage of the device array in Fig. 9 is the layered structure. Fabrication of this structure includes the following steps: after covering the vertical CNT with a coaxial gate insulator, different layers are deposited and patterned, starting with inter-metal dielectric between the source and lower gate contacts, the metal layer for the lower gate contact, inter-metal dielectric between the lower and upper gate contacts, and the top metal layer for the upper gate and drain contacts.

4 Conclusion

To improve the performance of CNTFETs, the ambipolar behavior of these devices must be suppressed. For this purpose a DG structure is proposed. In the DG structure the first gate controls the carrier injection at the source contact and the second gate controls parasitic carrier injection at the drain contact. The DG structure can be also integrated in device arrays with the potential for tera level integration.

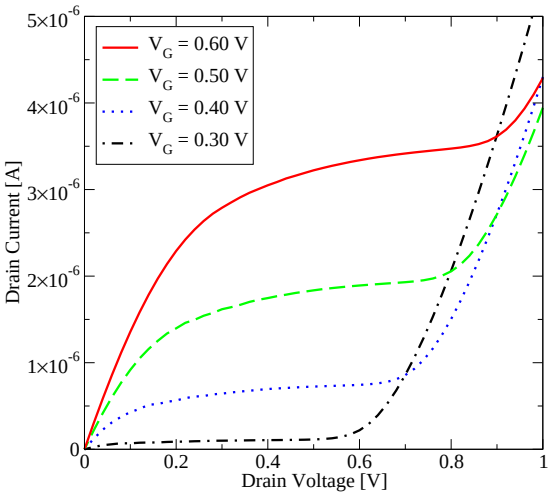

Figure 7: I-V characteristics of the coaxial SG structure.

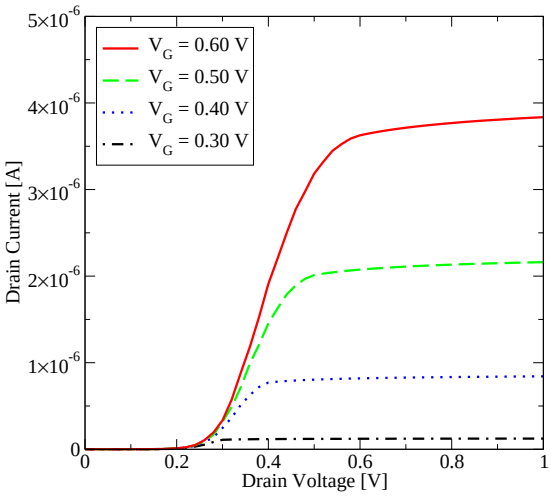

Figure 8: I-V characteristics of the coaxial DG structure.

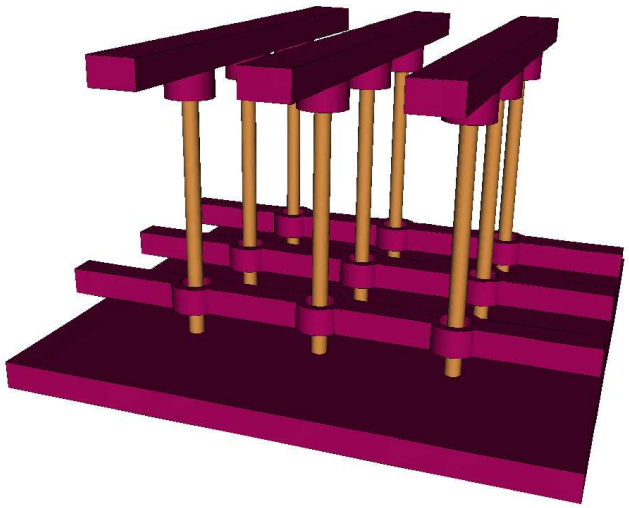

Figure 9: Array of coaxial DG devices.

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