9 Interconnects and Propagation of High Frequency Signals

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In deep submicron ULSI designs the overall circuit behavior is significantly determined by the on-chip interconnect structure. Until recently most interconnect models took only capacitances and resistances into account. Due to the steady increase in device speed integrated circuits will behave more and more like microwave circuits. With operating frequencies in the GHz regime the effect of the magnetic field can no longer be neglected. Inductances, skin effect, and transmission line behavior have to be considered carefully. Therefore, several advanced parameter extraction methods have been established. For complicated interconnect topographies, where lumped or one-dimensional distributed models do not reach the required accuracy, three-dimensional quasistatic or even full-wave models are required. These methods generate huge equation systems that cannot be used directly for circuit simulation. To increase efficiency model order reduction techniques become necessary. Since the amount of power dissipated in the interconnect structures is increasing, thermal interconnect modeling is also gaining importance, especially for Silicon-On-Insulator chips and low-k materials. We will analyze the impact on circuit design and discuss the requirements for simulation software to keep pace with these demands.

9.1 Introduction

On-chip interconnects play an increasingly important role in modern deep submicron integrated circuits (ICs). With the recent advances in IC technology devices got smaller and faster and it is most likely that this trend will continue for the next generations of semiconductor devices. State of the art microprocessors operate at clock frequencies in the GHz regime and signal rise times drop in the sub-nanosecond range. In contrast, the delay caused by the interconnect lines decreases at a much slower rate, in certain cases (e.g. for long wires) it may even increase with downscaling. Interconnects have become a potential bottleneck for further improvements in circuit speed because their performance is limited by various parasitic effects, like

- attenuation due to resistive voltage drops,

- signal delay which is mainly caused by the RC behavior of the wires,
- cross-talk resulting from capacitive or inductive coupling, or induced via the substrate,
- ringing and reflections incurred by discontinuities,
- electromagnetic radiation,
- skin effect and eddy currents (e.g. in spiral inductors).

These effects are mainly caused by the capacitance, resistance, and inductance of the wires.

The capacitance has the greatest influence on the electrical behavior and has been considered for a long time. In the 1980's interconnect line widths were around 1 μm, and their capacitance was modeled as a single lumped capacitor with a capacitance value proportional to the area of the wire (plate capacitor model). Because the aspect ratio of the wires was low and the distance was large, coupling between adjacent wires could be neglected. As the line widths got smaller the resistance of the interconnects increased and it had to be considered during circuit simulation. The signal delay was calculated with a first order approximation (a single RC lump) resulting in a single time constant (Elmore delay). The capacitance models had to be extended to include also fringing fields. With high aspect ratios, cross-talk between neighboring lines became significant and had to be implemented in the models with more accuracy. Taking into account the distributed nature of the capacitance and resistance, extraction of coupled RC-networks with many lumps has become necessary.

Inductance has been considered in printed circuit board and package design for a long time. With higher frequencies transmission line effects occur, hence, inductance of on-chip interconnects can no longer be neglected. This is especially true for long interconnect lines as used for clock and power distribution, global buses, and other long low-resistance interconnects optimized for high performance. Although global interconnects represent only a small percentage of the total wiring, many of these nets are "critical paths", and the delay on these lines has a direct influence on the system cycle time. More complex models for delay and impedance have been developed, that account for self-inductance and inductive cross-talk. As the wave-lengths of the signals reach the geometric feature size of the interconnects, quasistatic simulation becomes too inaccurate and full-wave models are required. Thus, the gap between digital and microwave designs is becoming narrow.

Higher current densities make the interconnects vulnerable to electromigration, which has to be considered during the design and verification process. Up to half of the total power consumption of a complex circuit is related to the interconnecting network and the line drivers alone. Therefore, effective models to determine the power consumption and strategies to minimize it for non-timing-critical nets are of great importance. On the other hand, also thermal interconnect models are required to prevent elevated temperature and guarantee system reliability.

The following sections shall give a general overview on existing modeling techniques, circuit simulation based on parasitics extraction, distributed models in one, two, and three dimensions, and model order reduction methods. Some issues regarding circuit design and reliability will be briefly discussed. In the last section important requirements on simulation software will be characterized.

9.2 Interconnect Modeling

Accurate analysis of electromagnetic phenomena in modern integrated circuits is difficult for three reasons: the large scale of the problem to be analyzed, the complexity of the geometries encountered, and the peculiarity of the physical equations that must be simultaneously analyzed. Basically this analysis is performed by calculating the electric and magnetic fields using Maxwell's equations. However, solving Maxwell's equations directly is only possible for a very limited area of the chip because of the enormous computational effort. To analyze larger domains, certain simplifications and assumptions have to be made to reduce the complexity of the equation system. Depending on the application one could ignore either the magnetic or the electric field, or the formation of electromagnetic waves using a quasistatic approach. Furthermore, the dimensionality of the simulation domain can be reduced to two, one (transmission line models), or zero dimensions (lumped model). For instance the capacitance of a straight line over a ground plane can be approximated by a two-dimensional simulation of the electric field in the cross-sectional plane, if the line is long enough and the fringing fields on both ends can be neglected. The electrical behavior of such a line can also be approximated by a one-dimensional transmission line model (see Section 5) based on per unit length resistance, inductance, capacitance, and conductance, if the cross-sectional dimensions are small compared to the smallest wavelength of interest. For lower frequencies the line may even be represented by a single resistor and capacitor (see Section 3).

Lumped models based on extracted capacitances, resistances, and inductances, are indeed the most frequently used simulation techniques in circuit analysis. In order to describe the distributed nature of the extracted parameters sufficiently accurate, many lumps may be necessary.

An example of computing resources needed by different simulation approaches is given in Fig. 9.1. All three examples have been performed for the structure displayed in Fig. 9.13. The circuit simulation has been realized with the program MINISIM [1], using a five stage lumped model based on the extracted resistances and capacitances of the structure. This approach uses the least computing resources by far[1].

[1] Because of the small size of the network the actual storage size of the system matrix is only a few percent of the value shown in Fig. 9.13 due to the static memory overhead of the program.

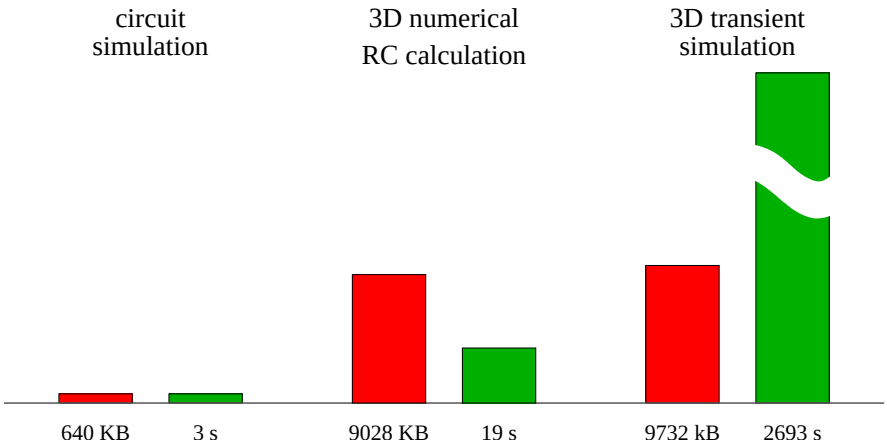

Fig. 9.1. Comparison of CPU time and memory requirements of different simulation approaches. The simulations have been performed for the structure in Fig. 9.13 on an Intel Pentium III PC at 500MHz

For the numerical capacitance and resistance calculation the finite element method (FEM) has been applied [2]. A significantly larger amount of memory is needed is for storing the simulation grid (approximately 20000 nodes and 13500 tetrahedron elements in this example) and the system matrix. The CPU time requirement of most numerical capacitance and resistance extraction methods scales approximately with $O(n * \ln n)$.

The three-dimensional transient simulation has also been calculated with the FEM in an electroquasistatic regime. The same simulation grid has been used as in the RC calculation example and, therefore, also the memory requirement is approximately the same. The high amount of CPU time needed stems from the fact that a large equation system has to be solved many times (once for each timestep). These methods give a good accuracy and can also be applied for non-linear systems, but may take prohibitively long even for the simulation of small parts of a layout.

To model the time dependence of signals two different techniques have established, namely time domain and frequency domain analysis.

Traditional circuit simulation tools like SPICE work in the time domain because the non-linear behavior of semiconductor devices can most easily be incorporated. The transient analysis is performed by breaking the time continuum into a series of adjacent short intervals. For the approximation of time dependent quantities low-order polynomials are used as the basis functions for each time step with the constraint, that the solution must be continuous across the interval boundaries. This time discretization transforms the ordinary differential equations (ODEs) describing the system into a set of non-linear algebraic equations that can be solved approximately with Newton's method. The presence of highly non-linear elements in the circuit may

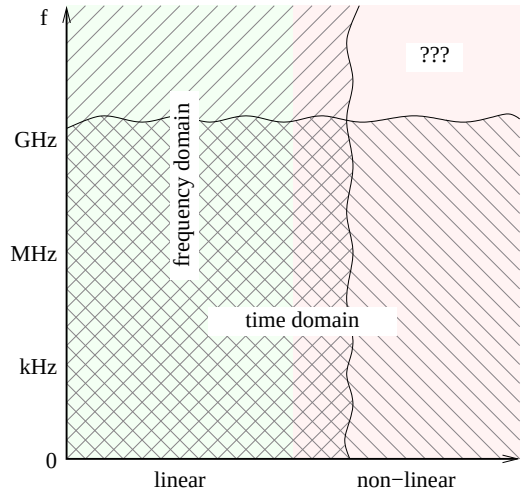

Fig. 9.2. Time domain vs. frequency domain analysis: Time domain models get inefficient for high frequencies, while simulation in the frequency domain cannot incorporate heavily non-linear circuits

cause the Newton iteration to fail. However, this problem can be circumvented simply by reducing the amount of the time step. This will bring the starting point and the solution of the Newton iteration closer together until convergence can be reached. For this reason time domain methods can achieve an excellent numerical robustness.

A drawback of transient simulation is that distributed elements (like transmission line models) and frequency dependent parameters (like dispersive permittivity) cannot be incorporated.

The efficiency of time domain methods decreases when the signal frequencies are high. This is especially true for narrow band signals in the form of modulated carriers, because the high-frequency carrier forces a small time step while a low-frequency modulation forces a long simulation interval.

For this reason frequency domain methods are commonly applied for the simulation of radio frequency (RF) circuits. They utilize the sparsity of the signal spectrum to reduce the computational effort. Therefore, the time is discretized with sinusoids as base-functions.

Most commercial circuit simulators offer a small-signal or AC analysis which is performed in the frequency domain where non-linear devices are linearized at their DC operating points. However, this method cannot be applied for circuits which depend on the non-linearity of devices, such as mixers, switched filters, samplers, or oscillators.

To a certain extent also non-linear elements can be used in extended frequency domain techniques. Passing a narrow-band RF signal through a non-linear circuit results in a broadband signal whose spectrum is relatively

sparse with clusters of frequencies near the harmonics of the carrier. Again, the sparse nature of the spectrum can still be exploited to minimize the computational cost. However, for a continuous broadband signal time domain methods would be more efficient.

The harmonic balance method is used to analyze circuits with non-linear components under a periodic excitation. Harmonically related sinusoids are the basis functions for the discretization of time dependent signals. Therefore, the initial transient behavior cannot be represented and only the steady-state behavior will be calculated. The differential equation model of the circuit is separated into a linear and a non-linear part. The linear part can be converted directly to the frequency domain using Laplace transformation. The evaluation of the non-linear part is performed in time domain. Inverse discrete Fourier transformation and forward discrete Fourier transformation is used to convert from frequency- to time domain and back. The spectrum of the output of the non-linear part may contain components higher than the highest input frequency. Therefore slight oversampling is usually used to suppress aliasing effects [3]. The discrete Fourier transformations can be expressed as matrix operations and combined with the model for the linear part resulting into an algebraic system of equations, which can be solved with the Newton-Raphson [4] method.

For strong non-linearities convergence problems may arise, which makes special algorithms (like the harmonic-relaxation Newton method) necessary in order to increase the stability of the harmonic balance method.

But also with transient methods it is possible to simulate in periodic time, simply by formulating the ODEs describing the system as a two point boundary value problem instead of an initial value problem [3]. The shooting method is used to obtain the solution for one time period. Thereby, even with highly non-linear elements a good numerical stability can be achieved, but one cannot directly simulate distributed components, such as transmission lines.

So called multi-variate methods are particularly suited for narrowband signals, utilizing the different time scales for the carrier and the modulation signals. Instead of a general time variable that is used for representing all frequencies, separate time variables are introduced for each of the base frequencies (e.g. carrier and modulation frequency), resulting in a partial differential equation (PDE) with a two- or more-dimensional time domain. The quasi-periodic harmonic balance method can be used for the solution of this equation [5].

9.3 Parasitics Extraction

Accurate parameter extraction is key for a successful simulation. Modern digital chip designs with several millions of gates require accurate calculation

of hundreds of millions of parasitic capacitances, resistances and inductances, which makes parameter extraction a very challenging task.

An immense number of such extraction methods have been reported in the literature, the next subsections shall give a short summary.

9.3.1 Capacitance Extraction

The numerical characterization of the electrostatic interconnect behavior and the extraction of the parasitic capacitive effects have become indispensable for the design of large-scale, reliable, and high-performance chips in the deep submicron domain. Accurate values are needed for the distributed net self capacitance and also for the electrostatic cross-coupling between individual nets.

Capacitance extraction methods can be divided into three groups, namely

- analytic calculation, which is only possible for very simple structures (e.g an infinitely long straight line over a ground plane [6]),
- geometric models or pattern matching techniques, which are very fast, but inaccurate for complex geometries with many layers [7–11] and are limited to rectangular structures, and
- numerical methods based on the solution of the Laplace equation, which have naturally a higher CPU-time and memory consumption.

Analytic capacitance calculation is hardly applied practically because of the limitation to simple geometries and the enormous mathematical effort needed to derive the equations. Sometimes analytic calculations of simple test structures are useful for the calibration of empirical capacitance models based on fitting formulae.

Geometric models approximate the capacitance values based on empirical formulae. E.g. the capacitance between two adjacent lines is determined by a portion that is proportional to the overlapping area and a portion that is caused by the fringing field. Pattern matching techniques partition the extraction domain into many smaller rectangular areas. For each part the closest match is searched for in a large pattern library and the capacitance values are looked up.

Both, geometric and pattern matching methods give results only for a specific IC technology. If essential technological parameters, like layer thicknesses, change, the models have to be recalibrated. For geometric models this is done by fitting the model parameters with accurate numeric simulations for a series of test examples. For pattern matching techniques the capacitance values for each of the library patterns have to be recalculated using a numeric method. Thus, the recalibration is usually a very time consuming (several days) task.

Both, geometric models and pattern matching are most frequently used for full-chip capacitance extraction because their execution is generally a lot faster than numerical methods.

Three-dimensional field solvers are most general since they directly solve the PDEs describing continuum electrostatics. The two most popular numerical techniques are the boundary element method (BEM) and the finite element method (FEM).

The BEM [12–14] uses an integral formulation based on Green's theorem

$$\varphi(\boldsymbol{r}) = \int_{\Gamma} G(\boldsymbol{r}, \boldsymbol{r}')\sigma(\boldsymbol{r}')\mathrm{d}A' \;, \tag{9.1}$$

where $G(\boldsymbol{r}, \boldsymbol{r}')$ is the Green's function that represents the potential at $\boldsymbol{r}$ due to a unit charge at $\boldsymbol{r}'$. The integration is performed over all charges (σ) i.e. the surface of conductors. For an infinitely large homogeneous dielectric Green's function is given as

$$G(\boldsymbol{r}, \boldsymbol{r}') = \frac{1}{4\pi\varepsilon|\boldsymbol{r} - \boldsymbol{r}'|} \;, \tag{9.2}$$

where ε is the permittivity and $|\boldsymbol{r} - \boldsymbol{r}'|$ is the Euclidean distance between the source and the evaluation point. For the approximate solution of the integral, the surface of the conductor is discretized into panels (boundary elements) and usually the method of moments is applied with a first-order collocation scheme or the Galerkin method [15]. The resulting algebraic system of equations has a fully occupied system matrix.

Traditional Gaussian-elimination would require $O(n^3)$ operations to solve the linear system, which renders this approach impractical if n is greater than a few thousands. Therefore, solving the system iteratively with the conjugate gradient method or GMRES [16] is more effective. Since a sparse matrix improves the performance of iterative methods significantly, several matrix sparsification techniques have been developed.

The fast multipole method [12,17], for instance, is used to reduce the overall computational complexity by efficient calculation of the "far-field". Using a hierarchical spatial decomposition into cells, the "far-field" is estimated between cells and not between every point, based on a multipole decomposition in the cell centers.

It is also possible to exploit the negligible influence of far apart conductors with the Schur algorithm [18]. Sparse system matrices can also be achieved with wavelet-like methods [19], singular value decomposition [20, 21], or grid based methods [22]. All of the mentioned methods help to reduce the computational complexity of the BEM to $O(n \log n)$ or even $O(n)$.

If the simulation domain consists of various materials with different permittivities ε also the interfaces between those materials have to be discretized with boundary elements to allow for polarization charge, thus increasing the size of the system matrix. To avoid this increase, it is possible to use appropriate Green's functions that represent the various dielectric constants, instead of the free space Green's function. Unfortunately for arbitrary geometries such a function cannot be easily derived. For stratified dielectric layers a Green's function can be found by the method of mirror images or with Fourier

transformation, which is well-suited for calculating interconnect capacitances in structures where planarization is applied throughout the manufacturing process. The evaluation and integration of complex Green's functions can be very time consuming, therefore numerical approximations may be used for performance improvement [23].

The above mentioned acceleration techniques make the BEM very efficient for accurate capacitance calculation, however, full-chip capacitance extraction is not feasible for complex layouts, mainly because of the memory requirements. On one side, some of the acceleration techniques reduce the memory consumption by sparsifying the system matrix, on the other side, additional data structures (tree-structures for geometry representation, ...) are required, needing far more memory than could be saved. To overcome this memory problem, geometric preprocessing is used to divide the layout into smaller subdomains, that can be simulated separately. For example the partial capacitances between a critical net and all neighboring conductors can be extracted by creating a "tunnel" around the critical net. Of course the width of the tunnel affects the obtained accuracy and must not be chosen too small. For full-chip extraction this procedure is repeated for each net [24].

Finite element [25] discretization gives a sparse matrix by nature, but usually larger than with BEM, because the whole interior of the dielectric has to be discretized with volume elements (e.g. tetrahedrons), not just the surface of the conductors. Therefore, fast iterative solvers are usually applied. For the discretization of the PDE the Galerkin- or the Ritz-Rayleigh-method is used. The finite element method (FEM) is most flexible and exhibits a good numerical stability. It is independent of the kernel of the PDE, therefore it is possible to apply it also for inhomogeneous, anisotropic, or non-linear dielectrics. High accuracy can be obtained by grid refinement or higher order shape functions.

Unlike integral methods, where Green's functions represent the electric field in an infinite domain, the simulation domain of the FEM is finite, usually delimited by homogeneous Neumann boundary conditions. Therefore, the electric field is truncated and distorted near the boundaries causing an error in the calculated capacitance (Fig. 9.3). The error decreases with the square of the width (or radius) of the simulation domain in two-dimensional simulations, and with the third power in three dimensions (Fig. 9.4).

Figure 9.5 depicts an example, where the FEM has been applied for capacitance extraction of two wires over a ground plane. In order to calculate all partial capacitance values for an n-conductor problem $n-1$ simulations have to be performed for different configurations of conductor potentials. In this example the potential distribution for the two field calculation runs are displayed using iso-surfaces (red = 1 V, blue = 0 V).

Compared to BEM, FEM is not limited to homogeneous stratified dielectrics, however, its computational effort is usually higher than the accelerated BEM.

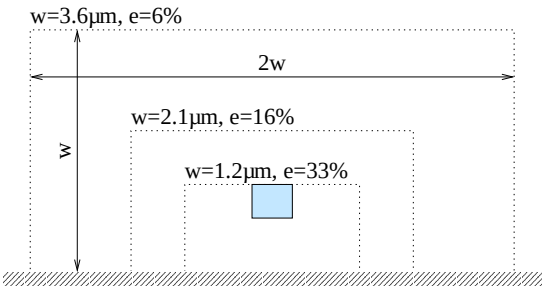

Fig. 9.3. Influence of the size of the simulation domain (w) on the error in the calculated capacitance (e) induced by the boundary of the simulation domain due to truncation of the electric field: The capacitance is calculated for a rectangular shaped wire (600 × 500 nm) over an ideal ground plane. The dotted lines delimit the simulation domains

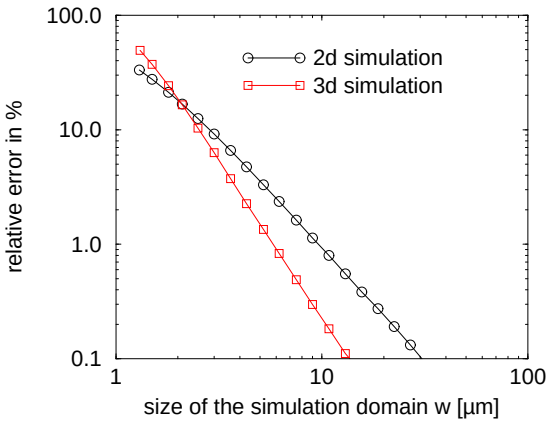

Fig. 9.4. Comparison of the field truncation error in two- and three-dimensional capacitance calculations. The calculations have been performed for a rectangular shaped conductor over a ground plane (cf. Fig. 9.3), for the three-dimensional case the length of the conductor is equal to its width

A combination of BEM and FEM, the so-called hybrid element method, integrates the advantages of both [26]. Areas with stratified layers are calculated with the BEM, for non-planar regions the FEM is used (cf. Fig. 9.6). Special models are required at the interfaces. A disadvantage of the hybrid element method is the necessity of a geometry preprocessing step, that divides the simulation domain into partitions for BEM and FEM discretization. Also the mesh generator must support both boundary and volume grids. This doubles the programming effort for the implementation of this method which may be the reason why it is hardly used for practical applications.

Another approach to combine the advantages of volume oriented methods like FEM and the boundary element method is called measured equation of invariance [27]. This method achieves a small but also sparse system matrix. The numeric effort is dominated by the evaluation of Green's functions. A speedup can be obtained by a variant, called geometry independent measured equation of invariance [28].

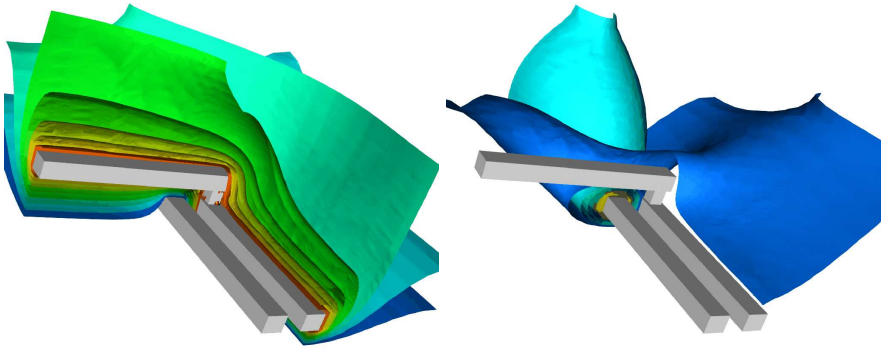

Fig. 9.5. Capacitance calculation with FEM for two interconnects over a ground plane (not shown). The iso-potential surfaces are displayed for two different conductor voltage configurations. Calculated capacitance values: $C_{1,2} = 0.52\,\text{fF}$, $C_{1,GND} = 1.04\,\text{fF}$, $C_{2,GND} = 1.15\,\text{fF}$

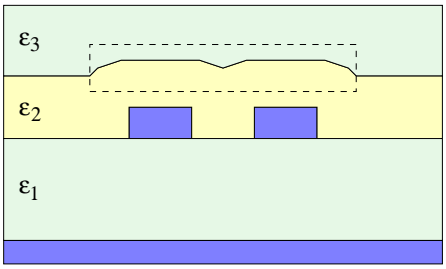

Fig. 9.6. The hybrid element method combines FEM and BEM. The area inside the dashed line is discretized with FEM because of the non-planar interface, for the rest of the simulation domain BEM is used

Capacitance can also be calculated with stochastic techniques, like the random walk method (RWM) [29,30]. It's low memory consumption makes it suitable for full-chip extraction. Like with most stochastic methods, the error decreases with the square root of samples (random walks). Therefore, this method has a performance of $O(n^2)$. While for big layouts and highly accurate results this means a longer run-time than accelerated BEM ($O(n \log n)$ or $O(n)$), it has the advantage, that a crude approximation of the calculated capacitances is available after a few iterations. Another advantage is the fact, that the RWM does not need a simulation grid.

9.3.2 Resistance Extraction

The interconnect resistance can either be approximated with polygonal decomposition models [31] (e.g. by "counting squares"), or calculated numerically.

The BEM cannot be applied efficiently, because interconnect wires tend to have a large surface and a small volume, leading to a huge fully occupied system matrix.

Hence, the FEM seems to be most accurate and robust, however at the cost of a higher computational effort than polygonal models. Speedups can be obtained by specially optimizing the elimination order of the Gaussian solver [32] and by introducing articulation nodes [33].

The simulation can be performed either in two dimensions for a single layer with constant thickness or in three dimensions for the whole structure including contacts and vias.

Since calculating the resistance with FEM requires solving the Laplace equation, as a by-product potential and current-density distributions can be obtained easily. In Fig. 9.7 the resistance of a via has been calculated and the current density distribution is displayed. The cones follow the direction of the current while their size (and color) corresponds to the value.

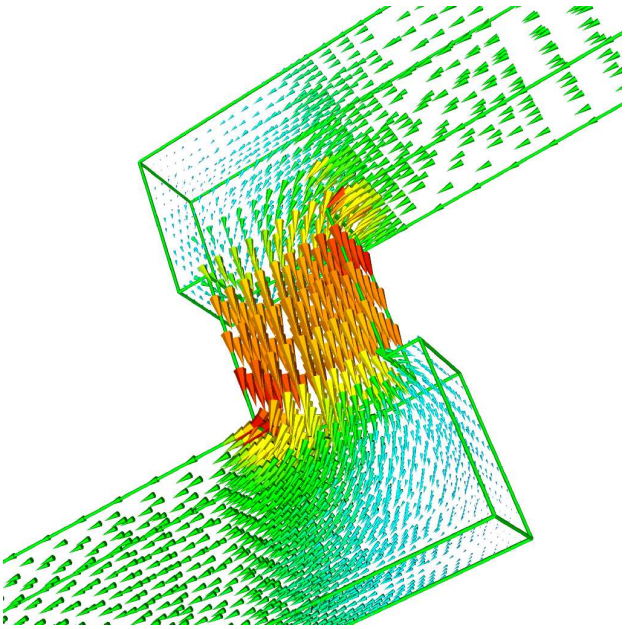

Fig. 9.7. Current density distribution in a via during resistance calculation. For symmetry reasons only the half of the structure has been simulated

9.3.3 Substrate Resistance

Not only parasitic capacitances and inductances cause cross-talk, but also the silicon substrate. Coupling to the substrate can be caused by the bulk contact

of transistors, diffused resistors, interconnects with a large substrate capacitance, or noisy supply lines with substrate contacts. Sensitive parts of the circuit may be influenced, especially in mixed-signal applications. Substrate resistance calculation is also performed with FEM, FDM [34], BEM [35, 36] or geometric models [37], whereas the substrate is approximated by an homogeneously conducting block.

Although the substrate resistance is modeled with the same physical equations as the interconnect resistance (Laplace equation), its calculation is more similar to capacitance extraction and the BEM can be applied efficiently. For substrates with a lightly doped epi-layer a layered Green's function can be derived [35]. However, for accurate simulation of diffused resistors, non-ideal contacts, or other non-stratified geometries, the FEM is better suited (cf. example in Fig 9.8). An approach, where FEM and BEM is combined for modeling substrate resistance is presented in [38].

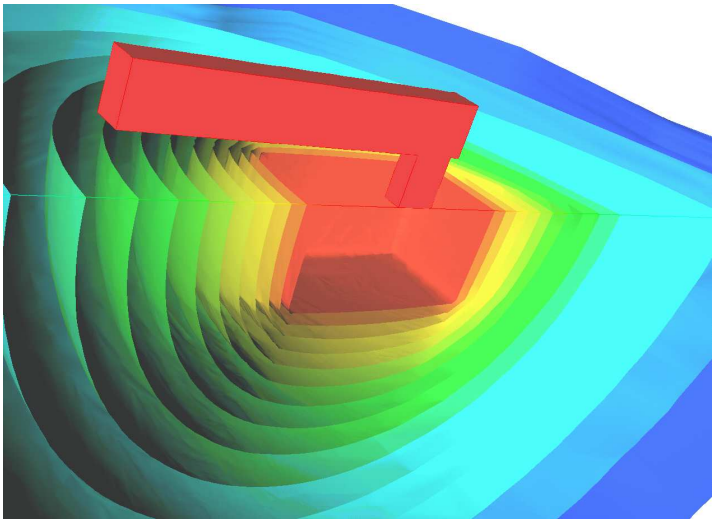

Fig. 9.8. Potential distribution around an Ohmic substrate contact with a diffused well to reduce the contact resistance. The solution has been obtained by finite element simulation

9.3.4 Inductance Extraction

Strictly speaking inductance is defined only for closed current loops. Therefore, the inductance of a wire depends on the current return path (and thereby on the signal frequency) which may not be known in advance. However, a worst-case estimation can always be obtained with the assumption that the return-path of the current is through the substrate, or the power grid. If

the real return-path goes through other nets, that are more close, then the real inductance will always be smaller. Another approach is the definition of partial inductances, where an infinitely far return path is assumed. Partial inductances may be included into circuit simulations, but will increase the system matrix size significantly.

Stationary inductance calculation methods are based on a numeric solution of Neumann's formula for a precalculated current density distribution:

$$L_{ik} = \frac{1}{I_i I_k} \frac{\mu}{4\pi} \int_{V_i} \int_{V_k'} \frac{\boldsymbol{J}_i(\boldsymbol{r}) \cdot \boldsymbol{J}_k(\boldsymbol{r}')}{|\boldsymbol{r} - \boldsymbol{r}'|} \, \mathrm{d}V \, \mathrm{d}V' \; . \tag{9.3}$$

The integration can either be carried out analytically for simple geometries and current distributions, numerically, where special attention has to be paid on the singularities of the integrand [39], or with the Monte Carlo method [40].

Another approach, where the evaluation of this two-fold volume integral is avoided, uses the magnetic vector potential $\boldsymbol{A}$ [41] and the Coulomb gauge by solving the vector-Poisson equation

$$\Delta \boldsymbol{A} = -\mu \boldsymbol{J} \; , \tag{9.4}$$

which can be separated into three scalar equations, one for each spatial coordinate. An ideal (superconducting) ground-plane can be represented by a homogeneous Dirichlet boundary condition for the vector potential $\boldsymbol{A}$. The inductance can then be calculated from the magnetostatic energy

$$L = \frac{W}{2I^2} = \frac{1}{I^2} \int_V \boldsymbol{A}\boldsymbol{J} \, dV \; . \tag{9.5}$$

An example of this method is demonstrated in Fig. 9.9, where the stationary distribution of the magnetic field $\boldsymbol{B}$ around a spiral inductor has been calculated using the FEM. Usually, the computational overhead of numerical inductance calculation methods is prohibitive for full chip extraction. Therefor, less accurate approximations of self and mutual inductances may be calculated with analytical formulae [42], based on a simplified geometric structure.

Extracted inductances based on the stationary distribution of the current density are only valid for low operating frequencies, because at higher frequencies current crowding at the surface of the wire can be observed, also known as skin effect. The thickness δ of current-carrying surface-area depends on the resistivity ϱ of the conductor, the signal frequency f, and the permeability μ of the medium, and can be approximated with the following equation:

$$\delta = \sqrt{\frac{\varrho}{\pi f \mu}} \; . \tag{9.6}$$

The skin depth for Aluminum and Copper has been plotted in Fig. 9.10. For example at 1 GHz it amounts to 2.7 µm for Al and 2.1 µm for Cu. For

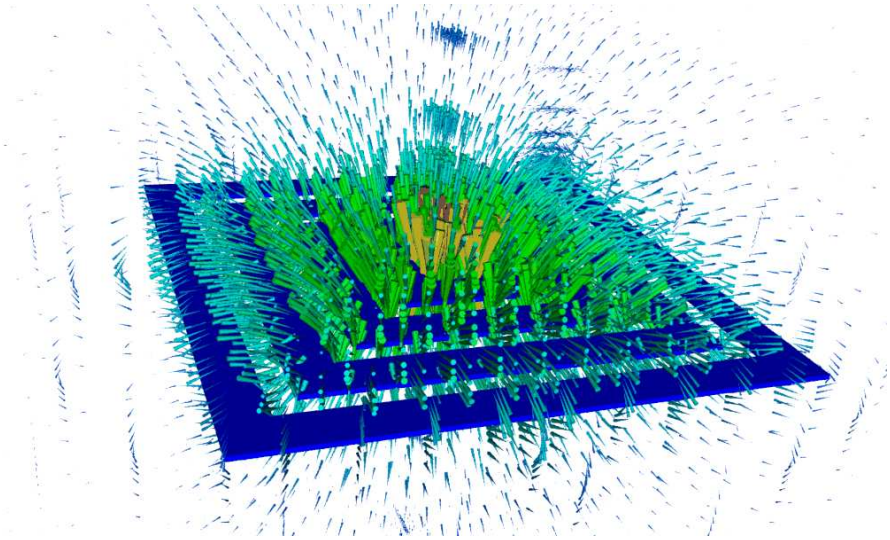

Fig. 9.9. Magnetic field ($\boldsymbol{B}$) around a spiral inductor

interconnects with a width larger than the skin depth, this brings out an "internal" inductance and results in an increased (frequency dependent) series impedance and attenuation, also a reduction in phase velocity can be observed.

Transient pulses with short rise times get rounded in the upper portion because the skin effect influences primarily the high-frequency components. Therefore, signal delay, which is usually measured at 50% levels is not greatly increased, but signal rise times, which are measured between 10% and 90% levels are significantly affected.

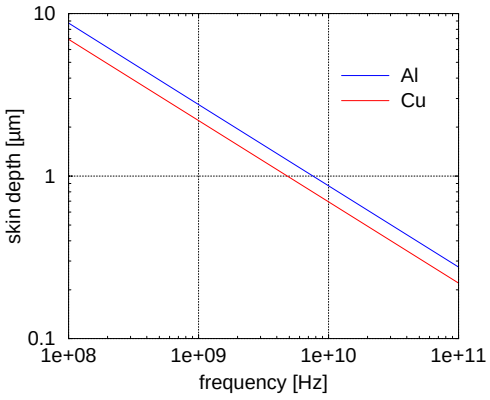

Fig. 9.10. Skin depth for Al and Cu wires

To calculate the frequency dependent inductance and resistance of one or multiple conductors a magnetoquasistatic approach can be used. Therefore, the conductors are divided into filaments with small rectangular cross-sections. The current density is assumed constant and flowing along the length of the filament. Based on an integral formulation for the magnetic vector potential the resistance and partial inductance matrix for the filaments can be calculated [43]. However, since this approach does not account for dielectric displacement current it can only be used in situations where capacitive coupling is negligible, and has therefore only a limited applicability in interconnect analysis.

9.4 Partial Element Equivalent Circuits

In the partial element equivalent circuit (PEEC) method the interconnection network is modeled as a passive RLC circuit with partial inductances and capacitances calculated from quasistatic (non-retarded) solution of Maxwell's equations. Therefore, the electric field $\boldsymbol{E}(\boldsymbol{r},t)$ is modeled using a scalar potential $\varphi(\boldsymbol{r},t)$ and a vector potential $\boldsymbol{A}(\boldsymbol{r},t)$:

$$\boldsymbol{E}(\boldsymbol{r},t) = -\nabla\varphi(\boldsymbol{r},t) - \frac{\partial}{\partial t}\boldsymbol{A}(\boldsymbol{r},t)\ . \tag{9.7}$$

Using the Lorentz gauge, integral equations for both the scalar and vector potentials can be formulated. Thereby, retardation is neglected and cross-couplings are assumed to happen immediately. This leads to the following equation

$$\gamma\boldsymbol{J}(\boldsymbol{r},t) + \frac{\mu_0}{4\pi}\int\frac{\partial}{\partial t}\frac{\boldsymbol{J}(\boldsymbol{r}',t)}{|\boldsymbol{r}-\boldsymbol{r}'|}dV + \frac{1}{4\pi\varepsilon}\nabla\int\frac{\varrho(\boldsymbol{r}',t)}{|\boldsymbol{r}-\boldsymbol{r}'|}dV = 0\ , \tag{9.8}$$

where $\boldsymbol{J}(\boldsymbol{r},t)$ is the current density, $\varrho(\boldsymbol{r},t)$ the charge density, γ, μ_0, and ε are conductivity, vacuum permeability, and permittivity. The integral equation is solved by discretizing the geometry of the conductors into two- or three-dimensional capacitive and inductive cells. A uniform voltage distribution is assumed for the integration over the capacitive cells, and a uniform current distribution for the inductive cells, respectively.

The obtained circuit models tend to be very large with densely occupied coupling matrices. Therefore, model order reduction techniques may be necessary for efficient application in a circuit simulator.

The method could also be extended for including retardation (called rPEEC) and is then equivalent to full-wave solution of Maxwell's equations [44–47].

9.5 Transmission Line Models

For certain applications lumped models based on extracted parameters are not adequate to describe the circuit behavior and the coupled system must be examined. For low-resistance interconnects in transversal electro-magnetic (TEM) or quasi TEM configuration transmission line models based on the telegraph equation do a good job, provided that the line is homogeneous over its length and it is much longer than the distance to the ground plane or return line [48, 49].

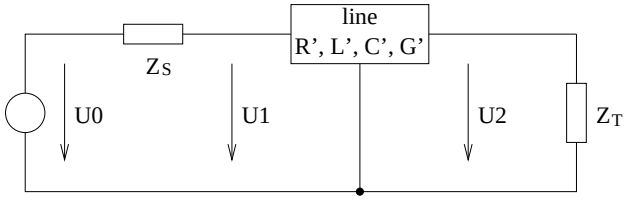

Fig. 9.11. Transmission line model

These models rely on the distributed resistance R', capacitance C', inductance L', and conductance G' of the line (per unit length) and can be expressed by an ODE in frequency domain:

$$\frac{\mathrm{d}}{\mathrm{d}x}I(x) = -(G' + sC')U(x) \tag{9.9}$$

$$\frac{\mathrm{d}}{\mathrm{d}x}U(x) = -(R' + sL')U(x) \tag{9.10}$$

The solution of these equations with boundary conditions as given in Fig. 9.11 is the following transfer function

$$H(s) = \frac{1}{\left(1 + \frac{Z_S}{Z_T}\right)\cosh(\Gamma l) + \left(\frac{Z_S}{Z_0} + \frac{Z_0}{Z_T}\right)\sinh(\Gamma l)}\,, \tag{9.11}$$

with the characteristic impedance $Z_0 = \sqrt{(R' + sL')/(G' + sC')}$ and the propagation coefficient $\Gamma = \sqrt{(R' + sL')(G' + sC')}$.

For higher frequencies skin effect may occur and R', L' get frequency dependent [50, 51]. When the inductance is neglected the telegraph equation becomes a diffusion equation and the solution can be calculated in time domain analytically [52, 53]. For practical applicability in circuit simulations approximations in time domain can be derived by series expansion, moment matching techniques or convolution formulas [54, 55]. The transmission line model can be extended to include cross-talk between lines (multi-wire transmission lines). Also models for lines over lossy substrate [56] are available, which account for slow wave effects in the substrate (Fig. 9.12).

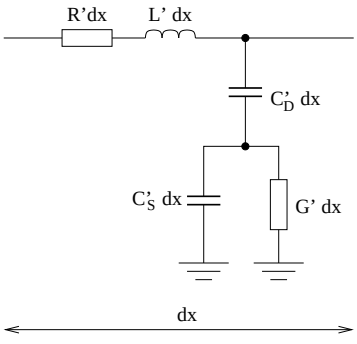

Fig. 9.12. Differential model for transmission lines over lossy substrate

9.6 Three-Dimensional Analysis

To obtain most accurate results for complex geometric structures, Maxwell's equations have to be solved in three dimensions. Depending on the nature of the problem certain simplifications can be made:

Electroquasistatic simulation can be used when the effects of the magnetic field can be ignored (i.e. the resistance dominates over inductance). Therefore, the electric field is assumed to be irrotational and is expressed by a scalar potential. Applications include local and midrange metal interconnects with a small cross-section, polysilicon interconnects and resistors, and the silicon substrate.

An example is given in Fig. 9.13, where the behavior of a pair of polysilicon resistors above a silicon substrate with a lightly-doped epi-layer has been analyzed using FEM [57]. At the time $t = 0$ a voltage step of 1 V has been applied to the left end of the lower line, the upper line is connected to ground. Also the substrate has a ground contact at the left side. The potential is displayed on the surface of the lines and the substrate (blue = 0 V, red = 1 V, green = 0.5 V) after 0.1, 1, 10, and 100 picoseconds. One can observe, that the propagation of the potential in the substrate is much slower than in the lines because of its high resistivity.

Magnetoquasistatic simulation is used when the capacitive displacement current can be neglected (i.e. inductance dominates over capacitance). This approach is commonly used for the calculation of inductances under the influence of the skin-effect, e.g. for printed circuit boards, connectors or packaging. Its applicability for on-chip interconnects is very limited because of the dominant capacitive coupling.

Quasistatic simulation combines the first two methods. Only the time-derivative of the electric displacement is neglected in the first Maxwell equation. Thereby a formation of electromagnetic waves is not possible. This method is applicable when the geometric dimensions of the simulated structure are small compared to the wavelength in the direction perpendicular to the signal propagation, e.g. for low resistive global interconnects and spiral inductors, provided that the operating frequency is not too high.

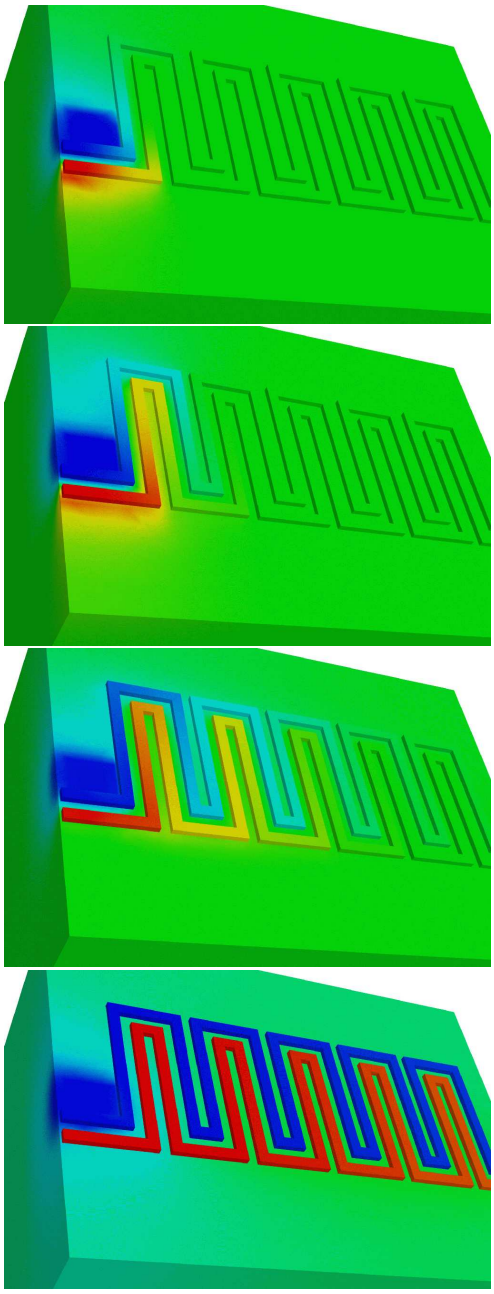

Fig. 9.13. Electroquasistatic simulation of a pair of polysilicon resistors over lossy substrate

All of the above simulation modes can be expressed by Poisson equations, which can be solved with finite element or finite difference or boundary element discretization schemes in time or frequency domain. Also (non-retarded) PEEC belong to this group of methods.

Full-wave simulation takes the complete set of Maxwell's equations into account. Such models are required when distributed electromagnetic effects can no longer be described in terms of "static" values of resistances, inductances, and capacitances (e.g. an integrated spiral inductor where skin-effect, losses in the substrate and radiation effects have to be considered). Usually the equations are solved in the frequency domain, e.g. [44]. Time domain solutions are possible but may lead to numeric instabilities and boundary conditions may be difficult to model, especially for radiation. The finite differences time domain method (FDTD) or box/surface integration method [58, 59] are commonly used for this purpose. The method is quite CPU intensive and only small parts of the layout can be simulated. A better performance can be reached with hybrid methods based on model reduction techniques [60].

9.7 Model Order Reduction

The discretization of three-dimensional partial differential equations leads to a large system of ODEs or a large lumped R(L)C network. Most discretization methods like FEM, FDM, BEM, or PEEC require spatial oversampling to ensure accurate results and therefore yield a model with a very high number of state variables. It is not efficient to incorporate such a model directly into a circuit simulation, because of its large memory and CPU time requirements. The representation must be considerably compressed through reduced order modeling techniques to generate a macro-model with a lower complexity. The reduced order model should capture with sufficient accuracy the input-output behavior of the original system in the desired frequency range and should have efficient representations in both time and frequency domain.

Large resistance-only, inductance-only, or capacitance-only networks can always be reduced exactly to a minimum sized network, that consist only of elements between the terminal nodes, simply by eliminating the inner nodes. For networks with mixed elements model order reduction is usually performed by projecting the system matrices into smaller "sub-spaces" e.g. by Padé approximation [61]. Therefore, the time domain transient response is approximated in terms of a small number of dominant poles in the frequency domain. This is accomplished by asymptotic waveform evaluation (AWE), which provides a generalized approach to waveform estimation for RLC circuits with initial conditions and non-zero input signal rise times [62]. For the calculation of the reduced order model only matrix-vector product or linear equation solvers are needed, hence a good efficiency is reached [63]. However, since with this method only poles are obtained and not an approximating circuit it cannot be used directly in a standard circuit simulator. Another

drawback of AWE is that numerical stability cannot be guaranteed, which may lead to nonphysical oscillations during simulation.

Besides AWE, numerous other model order reduction techniques have been reported including PVL [64], complex frequency hopping [65], the Arnoldi algorithm [66], moment preserving reduction [67], successive node removal [68], PRIMA [69], and a reduction method specifically designed for rPEEC models [46].

All of the above mentioned model order reduction techniques may of course only be applied to linear systems. They are only necessary if numerous simulation runs are required, since their numerical effort is comparable to or larger than one direct solution of the full system.

9.8 Reliability

Reduced wire cross-sections imply higher current densities resulting in an increasing power-loss density and thus higher temperatures. Thermal simulation becomes necessary to find a limit for the maximum current in a wire [70]. This is especially important for low-k materials which have a smaller thermal conductivity than oxide and for Silicon-On-Insulator (SOI) chips, since the heat transfer through the insulating oxide causes increased temperature [71]. Thermal simulations are of utmost importance for electrostatic discharge (ESD) protection circuits [72], because during an ESD event temperature can rise above the melting point of Al for some nanoseconds.

To calculate the transient temperature profile $T(\boldsymbol{r}, t)$, the heat conduction equation

$$\nabla(\gamma_T \nabla T(\boldsymbol{r}, t)) = c_p \rho_m \frac{\partial T(\boldsymbol{r}, t)}{\partial t} - p(\boldsymbol{r}, t) \tag{9.12}$$

has to be solved numerically. Here, γ_T, c_p, and ρ_m are the thermal conductivity, the specific heat, and the specific mass, respectively. The powerloss density $p(\boldsymbol{r}, t)$ is obtained by simulation of the electrical system. Since the electrical and thermal conductivities of many materials depend on the temperature the problem is non-linear, and the simulation of the electrical system cannot be separated from the thermal system.

Adiabatic approximations are only possible for very short pulses (a few nanoseconds) [73]. For accurate simulation of the steady state temperature the simulation area has to be rather large. If the chip is not mounted directly on a good thermal conductor it may be necessary to include package and pins [74].

Analytic thermal models can be developed for certain structures [75] but must be calibrated by numeric simulation.

To include thermal models in circuit simulation it is possible to simulate an equivalent thermal circuit, where temperature is replaced by a voltage and heat flow by an electric current. Similar to the calculation of electrical

resistances and capacitances also thermal resistances and capacitances can be extracted [76].

Interconnects exposed to high current densities for a long time (e.g. power supply lines) are susceptible to electromigration. Electromigration is a complex directional diffusion process whose driving force is the current density, but is accelerated by elevated temperatures. The knowledge of current density and temperature distribution is therefore the base for reliability analysis.

In Fig. 9.14 an example of a via structure in a Cu-dual-damascene architecture with a TiN barrier stressed under a high current density is shown. The bottom of the Si-substrate is kept at constant temperature of 24°C. The hottest spot ($T = 367$ K) is detected on the rightmost via, near the TiN-barrier. The high resistivity of the TiN barrier causes a large voltage drop at the bottom of the via resulting in a high heat generation rate. Due to the nature of the Poisson equation the locations of the maxima in temperature correspond well to the regions of high heat generation, but the actual temperature value is also very sensitive to the thermal boundary conditions. The results have been obtained using FEM simulation [77].

9.9 Design

Interconnect parasitics extraction is most important for post layout verification. Simple geometric models are sufficient in most cases. Only for "critical nets" highly accurate three-dimensional simulation is required. However, with higher clock frequencies and increasing total interconnect length also the number of critical nets increases and the need for highly accurate models will become more evident.

The correction of the errors detected during the post layout verification process may introduce new errors that have to be corrected again. As the number of critical nets rises, it is more likely that errors occur and the rerouting/verification loop has to be repeated many times, which will make the design process inefficient and costly. Therefore, the parasitics of the interconnects have to be considered during the design phase at the earliest possible stage, e.g. device placement and routing. Since at this stage the full topographic information of the interconnect stack is not yet available, the models have to make certain assumptions based on statistical information. These models should give an estimate of the delay caused by the interconnects and their impedance. Optimization should be performed on minimum signal delay during placement, also the driver sizes must be tuned to minimize delay and to prevent ringing. For long global interconnects the signal delay can also be reduced by the insertion of repeaters. However, optimizing a net for minimum delay increases the power loss, therefore for non-critical nets optimization strategies, that minimize the power consumption are required. Advanced design strategies have to account for the distributed nature of the

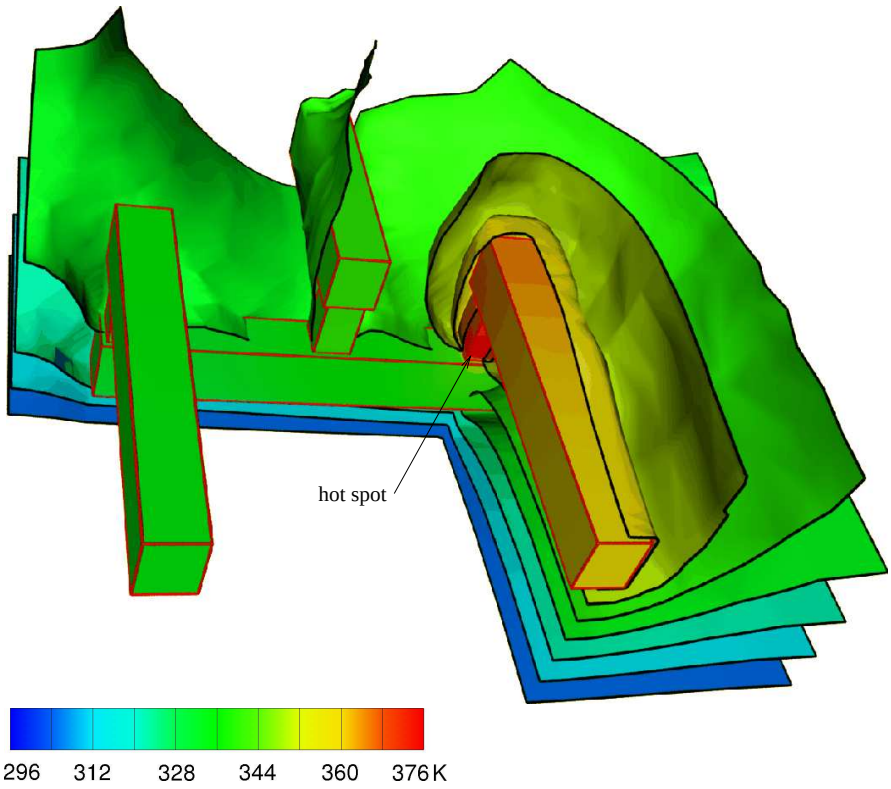

Fig. 9.14. Thermal analysis of a via structure. The temperature is shown on the surface of the interconnects and as contour faces in the dielectric

interconnect parasitics and should include inductance at least for the global lines [78–81].

To reduce the inductance of wires shielding planes or lines, that are connected to ground or supply voltage can be used. Thereby, the calculation of the inductances is greatly simplified because the current return path is defined. Also, the capacitive cross-talk to other wires is reduced, however, the total capacitance is increased. For low aspect-ratio wires shielding planes in the layers above and below the active lines are used, while for high aspect-ratios shielding wires in the same layer between the active lines are more adequate (Fig. 9.15).

Another approach to reduce inductance which is particularly suited for global buses is the shifted insertion of inverters (cf. Fig. 9.16). For long interconnects repeaters have to be used anyway in certain intervals. Instead of repeaters, one can use an even number of inverters. Their location is shifted for the half length of the interval for every second line. Since the direction of the current is reversed by every inverter, the magnetic fields are partially

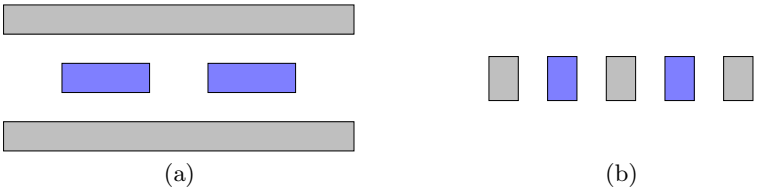

Fig. 9.15. Shielding planes (a) or wires (b) reduce the inductance of the active wires (blue) and minimize the cross-capacitance

canceled. Both, self and mutual inductances are reduced and the wires can be modeled as RC lines without introducing a large error. However, this approach results also in a higher power dissipation and increased chip area.

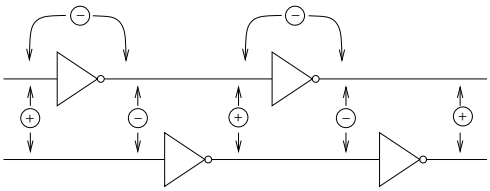

Fig. 9.16. Shifted insertion of inverters helps to reduce self and mutual inductances

9.10 Software

Basic requirements for practically useful simulation software are stability and accuracy. The accuracy must be known and controllable (runtime/accuracy-tradeoff). The simulation process should be as automated as possible. Since user-interaction may introduce errors it should be kept to an absolute minimum.

Therefore, the interconnect simulators should automatically identify critical nets and select appropriate models. To reduce the required CPU time the simulation domain can be divided into several regions applying models of different complexity according to the necessity on accuracy. An example is given in Fig. 9.17, where a non-linear device model is used for the MOS transistor, a full-wave model for a geometrically complex interconnection network, a transmission line model for a long straight line, and a single lumped capacitor for the gate.

The challenging task is to develop a general algorithm for automatizing this partitioning process and to find suitable models for the interfaces [82,83], because high frequencies cause complex interaction between structures, that traditionally could be analyzed separately.

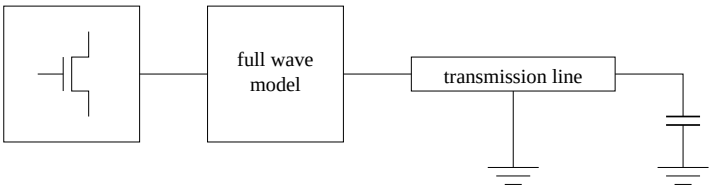

Fig. 9.17. Example of an hierarchical model

Commercial TCAD vendors present a wide range of solutions for interconnect simulations. These tools (e.g. [84–89]) provide R(L)C extraction, SPICE netlist generation, Poisson equation solvers, FDTD full-wave simulators, and furthermore some features, as e.g. simple electromigration models [90] are also offered.

9.11 Conclusion and Outlook

With the exponential progress in semiconductor technology also the requirements on modeling and simulation increase. According to the year 2000 update of the International Technology Roadmap for Semiconductors [91] the 90 nm technology node will be reached in the year 2004. The interconnect structure of a typical microprocessor will consist of 7–8 metal layers with current densities up to $9.6 \cdot 10^5$ A/cm^2. For the 30 nm node in the year 2014 ten metal layers with current densities up to $4.6 \cdot 10^6$ A/cm^2 are predicted. Joule heating due to increased power dissipation, current crowding effects, and the increasing importance of inductance make simulation most important.

In summary we can find three starting points for further reducing and controlling parasitic effects namely design, simulation, and materials.

Regarding design new routing strategies that better account for transmission line effects, the introduction of ground planes or shielding wires will help to control on-chip inductive effects.

Aggressive design rules with reduced safety margins require more accurate models. Therefore, numerical simulation has become indispensable and new simulation methods are required which are more accurate, efficient, robust, and flexible.

A lot of promising approaches have been reported in the literature, however, there is still some effort needed to implement these methods in a stable and generally applicable way. Therefore, commercial vendors will need some time to catch up until these models will be available in their simulators. Improved computational methods together with advanced performance of next generation computers will help to keep pace with the increasing demand on numerical simulation.

The migration from Aluminum to Copper lowers the interconnect resistivity by 40 % [92]. Together with the introduction of low-k dielectrics the RC

time constant can be reduced maximally by a factor of 6. However, decreased resistance and capacitance will bring out inductance effects more intensively, thus increasing the importance of numerical inductance extraction methods.

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