Separated carrier injection control in carbon nanotube field-effect transistors

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The ambipolar behavior limits the performance of carbon nanotube field-effect transistors. A double-gate device is proposed to suppress this behavior. In this device, the first gate controls carrier injection at the source contact and the second one controls carrier injection at the drain contact, which can be used to suppress parasitic carrier injection. The effect of the second gate voltage on the performance of the device has been investigated. Our results indicate that by applying a proper voltage range to the second gate, improved device characteristics can be achieved. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1897491]

Carbon nanotubes (CNTs) have emerged as promising candidates for nanoscale field-effect transistors. The contact between metal and CNT can be of ohmic[1] or Schottky type.[2,3] In this work we focus on Schottky contact carbon nanotube field-effect transistors (CNTFETs). These devices operate by modulating the transmission coefficient of carriers through the Schottky barrier at the metal-CNT interface.[3,4] However, the ambipolar behavior results in performance limitation.[2,5–7] In order to suppress this behavior, an asymmetric single-gate (SG) device has been proposed,[6] where the gate is not extended to the drain and the control of the gate over carrier injection from the drain is reduced. As a result the ambipolar behavior decreases to some extent.[6]

In this work a double-gate (DG) device is proposed, where the first gate controls carrier injection at the source contact and the second one independently controls carrier injection at the drain contact. We show that by applying a proper voltage range to the second gate, parasitic carrier injection at the drain can be avoided and improved device characteristics are achieved. Our results indicate that the DG device shows better performance than the asymmetric SG device.

For a fair comparison we used the same methodology for simulation, as presented in Ref. 6. Assuming ballistic transport, the drain current is calculated using the Landauer–Büttiker formula and the transmission coefficient of carriers is calculated using the WKB approximation.[8] We consider ambipolar devices, where the metal Fermi level is located in the middle of the CNT band gap at each contact. All our calculations assume a CNT with 0.6-eV band gap, corresponding to a diameter of 1.4 nm.[4]

In symmetric SG devices, in which the gate extends from the source to the drain, when the drain voltage becomes higher than the gate voltage the barrier for holes at the drain is suppressed. As a result the tunneling current of holes, which has a detrimental effect on the performance of the device, increases. To suppress this current component an asymmetric SG device, as shown in Fig. 1(a), has been proposed.[6] In this device the gate controls carrier injection at the source, the effect of the gate voltage on the band-edge profile near the drain is reduced, and as a result the parasitic tunneling current decreases. However, even in this device the barrier for holes at the drain is reduced and the parasitic current increases, see Fig. 3, if the difference between the gate and drain voltages becomes high, as shown in Fig. 2. To

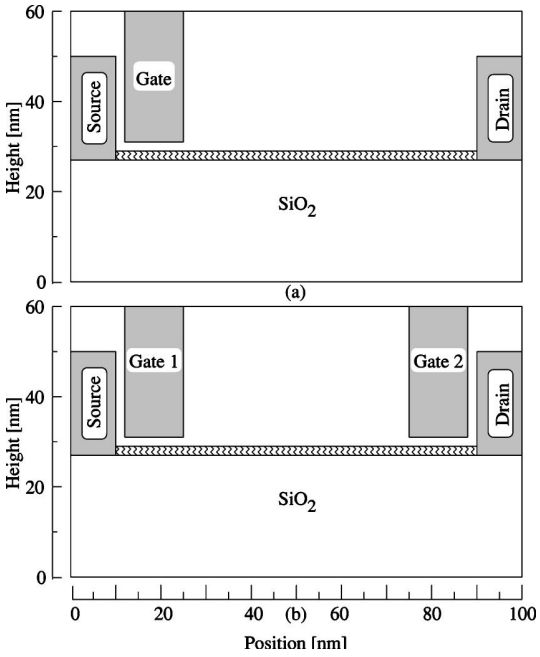

FIG. 1. (a) Sketch of the symmetric SG device. (b) Sketch of the DG device. The gate oxide thickness is 2 nm for both devices.

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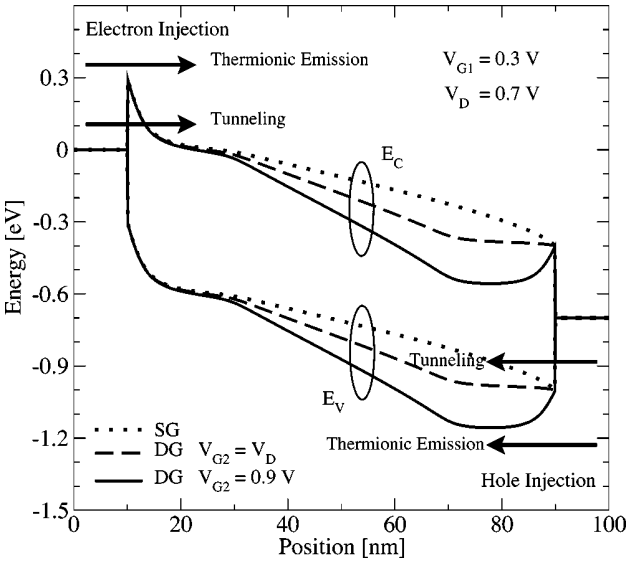

FIG. 2. The band-edge profile for the asymmetric SG device (dotted lines), the DG device with $V_{G2}=V_D$ (dashed lines), and the DG device with V_{G2} =0.9 V (solid lines).

avoid this problem we propose a DG device, as shown in Fig. 1(b). In this device the band-edge profiles near the source and drain are controlled separately.

In order to suppress the tunneling current of holes at the drain it is necessary that the voltage of the second gate be equal or higher than the voltage of the drain; therefore, we consider two possibilities for the second gate voltage:

(a) Applying the same voltage as the drain voltage.
(b) Applying a constant voltage higher than the maximum drain voltage.

If the drain voltage is applied to the second gate, at any drain voltage the band-edge profile near the drain will be nearly flat, as shown Fig. 2. In consequence the parasitic tunneling current of holes is suppressed and the parasitic current is limited to thermionic emission of holes over the Schottky barrier at the drain, as shown in Fig. 3. While electron injection at the source contact can be controlled through the first gate, the second gate suppresses parasitic hole current at the drain contact. The same discussion holds for *p*-type devices. By applying negative voltages to the first gate, hole injection at the source contact can be controlled and the second gate suppresses parasitic electron current at the drain contact. A CNTFET can be operated as an *n*-type or *p*-type device just by reversing the polarity of the applied voltages.[6]

By applying a voltage higher than the maximum drain voltage to the second gate (see Fig. 2), the thermionic emission current of holes at the drain contact will decrease exponentially and consequently, a lower parasitic current can be achieved, see Fig. 3.

The output characteristics of the DG structure for these two options are shown in Fig. 4. If the second gate is biased at the drain voltage, the drain current will be small until the drain voltage reaches the first gate voltage. The reason of this behavior is that in this case the band-edge profile near the

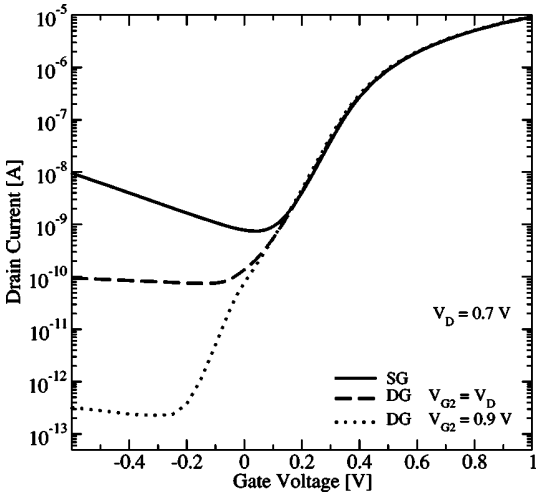

FIG. 3. Transfer characteristics for the SG device (solid line), the DG device with $V_{G2}=V_D$ (dashed line), and the DG device with $V_{G2}=0.9$ V (dotted line). For both devices $V_D=0.7$ V.

drain contact is nearly flat; therefore at low drain voltages, as shown in Fig. 5, injected carriers from the source have to overcome a thick barrier until the drain voltage reaches a voltage higher than the first gate voltage. The output characteristics of the asymmetric SG device are also very similar to this case. If the second gate is biased at a voltage higher than the maximum drain voltage, injected carriers from the source have to overcome a thin barrier even at low drain voltages and as a result, the drain current will be higher. The comparison of current–voltage characteristics of the asymmetric SG and DG structures shows that the proposed DG structure shows improved device characteristics, which are necessary for future nanoelectronic applications.

Regarding the separation between the two gates, several parameters should be considered: By decreasing this separation, the parasitic capacitance between the gates increases which deteriorates the frequency response of the device. Also, because of narrow band gap in CNTs at fixed operating

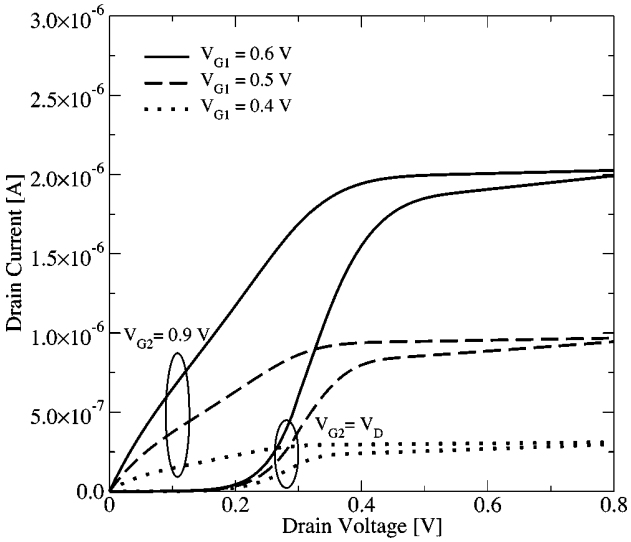

FIG. 4. Output characteristics for the DG device with $V_{G2}=V_D$ and the DG device with $V_{G2}=0.9$ V , $V_D=0.7$ V.

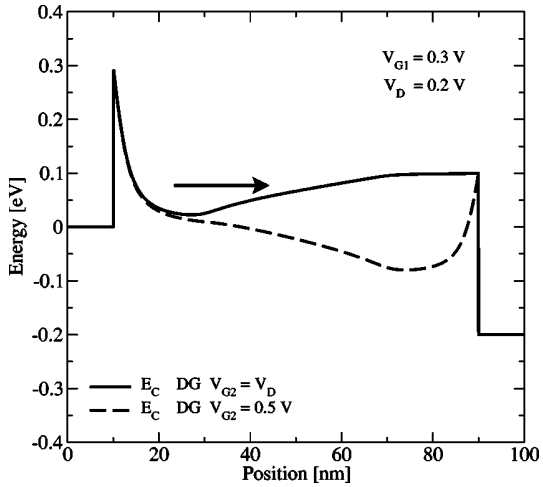

FIG. 5. Conduction-band edge for the DG device with $V_{G2}=V_D$ (solid line) and DG device with $V_{G2}=0.5$ V (dashed line).

voltages by decreasing this distance, the band to band tunneling current will increase which affects the device characteristics.[9]

In (Ref. 10) a split gate structure has been implemented. Although this structure was used as a *pn* diode, it shows that by controlling the band-edge profile near the source and drain contacts, better device characteristics can be achieved.

We demonstrated that in a DG structure the first gate controls the carrier injection at the source contact and the second gate can be used to suppress parasitic carrier injection at the drain contact. We considered the cases where either the drain voltage or a constant voltage higher than the maximum drain voltage can be applied to the second gate. It is of advantage to apply the drain voltage to the second gate because parasitic capacitances between the second gate and the drain are avoided, no separate voltage source for the second gate is needed, and the fabrication is more feasible. The off current is determined by the thermionic emission current over the Schottky barrier. The drain current, however, is small until the drain voltage reaches a value higher than the first gate voltage.

By applying a voltage higher than the maximum drain voltage to the second gate, a high I_{on}/I_{off} ratio can be obtained. However, for both of these methods, better device characteristics as compared to the asymmetric SG device are achieved.

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