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Applications of Two- and Three-Dimensional General Topography Simulator in Semiconductor Manufacturing Processes

A. Sheikholeslami°, R. Heinzl△, S. Holzer△, C. Heitzinger†, , M. Spevak△,
M. Leicht+, O. Häberlen+, J. Fugger+,
F. Badrieh⋆, F. Parhami⋆, H. Puchner⋆,
T. Grasser△, and S. Selberherr°
°*Institute for Microelectronics, TU Vienna, A-1040 Vienna, Austria*
△*Christian Doppler Laboratory for TCAD at the Institute for Microelectronics*
†*School of Electrical and Computer Engineering, Purdue University, USA*
+*Infineon Technologies, Villach, Austria*
⋆*Cypress Semiconductor, USA*
sheikholeslami@iue.tuwien.ac.at

Abstract

We present applications of the two- and three-dimensional general purpose topography simulator ELSA *(Enhanced Level Set Applications) for semiconductor manufacturing processes. The first process considered is the deposition of silicon dioxide from* TEOS *for power* MOSFETs*. For backend processes in addition to a* TEOS *process, the deposition of silicon nitride into interconnect lines, where two and three-dimensional void characteristics play an important role for determining timing delays and cracking effects, is necessary and thus is simulated.*

1. Introduction

During the fabrication of an IC (Integrated Circuit) a wafer has to undergo many processes. Each process accomplishes a specific change in the state of the wafer. Some of these processes can be described using relatively simple models. However, many processes require more complex models to be developed reliably. Process modeling and simulation have been used generally for principal understanding and not for quantitative prediction of processes. Therefore, for more general prediction and analysis, a topography simulator must use detailed descriptions of chemical reactions with chemical reaction rates and thermodynamic properties of species obtained by experiment and/or by calculation. However, in spite of the complexity of these models, their quantitative predictability is still limited for processes of industrial interest. Therefore, the simpler calibrated sticking coefficient models provide good alternatives for process investigations and especially for time-consuming optimization and inverse modeling tasks. Inverse modeling and parameter estimation are achieved using SIESTA (Simulation Environment for Semiconductor Technology Analysis) [1].

The RC timing delays stemming from metal lines in interconnect structures are contribute increasingly to the overall delays in IC as its dimensions are decreased incredibly with shrinking technologies. For proper modeling these delays, the knowledge about metal profile, the profile of deposited layers, and the profile of the void, is very essential. As our studies in two dimensions have shown, a void has significant influence on the timing delays and can substitute expensive low-k material in a controlled and reproducible way [2]. However, for the prediction of cracking effects which strongly depends on the void characteristics, a two-dimensional void characteristic is not sufficient and the three-dimensional behavior must be considered.

The outline of this paper is as follows: first, a brief description of the level set method used for implementation of an efficient and fast simulator is presented. Secondly, we present a model which gives good agreement of simulation results with measurements from a TEOS process. This model avoids the complex reactor-scale and surface reaction models. Finally, three-dimensional investigations of void characteristics and their dependence on metal profile is presented. This profile plays an important role for predicting the cracking effects.

2. The Level Set Method

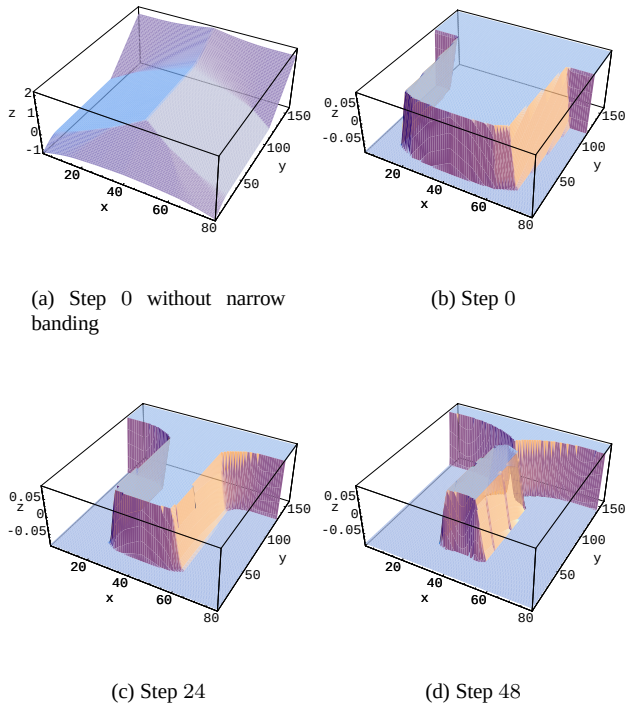
The level set method [3] provides means for describing boundaries, i.e., curves, surfaces or hypersurfaces in arbitrary dimensions, and their evolution in time which is

caused by forces or fluxes normal to the surface. The basic idea is to consider the curve or surface in question at a certain time t as the zero level set (with respect to the space variables) of a certain function $\varphi(t, \mathbf{x})$, the so called level set function. Thus the initial surface is the set $\{\mathbf{x} \mid \varphi(0, \mathbf{x}) = 0\}$.

Each point on the surface is moved with a certain speed normal to the surface and this determines the time evolution of the surface. The speed normal to the surface will be denoted by $F(t, \mathbf{x})$. The surface at a later time t_1 shall also be considered as the zero level set of the function $\varphi(t, \mathbf{x})$, namely $\{\mathbf{x} \mid \varphi(t_1, \mathbf{x}) = 0\}$. As shown in [3], this leads to the level set equation

$$\varphi_t + F(t, \mathbf{x}) \|\nabla_{\mathbf{x}} \varphi\| = 0, \qquad \varphi(0, \mathbf{x}) \quad \text{given},$$

in the unknown variable φ, where $\varphi(0, \mathbf{x})$ determines the initial surface. Having solved this equation the zero level set of the solution is the sought curve or surface at all later times. One of the most important techniques used in ELSA is the narrow banding technique which stems from observing that only the values of the level set function near its zero level set are essential and they only have to be calculated at the grid points in this narrow band around the zero level set. The simulation results of a deposition process into a rectangular trench as the initial structure including the narrow banding technique are shown in Figure 1. We refer to [3] for more details regarding the level set method and other techniques which have been used for the implementation of ELSA.



(a) Step 0 without narrow banding

(b) Step 0

(c) Step 24

(d) Step 48

Figure 1. The level set functions at step 0, 24, and 48 during the simulation of a deposition process. Inside the narrow band the level set function is retained until the end of simulation, whereas level set function values of the other points have been substituted with the width of the narrow band multiplied by 1 or -1 depending on their position.

3. The Model for Inverse Modeling a TEOS Process

Before introducing the model, it is important to note that we only performed the parameter estimation for the low aspect ratio trench from a set of trenches with different aspect ratios. The best model is a model whose parameters extracted from the measurements of a TEOS process for a low aspect ratio trench give simultaneously the best agreement for the measurements of the highest aspect ratio.

In [4] a set of our attempts for finding the best model during the inverse modeling has been presented. We only present here the best model. The model is based on two species that take part in a TEOS deposition reaction as has been suggested in [5], of course, with some differences compared to our model. Here the second species is the by-product of the reaction of a particle of the first species with the surface. The flux of the second species is proportional to the flux of the first species, but the sticking probabilities of both species are constant. This model shows excellent agreement with SEM images as shown in Figure 2 and Figure 3.

4. Two-Dimensional Interconnect Capacitance Simulations

In the process considered the films deposited as ILD (Interlayer Dielectric) are silicon nitride and silicon dioxide films. Figure 4 shows a whole backend stack comprised of three different metal lines M1, M2, and M3, bottom-up, respectively. In order to model capacitances, we assume that a signal line is at high voltage and surrounded by two lines on the left, two lines on the right, a plane underneath, and a plane above. The surrounding lines and planes are assumed to be at ground voltage. For example an M2 signal line could be surrounded by M2 grounded lines above the M1 plane and underneath the M3 plane. This skeleton is shown in Figure 5. Most RCX (Resistance and Capacitance Extraction) tools have very simplistic void models. Even if the metal slope is modeled, it is mostly assumed constant and independent of space. This is insufficient for today's technologies where interconnects have a large number of special features which are nowhere close to ideal [2].

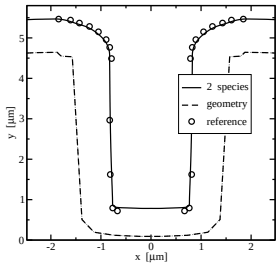


Figure 2. Comparison between simulation and measurement for the two species model for a trench with a low aspect ratio.

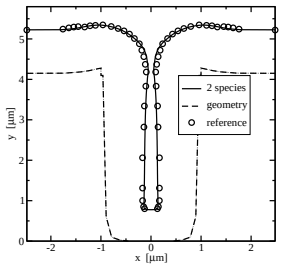


Figure 3. Comparison between simulation and measurement for the two species model for a higher aspect ratio.

Figure 6 shows the simulation result of void formation at 90μm line-to-line spacings where the slopes of metal lines have been assumed to dependent on line-to-line spacings. A very good agreement between the simulations and measurements of M3 line capacitances with an error of less than 5% has been achieved as shown in Figure 7.

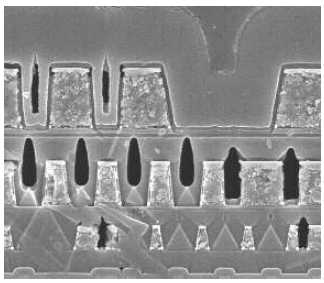


Figure 4. SEM image of a whole backend stack comprised of three Al metals and a Ti-nitride interconnect.

5. Prediction of Cracking Effects Based on Void Characteristics

Figure 8 shows a schematic of three-dimensional structure used in our investigations. The geometrical parameters for which we obtain the void characteristics, are line-to-line spacings (S), metal thickness (T), metal width (W),

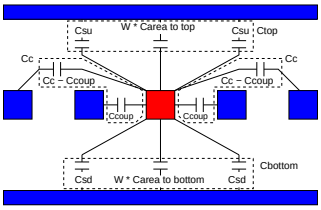


Figure 5. Two-dimensional schematics of a signal line (middle) surrounded by grounded lines and planes.

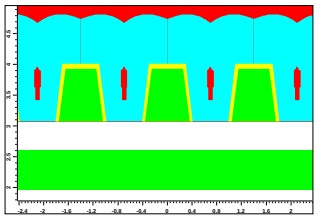


Figure 6. Simulation of void formation by M3 lines at 0.90μm space above the M2 plane.

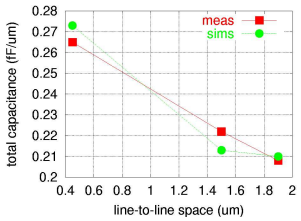


Figure 7. Comparison between simulation and measurement of M3 middle line capacitance as a function of line-to-line spacings.

displacement parameter (L), and a diagonal parameter (P). The last two parameters demonstrate the pronounced three-dimensional effects.

Since our simulations [6] have shown that the metal width does not play an important role by void characteristics, it will be held constant during all investigations. The first set of simulations was performed for different line to line spacings holding the metal thickness at $T_1 = 0.845\mu$m and $T_2 = 1.045\mu$m. The deposited layers were silicon dioxide and silicon nitride with thickness of $D_1 = 0.1\mu$m and $D_2 = 0.9\mu$m, respectively.

For analyzing cracking effects we introduce a parameter C which is shown in Figure 9. The simulations have shown generally that increasing S shifts the void upwards while it simultaneously decreases C as can be seen by a comparison between Figure 9 and Figure 10. In addition, increasing S causes the void to be wider (cf. Figure 9 and Figure 10).

We now introduce the parameter P whose variation results pronounced in three-dimensional effects. Because $P = \sqrt{S^2 + L^2}$ is not a single-valued function of S and L as shown in Figure 8, talking about dependence of C on P is

difficult. Therefore, it is very important to have a profile of C depending on S and L that can lead to the same P with different combinations. These investigations have led to a profile of C as shown in Figure 11. The profile predicts C and therefore enables process engineers to choose the optimal geometrical parameters for avoiding cracks. The cracks are avoided by choosing C as large as possible because the smaller C the more probable are cracking effects.

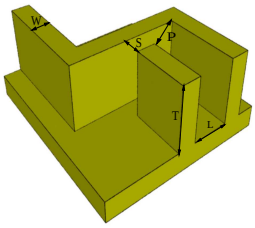


Figure 8. Schematic of the investigated three-dimensional interconnect structure.

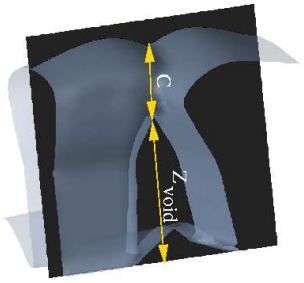


Figure 9. Void formation during deposition into an initial structure with $S = 0.72\mu\mathrm{m}$ and at T_2.

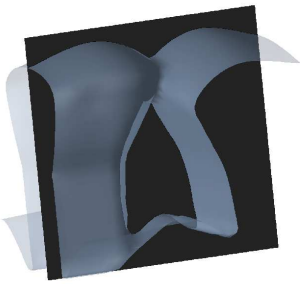


Figure 10. Void formation during deposition into an initial structure with $S = 1\mu\mathrm{m}$ and at T_2.

6. Conclusion

State of the art algorithms for surface evolution in two and three dimensions have been implemented. Using inverse modeling a model for deposition of a TEOS process has been implemented, which agrees very well with measurements. A set of three-dimensional investigations for different geometrical parameters has been performed and presented. How these different geometrical parameters affect void characteristics and subsequently a cracking measure C has been presented. Using C the cracking effects can be predicted, since the smaller C the more probable are cracking effects. To some extent low-K material can be substituted with interconnect designs making use of voids.

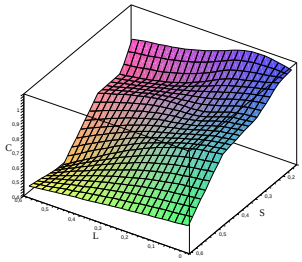


Figure 11. Dependence of C on S and L.

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