# Applications of Two- and Three-Dimensional General Topography Simulator in Semiconductor Manufacturing Processes

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## Abstract

*We present applications of the two- and three-dimensional general purpose topography simulator ELSA (Enhanced Level Set Applications) for semiconductor manufacturing processes. The first process considered is the deposition of silicon dioxide from TEOS for power MOSFETs. For backend processes in addition to a TEOS process, the deposition of silicon nitride into interconnect lines, where two and three-dimensional void characteristics play an important role for determining timing delays and cracking effects, is necessary and thus is simulated.*

## 1. Introduction

During the fabrication of an IC (Integrated Circuit) a wafer has to undergo many processes. Each process accomplishes a specific change in the state of the wafer. Some of these processes can be described using relatively simple models. However, many processes require more complex models to be developed reliably. Process modeling and simulation have been used generally for principal understanding and not for quantitative prediction of processes. Therefore, for more general prediction and analysis, a topography simulator must use detailed descriptions of chemical reactions with chemical reaction rates and thermodynamic properties of species obtained by experiment and/or by calculation. However, in spite of the complexity of these models, their quantitative predictability is still limited for processes of industrial interest. Therefore, the simpler calibrated sticking coefficient models provide good alternatives for process investigations and especially for time-consuming optimization and inverse modeling tasks. Inverse modeling

and parameter estimation are achieved using SIESTA (Simulation Environment for Semiconductor Technology Analysis) [1].

The RC timing delays stemming from metal lines in interconnect structures are contribute increasingly to the overall delays in IC as its dimensions are decreased incredibly with shrinking technologies. For proper modeling these delays, the knowledge about metal profile, the profile of deposited layers, and the profile of the void, is very essential. As our studies in two dimensions have shown, a void has significant influence on the timing delays and can substitute expensive low-k material in a controlled and reproducible way [2]. However, for the prediction of cracking effects which strongly depends on the void characteristics, a two-dimensional void characteristic is not sufficient and the three-dimensional behavior must be considered.

The outline of this paper is as follows: first, a brief description of the level set method used for implementation of an efficient and fast simulator is presented. Secondly, we present a model which gives good agreement of simulation results with measurements from a TEOS process. This model avoids the complex reactor-scale and surface reaction models. Finally, three-dimensional investigations of void characteristics and their dependence on metal profile is presented. This profile plays an important role for predicting the cracking effects.

## 2. The Level Set Method

The level set method [3] provides means for describing boundaries, i.e., curves, surfaces or hypersurfaces in arbitrary dimensions, and their evolution in time which is