Influence of Interface and Oxide Traps on Negative Bias Temperature Instability

R. Entner, T. Grasser, H. Enichlmair*, and R. Minixhofer*
Christian Doppler Laboratory for TCAD in Microelectronics at the Institute for Microelectronics,
TU Wien, Gusshausstrasse 27–29/E360, 1040 Wien, Austria
*austriamicrosystems, Tobelbaderstrasse 30, 8141 Unterpremstaetten, Austria
Phone: +43/1/58801/36050, Fax: +43/1/58801/36099, E-mail: entner@iue.tuwien.ac.at

I. INTRODUCTION

The negative bias temperature instability (NBTI) behavior of pMOS structures is a critical reliability concern for modern semiconductor devices. The demand to model the degradation mechanisms as physically as possible is high, as it helps to keep process development time and costs as low as possible. The basic reaction-diffusion (RD) model [1] describes negative bias temperature instability as a combination of a reaction process at the Si/SiO$_2$ interface breaking silicon-hydrogen bonds and the transport of a hydrogen species (e.g. H° or H$_2$) away from the interface. The broken bonds at the interface form fast interface-states which, when positively charged, lead to a severe shift of important transistor parameters as the threshold-voltage (V_{th}) or the saturation-current ($I_{\text{d,sat}}$).

II. ENHANCED NBTI MODEL

In addition to the basic RD model we include the fully dynamic dispersive multiple trapping equations [2] in contrast to the commonly used quasi-equilibrium approximation [3]. Furthermore, we include the forming of distributed oxide charges [4] during the degradation process and thus a second mechanism describing the shift of transistor parameters. The oxide-charges are generated by diffusing H$_2$ which is cracked at oxide defects [5] with H° being trapped and forming slow positive charges.

This enhanced RD model was implemented in the multi-dimensional device simulator MINIMOS-NT [6] and is evaluated self-consistently with the semiconductor equations. The numerical simulations were compared to recent measurement data.

III. RESULTS AND DISCUSSION

The measured device was a high-voltage pMOS structure with a gate oxide thickness of 48 nm which was stressed at 175 °C at -25 V gate voltage. Fig. 2 depicts the simulation results for a 1000 s stress and relaxation cycle with and without the inclusion of oxide traps in the model. It can be clearly seen that during the annealing phase the V_{th}-shift shows two different time constants. During the faster process within the first few seconds the annealing is attributed to re-passivation of dangling Si/SiO$_2$ interface bonds. This process is governed by the availability of mobile hydrogen near the interface. After the consumption of all available hydrogen, shown in Fig. 1, new hydrogen can only be provided by detrapping in the oxide bulk (Fig. 3). Due to the slower time constant of this process a second regime can be seen in Fig. 2.

In Fig. 2 in the “No measurement delay” plot the importance of the inclusion of measurement delays (Fig. 6) during the simulation is highlighted. The fast annealing of interface traps significantly influences the measured degradation. The importance of the self-consistent simulation is highlighted in Fig. 5. The change of the electric field and the hole concentration at the interface is properly accounted for. Fig. 4 shows the linear dependence of V_{th} shift due to interface traps and charged oxide traps to the overall shift. It highlights the correlation between interface state and oxide charge generation.

IV. SUMMARY AND CONCLUSION

We presented the analysis of an enhanced reaction-diffusion model to describe negative bias temperature instability. The model includes dispersive transport for the hydrogen species and the generation of distributed oxide charges during the stress phase. These oxide charges are crucial in the description of the annealing phase. Applying the model in a two-dimensional, numerical device simulation and solving it, for the first time, fully self-consistently with the semiconductor equations the degradation and annealing behavior of a high-voltage pMOS structure could be reproduced and show very good agreement with measurement data.

V. ACKNOWLEDGMENT

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[1] K. O. Jeppson *et al.*, J.Appl.Phys. **48**, 2004 (1977).
[2] J. Noolandi, Phys.Rev.B **16**, 4466 (1977).
[3] B. Kaczer *et al.*, Appl.Phys.Lett. **86**, 143506 (2005).
[4] N. Stojadinovic *et al.*, Microelectron.Reliab. **45**, 1343 (2005).
[5] A. H. Edwards, Phys.Rev.B **44**, 1832 (1991).
[6] *MINIMOS-NT 2.1 User's Guide*, Institut für Mikroelektronik, Technische Universität Wien, Austria, 2004, `www.iue.tuwien.ac.at/software/`.

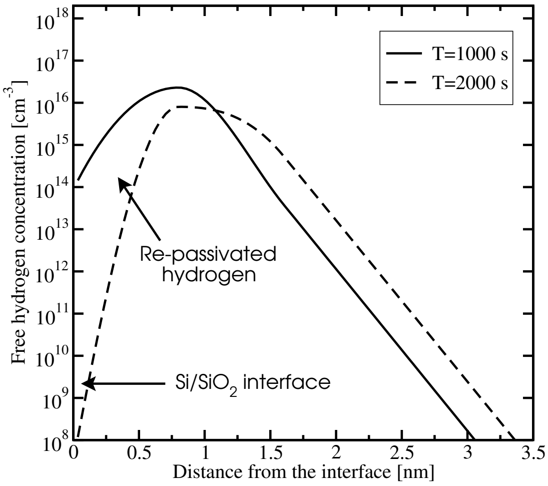

Fig. 1. During the first seconds of the annealing phase the reservoir of free hydrogen close to the Si/SiO$_2$ interface is used for re-passivation of the broken interface bonds.

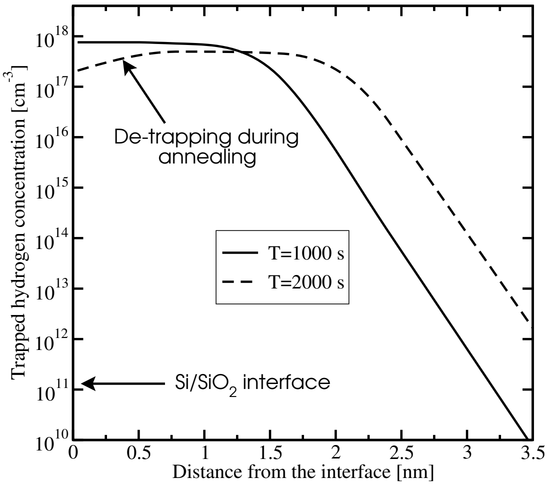

Fig. 3. The de-trapping process during the annealing cycle. Trapped hydrogen is released, removing fixed oxide charges in our model, which leads to re-passivation of interface bonds. The process is assumed to be slower compared to the annealing with mobile hydrogen.

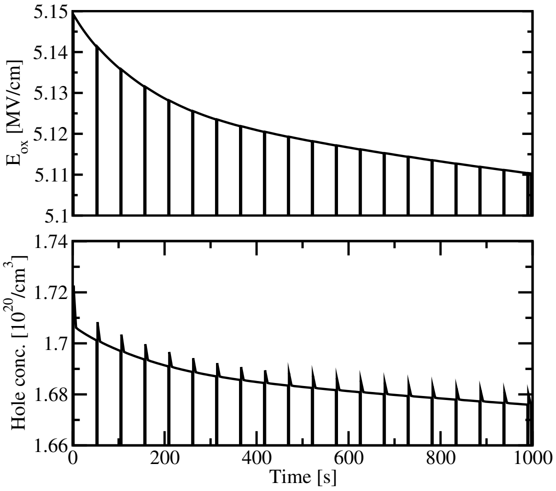

Fig. 5. The model is solved self-consistently with the semiconductor equations. Therefore the changing electric field and the hole concentration at the Si/SiO$_2$ interface are accounted for. The vertical lines depict the rapid change in the electric field during the measurement cycles.

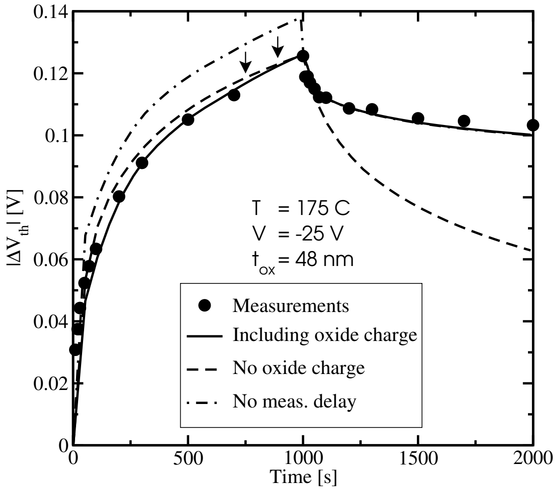

Fig. 2. Comparison of the measurements to the simulation results. The measurements can only be described by properly accounting for the measurement delays during the stress phase and by including the generation of oxide charges.

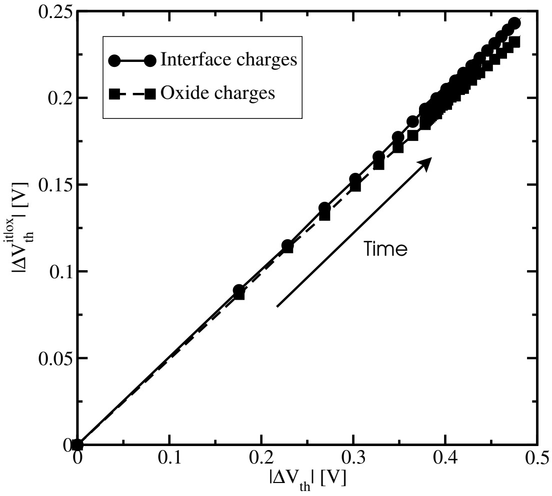

Fig. 4. Interface charge and oxide charge related V_{th} shift versus total V_{th} shift. The linear dependence during the whole measurement cycle shows the correlation between interface-state and oxide-charge generation.

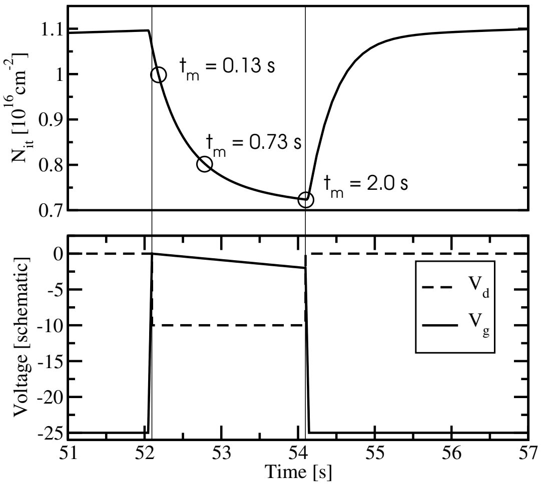

Fig. 6. Simulation of a measurement cycle and the results achieved from three different measurement points. Any delay greatly influences the measurement results.