Demonstration of a Slipstream Simulation Flow Including Device and Circuit Simulators

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Summary: A slipstream design flow from process via device to circuit simulation is proposed. Simulation results of the device simulator Minimos-NT and the circuit simulator Spectre are evaluated. A ring oscillator circuit is used as an example to demonstrate the coherence between these simulators.

Keywords: Device simulations, ECAD, TCAD, SPICE, Spectre, Minimos-NT.

Motivation

Device feature sizes have been reducing over the years and now crossed below 100 nm at the mass-production level. The ultra-deep submicron and nanometer CMOS ULSI technologies imply the use of complex multilevel development paradigms where ECAD and TCAD methodologies play the major role. The challenging demand is to utilize the available technology to the utmost, while reducing design margins. A key modeling goal is to set up a consistent modeling infrastructure from process through device/circuit to systems design level. Adequate modeling and simulation are integral parts of such an infrastructure. Traditionally, technology developers and circuit designers are largely separate entities loosely linked by a set of layout files and SPICE model parameters. In the context of shrinking ULSI technologies the need for consistent modeling flow requires a continuous workbench of simulation and design tools. A ring oscillator circuit simulation is chosen as a particular example to demonstrate the coherence between the simulators Spectre [1] (part of the Cadence CAD system) and Minimos-NT [2] (part of the Viennese Integrated System for TCAD Applications).

Results

The slipstream simulation and design software includes process simulation (TSUPREM4 [3]), device/circuit simulation (Minimos-NT) and circuit simulation (Spectre). The two-dimensional device simulator Minimos-NT is equipped with an extensive mixed-mode circuit capability including modeling of distributed devices [4]. Spectre is an advanced circuit simulator that uses direct methods to simulate analog and digital circuits at the differential equation level.

High-speed operation is a key challenge for lots of novel devices. The average gate delay time of an inverter chain provides a metric for the overall speed of a digital circuit. As an example, a ring oscillator circuit of five inverter chains with the output fed to the input, is used (Fig.1). By determining the oscillation frequency f of such a ring circuit the average gate delay time t_d of one inverter stage can be calculated using $t_d = 1/(2nf)$ with n — number of stages (here $n = 5$).

Minimos-NT simulation results for 0.25μm and 0.13μm technologies are in good agreement with experimental data [5]. Opposite to that, the Spectre model available in our Cadence Design software is calibrated for 0.35μm technology and higher, and therefore, can be applied according to this constraint.

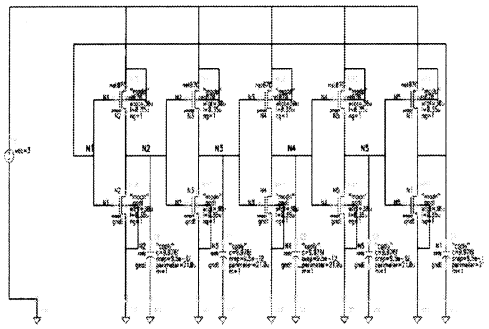

Fig. 1. Circuit diagram of a five stage ring oscillator.

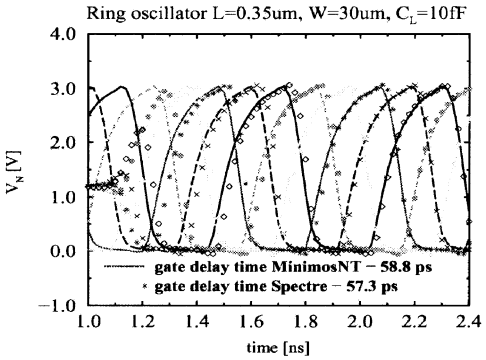

Fig. 2. Node voltages simulated with Spectre and Minimos-NT.

Table I — Simulation results of Minimos-NT and Spectre (with gate length L_g, gate width W_g, load capacitance C_L , and applied voltage V_{DD})

Simulator	No.	L_g [um]	W_g [um]	V_{DD} [V]	C_L [fF]	Δ [ps]	$f = 1/\Delta$ [GHz]	t_d [ps]
Minimos-NT	1	0.35	30	3.0	10	588	1.70	**58.8**
	2	0.25	20	2.5	5.4	295	3.39	29.5
	3	0.13	10	1.5	3.8	152	6.58	15.2
Spectre	1	0.6	30	3.0	10	1140	0.88	114.0
	2	0.6	20	3.0	10	1163	0.86	116.3
	3	0.6	10	3.0	10	1339	0.75	133.9
	4	0.35	30	3.0	10	573	1.74	**57.3**
	5	0.35	20	3.0	10	590	1.69	59.0
	6	0.35	10	3.0	10	640	1.56	64.0

Since our Spectre model is calibrated for 0.35 μm technology and higher, we were able to explicitly compare these results only. As can be seen from Table I, comparable average gate delays per stage t_d are obtained from device/circuit simulation with Minimost-NT (58.8ps) and from Spectre circuit simulator (57.3ps). Fig. 2 shows the simulated node voltages V_N (N=1…5) vs. time resulting from the two simulators. The established setup allows combination of ECAD and TCAD simulation tools in continuous flow, which provides a link from technology development through device development to circuit design.

References

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