Efficient Calculation of Life Time Based Direct Tunneling through Stacked Dielectrics

M. Karner, A. Gehring, and H. Kosina

Institute for Microelectronics, TU Vienna, Gußhausstraße 27–29, A-1040 Wien, Austria
Phone: +43-1-58801/36016, Fax: +43-1-58801/36099, E-mail: karner@iue.tuwien.ac.at

The continuous progress in the development of MOS field-effect transistors within the last years goes hand in hand with down-scaling the device feature size. Therefore, they feature gate oxide thicknesses below two nanometers which suffer from high gate leakage currents. The use of high-k gate dielectrics provides an option to reduce the gate leakage current of future CMOS devices while retaining a good control over the inversion charge [1].

Calculation of tunneling currents is traditionally based on the assumption of a three-dimensional continuum of states at both sides of the dielectric and the conservation of parallel momentum. Using this assumptions, the tunneling current can be described by the Tsu-Esaki formula [2]. In this work, we study the calculation of gate leakage currents in CMOS devices with a SiO_2-high-k dielectric stack in inversion. In contrast to other publications [1] [3] using a Tsu-Esaki based approach, the calculation of direct tunneling currents is performed by the more rigorous life time approach [4]. Assuming quasi-bound states (QBS) with a finite life time yields the current $J_{2\mathrm{D}}$. For energies greater than $\mathcal{E}_{\mathrm{lim}}$, a continuum of states is assumed, which gives rise to $J_{3\mathrm{D}}$ as displayed in Fig. 1. Hence, the Tsu-Esaki formula is replaced by

$$J = J_{2\mathrm{D}} + J_{3\mathrm{D}} = \frac{\mathrm{k_B}T\mathrm{q}}{\pi\hbar^2}\sum_{i,\nu}\frac{g_\nu m_\parallel}{\tau_\nu(\mathcal{E}_{\nu,i}(m_\mathrm{q}))}\ln\left(1+\exp\left(\frac{\mathcal{E}_\mathrm{F}-\mathcal{E}_{\nu,i}}{\mathrm{k_B}T}\right)\right) + \frac{4\pi\mathrm{q}m_{3\mathrm{D}}}{h^3}\int_{E_\mathrm{min}}^{E_\mathrm{max}} TC(\mathcal{E}_x, m_\mathrm{diel})N(\mathcal{E}_x)\,\mathrm{d}\mathcal{E}_x\ ,$$

where g_ν denotes the valley degeneracy, $m_\parallel$ the parallel mass, and m_q the quantization masses, which enters the SCHRÖDINGER equation, and $\tau_\nu(\mathcal{E}_{\nu,i})$ the life time of the quasi-bound state $\mathcal{E}_{\nu,i}$. For the calculation of direct tunneling in [100] silicon MOS structures, $J_{2\mathrm{D}}$ must be evaluated two times using $g_\nu = 2$, $m_\parallel = m_\mathrm{t}$, $m_\mathrm{q} = m_\mathrm{l}$, and $g_\nu = 4$, $m_\parallel = \sqrt{m_\mathrm{l} m_\mathrm{t}}$, $m_\mathrm{q} = m_\mathrm{t}$. Tunneling from the continuum is taken into account by evaluation of the Tsu-Esaki formula, starting from the energy $\mathcal{E}_{\mathrm{lim}}$, where $TC(\mathcal{E}_x)$ is the transmission coefficient of the barrier (see Fig. 2) and $N(\mathcal{E}_x)$ the supply function.

The major source of tunneling electrons in the inversion layers of MOS-structures is due to QBS [5] which follows from the SCHRÖDINGER equation. Within this work a method based on the perfectly matched layer formalism (PML), which has been been applied successfully for band structure calculations in III-V heterostructure devices [6], has been used to determine the life time broadening of the QBS. It is based on a complex coordinate stretching to introduce artificial open boundary conditions in the SCHRÖDINGER equation [7]. Inserting the stretched coordinate $\tilde{x} = \int_0^x s_x(\tau)\,\mathrm{d}\tau$ leads to $\partial/\partial\tilde{x} = 1/s_x(x)\partial/\partial x$. Within the PML region the stretching function $s_x(x)$ is given as $s_x(x) = 1 + (\alpha + \imath\beta)x^n$, with $\alpha = 1$, $\beta = 1.4$, and $n = 2$, while it is unity in the physical region. This procedure prevents reflections at the boundary of the physical region (see Fig. 3) and, therefore, the resulting system is an open-boundary system, although Dirichlet boundary conditions are applied. In contrast to cumbersome searching algorithms, this approach allows one to efficiently determine all QBS life times which are related to the imaginary parts of the complex eigenvalues of the Hamiltonian as $\tau_i = \hbar/2\mathcal{E}_i$.

With the described approach, the gate current density was evaluated for stacked SiO_2-Si_3N_4 and a single SiO_2 layer gate dielectric. The conduction band edge has been acquired from a self-consistent quantum-mechanical SCHRÖDINGER-POISSON solver as displayed in Fig. 4. The energy level, the value of the supply function, and the contribution of each QBS to the gate current density is listed in Fig. 5. In Fig. 6, the gate current density evaluated using the Tsu-Esaki formula is compared to an more accurate life time based approach. It can be seen that the current of stacked dielectric is considerably smaller. Furthermore, it is to point out that the Tsu-Esaki approach overestimates the gate current leakage under inversion. Thus, the life time based approach represents a method to accurately model direct tunneling through stacked gate dielectrics in inversion conditions. Furthermore, the PML formalism represents a more efficient scheme to calculate the lifetimes as compared to commonly applied algorithms.

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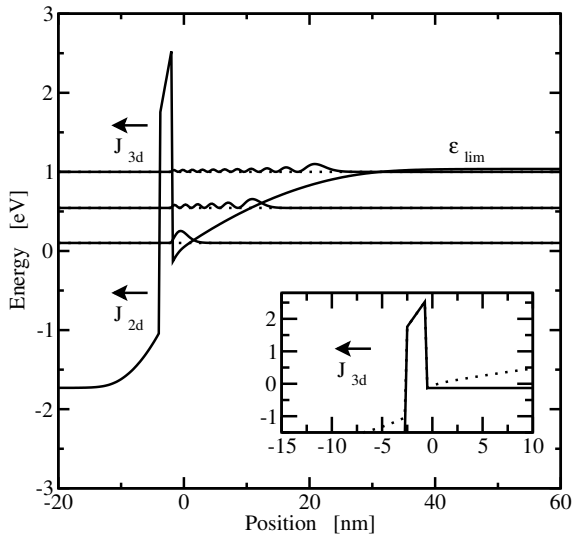

Figure 1: The potential well that arises at an nMOS inversion layer. For energies greater than $\mathcal{E}_{\rm lim}$, a continuum of states exists.

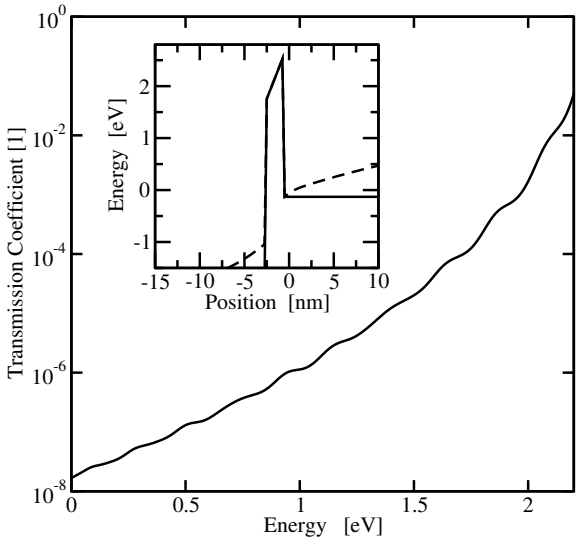

Figure 2: The transmission coefficient for the evaluation of the Tsu-Esaki formula. An energy barrier as displayed in the inset of the figure was assumed.

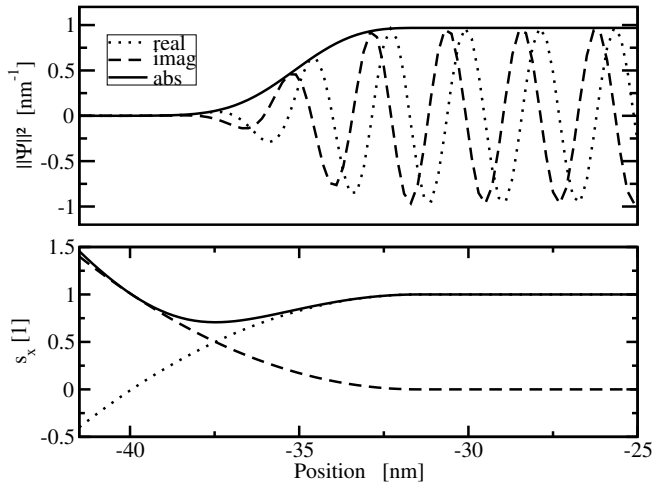

Figure 3: The wavefunction of the first QBS and the complex stretching function are displayed in the perfectly matched layer region as well as its transition to the physical region.

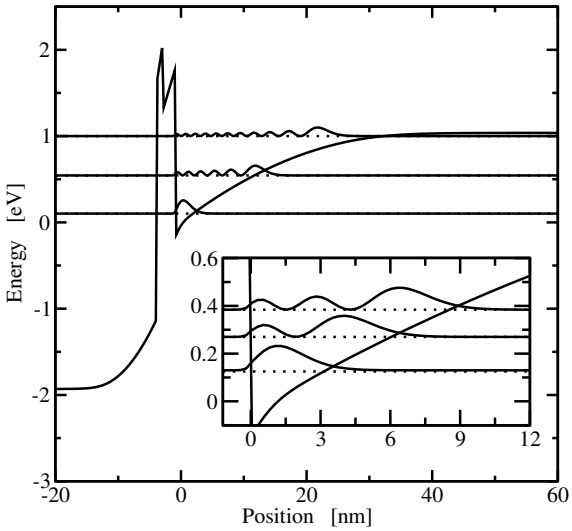

Figure 4: The figure shows the energy levels and the squared wavefunctions of some quasi-bound states as obtained by the PML method.

QBS	$\mathcal{E}_{\rm r}$ [eV]	N($E_{\rm r}$) [1]	$\tau_{\rm l}$ [ps]	$J_{\rm G}$ [A m^{-2}]
1	0.14	6.3×10^{-3}	210	1.7×10^{5}
2	0.27	2.5×10^{-5}	160	8.6×10^{2}
3	0.38	3.4×10^{-7}	140	1.4×10^{1}
10	0.86	3.1×10^{-15}	56	3.2×10^{-6}
15	1.01	5.0×10^{-18}	93	3.1×10^{-9}

Figure 5: The QBS of the MOS-capacitor for a gate bias of 1.5V, lifetimes, values of the supply function and their contribution to the gate current density.

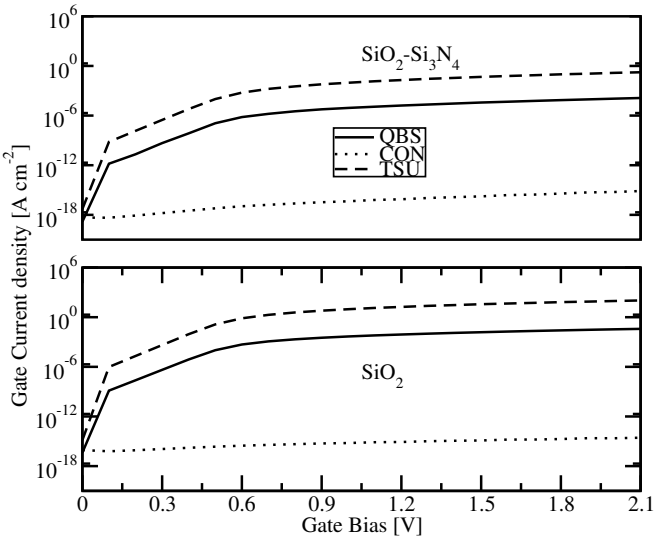

Figure 6: The gate current density for a single SiO_2 layer as well as a stacked SiO_2-Si_3N_4 dielectric calculated by using Tsu-Esaki formula and the life time based approach.