Demonstration of a Slipstream Simulation Flow Including Device and Circuit Simulators

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***Abstract**: A slipstream design flow from process via device to circuit simulation is proposed. Simulation results of the device simulator Minimos-NT and the circuit simulator Spectre are evaluated. A ring oscillator circuit is used as an example of the coherence between these simulators is demonstrated.*

1. INTRODUCTION

For more than 30 years, MOS device technologies have been improving at a dramatic rate. The scaling of the CMOS transistor has been the primary factor driving improvements in microprocessor performance. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. The ability to improve performance consistently while decreasing power consumption has made CMOS architecture the dominant technology for integrated circuits. In order to maintain this rapid rate of improvement, complex multilevel development methodologies, where ECAD and TCAD are the backbone, are required. A key modeling goal is to set up a consistent modeling infrastructure from process through device/circuit to systems design level. The slipstream simulation flow from device to circuit and system is an integral part of such an infrastructure.

It is important, both for industrial and academic purposes, to show the coherence between well-established simulation and design tools in the context of multi-level modeling paradigm. Generally, design engineers in the industry do not use device simulators. They rely on the models built in the particular CAD system they work with without having the option to adjust them. On the other hand, technology-development engineers and device physicists tune technology and device simulators to attain accurate results by calibrating the physical models. A ring oscillator circuit simulation is chosen as a particular example to demonstrate the coherence between the simulators Spectre (part of the Cadence CAD system) and Minimos-NT (part of the Viennese Integrated System for TCAD Applications).

2. MULTILEVEL MODELING

Depending on applications, there are various ways to categorize design and methodology flow, such as top-down versus bottom-up, analog versus digital, synthesis versus analysis, etc. The electrical characterization and analysis of analog and digital systems might be classified at the following levels.

System level relates to the analog or digital blocks within a particular system. From a simulation point of view, efficient methods to simulate these blocks at a higher level of abstraction are required, such as an analog behavioral modeling, very high-speed IC hardware description language (Verilog, VHDL), etc.

Circuit level refers to the circuit elements of a system and hence it involves complex systems of linear or nonlinear equations solved by matrix-solution techniques, such as nodal analysis, vector-sparse techniques. Besides the convergence problems occurring in any iterated solution procedure as well as storage allocation for large matrices, a key concern is the accuracy-speed tradeoff, which strongly depends on the device models and the circuit size.

Device level is referred to the analytical description of transistor terminal characteristics, normally expressed in compact closed-form equations, although iterated solutions, or even numerical solutions, sometimes are also considered to be at this level. It feeds Circuit level with the models of the electrical elements that build up the schematics.

Technology level is related to the detailed layer structures and doping profiles of the devices and their dependence on process variations as well as the resultant electrical characteristics. This is modeled by numerically solving process and transport differential equations on the cross section of a single transistor.

At the core of the development of new microelectronic products lay the complex, iterative loop of design–manufacturing–characterization–simulation−verification. Typically, a design process starts with the system specification, followed by the front-end and back-end designs. In this phase, by means of electronic computer-aided design (ECAD) tools the logic design can be synthesized from a high-level description language, the circuit netlist can be extracted from the logic functional description, and the layout can be extracted from the circuit-and logic-level descriptions. Once a set of masks has been designed, it is combined with a given process technique in the manufacturing phase. Electrical and technological characterization is then performed on the fabricated device to extract the parameters for back-annotation and verification. Wafer fabrication can be emulated by process simulation with technology CAD (TCAD) tools, from which realistic device structures and doping profiles can be generated, and transistor performance can be characterized through device simulation with reasonable accuracy. Interconnect delays can also be extracted through technology characterization with three-dimensional accuracy, which can provide information for design rule checker (DRC) and layout parasitic extraction (LPE) tools in the physical design. SPICE parameters can also be extracted from the *I-V* characteristics of the emulated device for back-annotating circuit simulators and timing analyzers, which might be regarded as calibration of ECAD tools based on TCAD tools.

The real challenge in the multi-level modeling infrastructure is to "propagate" the detailed physics captured at a lower-level (atomic/process) model to higher-level (circuit/block) abstraction. Therefore, an unified single-engine simulator environment is needed along with a consistent dual-representation at each level of abstraction, so that the higher-level model is extracted from its lower-level equivalent. The point is that it is not enough just to simulate different types of electronic circuits (transistor/gate/block levels) but to combine distinctively different algorithms in an unified simulator and applying to the same circuit described at different levels of abstraction. The separate (commercial) simulators are good for their respective areas, but information/consistency might be lost when simulators are combined. It is also difficult to move one design across different simulators.

3. CIRCUIT SIMULATORS

Today, SPICE — the most well known standard for circuits simulation — serve as a basis for the commercial circuit simulators. Among the most popular simulators are Spectre (Cadence Design Systems), Pspice (OrCad, Cadence Design Systems), Eldo (Mentor Graphics), HSPICE (Synopsis), Saber (Analogy), Tspice (Tanner Research), SmartSPICE (Silvaco), Smash (Dolphin Integration), APLAC (APLAC Solutions), etc. [1].

The most widely adopted models in the industry today are BSIM 3v3/4, MM 11, and EKV v3.0. The most popular model, BSIM3v3 [2], is an advanced submicron model that emphasizes physical formulation, computational efficiency, and ability to accommodate a variety of technologies. EKV v3.0 is oriented towards use in low-voltage, low-power analog and mixed design and simulation with very small number of parameters. Models such as BSIM3/4 and MM9/11 (Philips) are based on threshold voltage (V_{Th}) formulation. A disadvantage of this approach is the use of approximate expressions of I_{DS} in the weak- and strong-inversion regions, tied by a smoothing function. In result, the description of I_{DS} in the moderate inversion region is neither physical nor accurate (moderate inversion region becomes increasingly important in analog and RF design). To enlarge the physical content, model developments focus on charge sheet models based on surface potential ($\Box_s$) formulation (e.g. SP2001) [3]. These models allow an inherently single-equation and accurate calculation of I_{DS}, and could serve as a basis for the next sub-100-nm generation of compact models [4].

4. DEVICE SIMULATORS

The continuously increasing computational power of computer systems allows the use of TCAD tools on a very large scale. Several commercial device simulators (such as APSYS, ATLAS, BIPOLE3, DESSIS, G-PISCES, and MEDICI), company-developed simulators (like FIELDAY and NEMO), and university-developed simulators (such as DEVICE, FLOODS, GALENE, Minimos, nextnano3, PISCES, and PROSA) have been successfully employed for device engineering applications (for detailed review see [5]). These simulators differ considerably in dimensionality, in choice of carrier transport model (drift-diffusion, energy-transport, or Monte Carlo statistical solution of the Boltzmann transport equation), and in the capability of including electro-thermal effects. The drift-diffusion transport model is by now the most popular model used for device simulation. With down-scaling of the feature sizes, non-local effects become more pronounced and they must be accounted for by applying an energy-transport model. Quantum mechanical effects gain more importance with the scaling of the feature sizes.

The device simulator PISCES developed at Stanford University incorporates modeling capabilities for various devices and includes harmonic balance for large-signal simulation. MEDICI from Synopsys, which is based on PISCES, offers hydrodynamic simulation capabilities and rigorous modeling of carrier generation and recombination processes. DESSIS from ISE offers extensive trap modeling. The density-gradient method is used to model quantum effects.

At the quantum level a one-dimensional Schrödinger-Poisson solver, NEMO, based on non-equilibrium Green's functions is offered for sub-100 nm structures. The program SIMBA links one-dimensional Schrödinger solver with a two-dimensional Poisson solver. Quasi-two-dimensional approaches using a simplified one-dimensional current equation are demonstrated by several simulators (among others BIPOLE3 from BIPSIM). A similar approach which couples a full hydrodynamic transport model with a Schrödinger solver has been developed at the University of Leeds. A software interface between the device model and the compact Root large-signal model within the Microwave Design System has been offered by Agilent.

5. SIMULATION RESULTS

The slipstream workbench of simulation and design software includes process simulation [6] (TSUPREM4), device/circuit simulation (Minimos-NT) [7] and circuit simulation (Spectre) [8]. The two-dimensional device simulator is equipped with an extensive mixed-mode circuit capability including modeling of distributed devices [9]. This allows insight into the performance of devices under realistic dynamic boundary conditions imposed by a circuit. Spectre is an advanced circuit simulator that uses direct methods to simulate analog and digital circuits at the differential equation level. Its basic capabilities are similar in function and application to those of SPICE.

Here, we concentrate on electrical and device characterization proceeding from two particular simulators, namely Cadence Spectre circuit simulator and Minimos-NT device/circuit simulator. The Cadence Spectre simulator was used to demonstrate how industrial design software compares to TCAD simulation software, represented by Minimos-NT. Selected critical modeling issues are addressed in the device/circuit simulator Minimos-NT, which we used for the following examples.

5.1. Technology and Device Simulation

The process simulation starts from the blank wafer to the final device and reflects real device fabrication as accurately as possible. The implant profiles are calibrated to one-dimensional SIMS profiles. Process and device calibration is completed when the threshold voltage–gate length characteristic (V_{Th}–L_g) obtained by device simulation (Fig. 1) matches experimental data which indicates that the simulation includes advanced device behavior such as the reverse short channel effect [10].

The physical models in Minimos-NT are well calibrated [11], especially for silicon-based devices. There are only a few technology dependent model parameters that can be used for calibration purposes. One parameter is the gate workfunction difference which depends on the interface charges at the Si/SiO_2 interface and the properties of the polysilicon gate. Other parameters are used to model the surface mobilities, which are strongly dependent on the quality of the Si/SiO interface and on the electric field distribution in the channel.

5.2 Circuit Simulation

High-speed operation is a key challenge for lots of novel devices. As an example a ring oscillator circuit of five inverter chains with the output fed to the input, is used (Fig. 2). By determining the oscillation frequency f of such a ring circuit the average gate delay time t_d of one inverter stage can be calculated using $t_d = 1/(2nf)$ with n – number of stages (here $n = 5$). Minimos-NT can handle various sub-micron technologies. Simulation results for 0.25 µm and 0.13 µm technologies are presented in Fig. 3 and Fig. 4, respectively, which are in good agreement with experimental data [10]. Opposite to that, the Spectre model available in our Cadence Design software is calibrated for 0.35 µm technology and higher, and therefore, can be applied under this constraint. Simulation results for devices with two different gate-widths from the 0.35 µm technology are presented in Fig. 5 and Fig. 6, respectively.

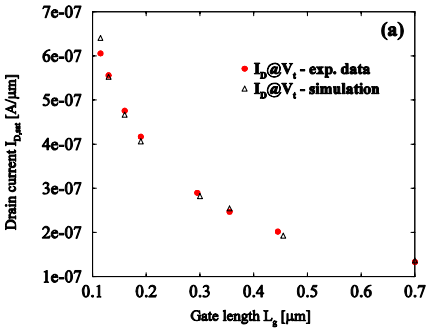

Fig. 1. Calibration of the drain current [A/µm] at threshold voltage.

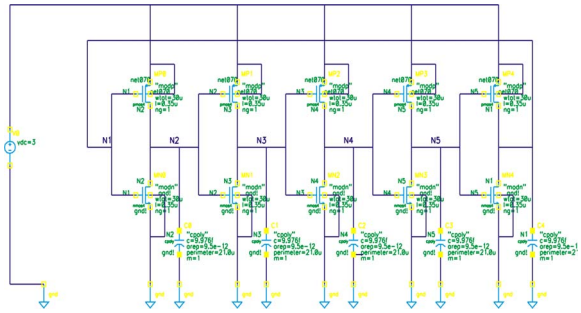

Fig. 2. Circuit diagram of a five stage ring oscillator.

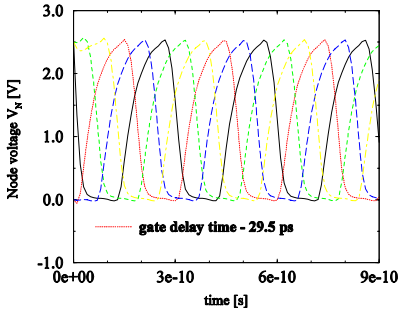

Fig. 3. Node voltages vs. time for nominal oscillator circuit from 0.25µm technology.

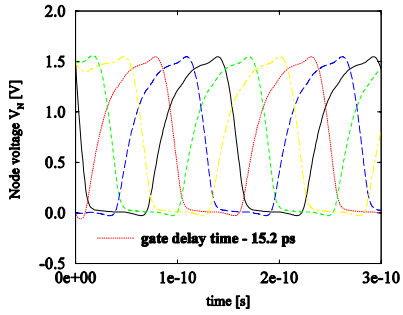

Fig. 4. Node voltages vs. time for nominal oscillator circuit from 0.13µm technology.

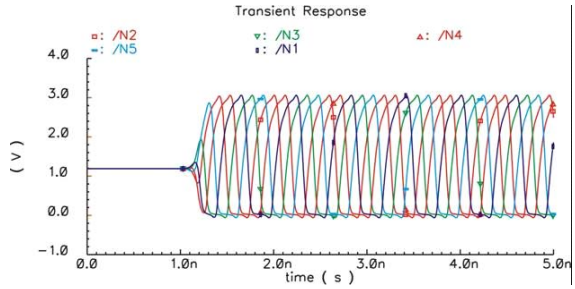

Fig. 5. Node voltages vs. time for oscillator circuit from 0.35µm technology (Wg=20µm).

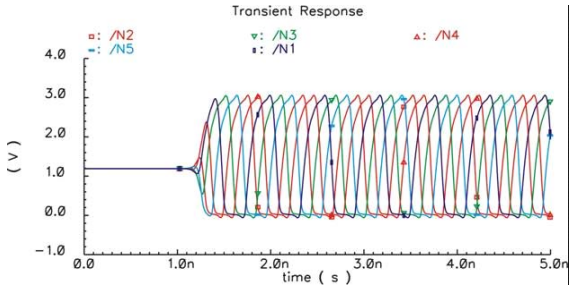

Fig. 6. Node voltages vs. time for oscillator circuit from 0.35µm technology (Wg=10µm).

5.3 Evaluation of the Results

The gate length L_g, gate width W_g, and applied voltage V_{DD} for the investigated technologies are summarized in Table I, together with simulation results for the ring circuit average gate delay time obtained with both simulators.

Since our Spectre model is calibrated for 0.35 µm technology and higher, we were able to explicitly compare these results only. As can be seen from Table I, comparable average gate delays per stage t_d are obtained from device/circuit simulation with Minimost-NT (58.8ps) and from Spectre circuit simulator (57.3ps). Fig. 7 shows the simulated node voltages V_N (N=1…5) vs. time resulting from the two simulators. The established setup allows combination of ECAD and TCAD simulation tools in continuous flow, which provides a link from technology development through device development to circuit design.

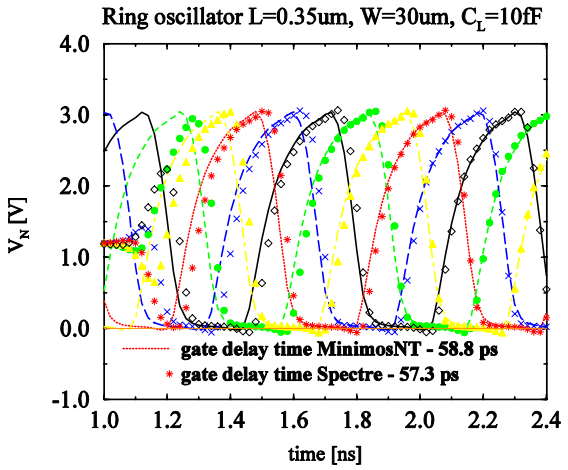

Fig. 7. Comparison of node voltages simulated with Spectre and Minimos-NT.

Simulator	No.	L_g [um]	W_g [um]	V_{DD} [V]	C_L [fF]	□ [ps]	$f = 1/$□ [GHz]	t_d [ps]
Minimos-NT	1	0.35	30	3.0	10	588	1.70	**58.8**
	2	0.25	20	2.5	5.4	295	3.39	29.5
	3	0.13	10	1.5	3.8	152	6.58	15.2
Spectre	1	0.6	30	3.0	10	1140	0.88	114.0
	2	0.6	20	3.0	10	1163	0.86	116.3
	3	0.6	10	3.0	10	1339	0.75	133.9
	4	0.35	30	3.0	10	573	1.74	**57.3**
	5	0.35	20	3.0	10	590	1.69	59.0
	6	0.35	10	3.0	10	640	1.56	64.0

Tab. 1. Minimos-NT and Spectre simulation results.

6. CONCLUSION

A concise outline of the multilevel modeling concept as well as the state-of-the-art compact models and simulation tools for MOS devices was given. A slipstream simulation workflow (Fig. 8) was demonstrated on a circuit example proving the coherence between circuit simulators (Cadence Spectre) and device simulators (TU-Vienna Minimos-NT). The established simulation setup can be beneficial for both scientific and educational purposes.

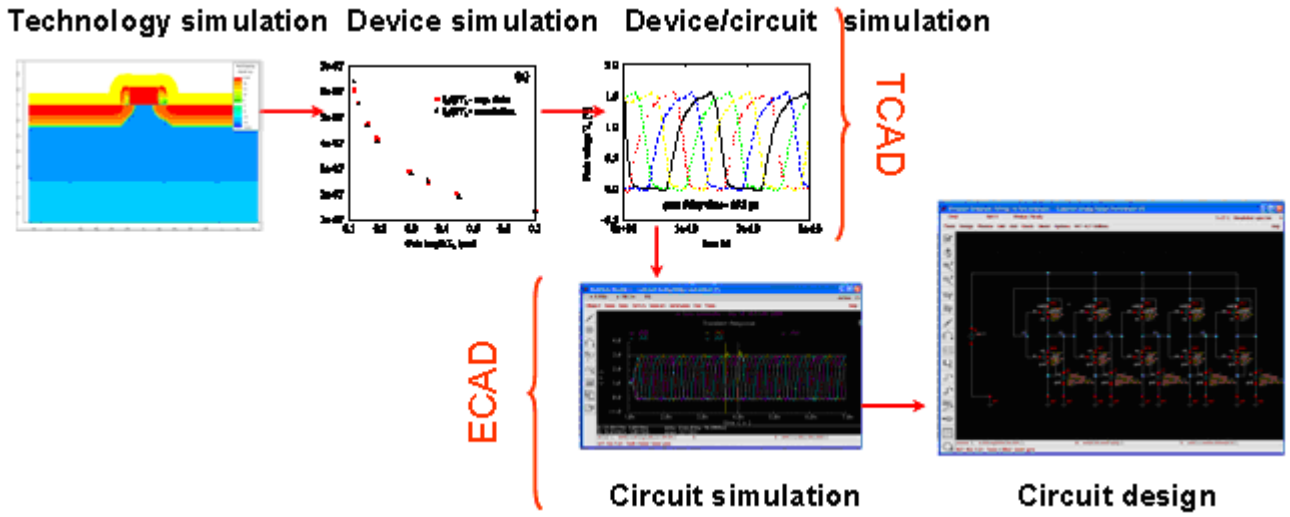

Fig. 8. Slipstream simulation flow including TCAD and ECAD tools.

ACKNOWLEDGMENT

The authors acknowledge partial support from the Osterreichische Forschungsgemeinschaft (OeFG), Project MOELPlus 044, and from the Austrian Science Funds (FWF), START-Project Y247-N13.

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