Improving DC and AC Characteristics of Ohmic Contact Carbon Nanotube Field Effect Transistors

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Abstract:

A study of ohmic contact carbon nanotube field effect transistors is presented. The effect of the gate-drain spacer on the DC and AC response of the device was studied. Simulation results suggest that by appropriately selecting the gate-drain spacer both the DC and AC characteristics of the device are improved.

1. Introduction

Exceptional electronic and mechanical properties together with nanoscale diameter make carbon nanotubes (CNTs) candidates for nanoscale field effect transistors (FETs). High performance CNTFETs were achieved recently [1–5]. In short devices (less than 100 nm) carrier transport through the device is nearly ballistic [3, 6]. We solved the coupled Poisson and Schrödinger equation system to study the DC response of CNTFETs. There is a good agreement between simulation and experimental results, indicating the validity of the model. The Quasi Static Approximation (QSA) was used to investigate the AC response of these devices.

The contact between metal and CNT can be of Ohmic [6] or Schottky type [7]. In this work we focus on Ohmic contact CNTFETs which theoretically [8] and experimentally [3] show better performance than Schottky contact devices. In a p-type device with ohmic contacts holes see no barrier while the barrier height for electrons is $\mathcal{E}_{\mathrm{g}}$. By changing the gate voltage the transmission coefficient of holes through the device is modulated and as a result the total current changes [6]. However, unwanted ambipolar behavior is observed, which limits the DC characteristics of the device by reducing the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio. This behavior is more apparent in Schottky contact devices, where both electrons and holes see a barrier height of $\mathrm{E_g}/2$ [9]. In our previous work [10] we showed that a double gate structure can be used to suppress the ambipolar behavior of Schottky contact devices. In a double gate device the carrier injection at the source and drain contacts are controlled separately. In ohmic contact devices, however, because of asymmetric barrier heights the ambipolar behavior can be reduced without the need of the second gate. We prove that by appropriately selecting the gate-drain spacer not only the ambipolar behavior and DC characteristics, but also the AC characteristics of the device are improved.

2. Approach

In this section the models which were used to study the DC and AC response of CNTFETs are explained. As will be shown at the end of this section we achieve a good agreement between simulation and experimental results.

2.1 DC Response

In order to account properly for ballistic transport we have solved the coupled Poisson and Schrödinger equations.

$$\frac{\partial^2 V}{\partial \rho^2} + \frac{1}{\rho}\frac{\partial V}{\partial \rho} + \frac{\partial^2 V}{\partial z^2} = -\frac{Q}{\epsilon} \qquad (1)$$

$$-\frac{\hbar^2}{2\mathrm{m}^*}\frac{\partial^2 \Psi^{n,p}_{s,d}}{\partial z^2} + (U^{n,p} - E)\Psi^{n,p}_{s,d} = 0 \qquad (2)$$

We have considered a cylindrical symmetric structure, in which the gate surrounds the CNT, such that the Poisson equation (1) is restricted to two-dimensions. In (2) superscripts denote the type of the carriers. Subscripts denote the contacts, where s stands for the source contact and d for the drain contact. For example, $\Psi^{\mathrm{n}}_{\mathrm{s}}$ is the wave function associated with electrons that have been injected from the source contact. The Schrödinger equation is solved on the surface of the tube, and is restricted to one-dimension because of cylindrical symmetry. All our calculations assume a CNT with 0.5 eV band gap, corresponding to a diameter of 1.7 nm [3].

The space charge density in (1) is calculated as:

$$Q = \frac{\mathrm{q}(p - n)\delta(\rho - \rho_{cnt})}{2\pi\rho} \qquad (3)$$

where n and p are the total electron and hole concentrations per unit length. In (3) δ/ρ is the Dirac delta function in cylindrical coordinates, indicating that carriers were taken into account by means of a sheet charge distributed uniformly over the surface of the CNT [11]. Including the source and drain injection components, the total electron concentration in the CNT is calculated as:

$$n = \frac{4}{2\pi}\int f_s|\Psi^n_s|^2 dk_s + \frac{4}{2\pi}\int f_d|\Psi^n_d|^2 dk_d \qquad (4)$$

where $f_{s,d}$ are equilibrium Fermi functions at the source and drain contacts, respectively. The total hole concentration in the CNT is calculated analogously.

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The Landauer-Büttiker formula is used for calculating the current:

$$I^{n,p} = \frac{4\mathrm{q}}{\mathrm{h}} \int [f_s^{n,p}(E) - f_d^{n,p}(E)]\, TC^{n,p}(E)\, dE \qquad (5)$$

where $TC^{n,p}(E)$ are the transmission coefficients of electrons and holes through the device. The factor 4 in (4) and (5) stems from the twofold band and twofold spin degeneracy.

2.2 Dynamic Response

To study the dynamic behavior of CNTFETs, the QSA was used. Generally in this method device capacitances are given by the derivatives of the various charges with respect to the terminal voltages,

$$C_{ij} = \chi_{ij} \frac{\partial Q_i}{\partial V_j}\bigg|_{V_{k\neq j}=0} \qquad (6)$$

where the indices i, j, k represent terminals (gate, source or drain), and $\chi_{ij} = -1$ for $i \neq j$ and $\chi_{ij} = +1$ for $i = j$. The differentiation of these expressions is performed numerically over steady state charges [12]. This method is widely used for the analysis of conventional semiconductor devices, where the charge is partitioned into two parts indicating the contribution of the source and drain contacts [12, 13]. For example, the gate-source capacitance is calculated by

$$C_{sg} = \frac{\partial Q_{se}}{\partial V_{gs}} + \frac{\partial Q_{st}}{\partial V_{gs}} = C_{se} + C_{sq} \qquad (7)$$

where Q_{se} is total charge charge on the source contact and Q_{st} is the total charge on the tube injected from the source contact. As shown in (7) the total gate-source capacitance is split into two components, the first term indicates the electrostatic gate-source capacitance and the second term is usually referred to as quantum capacitance [14]. The capacitance matrix has a rank of 3, and due to quantum capacitances the matrix elements are not reciprocal ($C_{ij} \neq C_{ji}$). In this work we assumed that only the gate voltage changes, whereas the voltages of the other terminals are kept constant. Therfore, the capacitance matrix simplifies to three components, and an equivalent circuit as shown in Fig. 1 is achieved [15]. In Fig. 1, g_m is the differential transconductance calculated by $g_m = \partial I_{ds}/\partial V_{gs}$. Based on the equivalent circuit in Fig. 1, the cutoff frequency of the device can be derived as

$$f_T = \frac{g_m}{2\pi C_{\mathrm{sg}}\sqrt{1 + 2\frac{C_{\mathrm{dg}}}{C_{\mathrm{sg}}}}} \qquad (8)$$

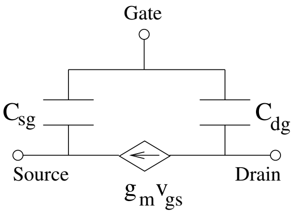

Figure 1: Simplified equivalent circuit model for the dynamic response of CNTFETs.

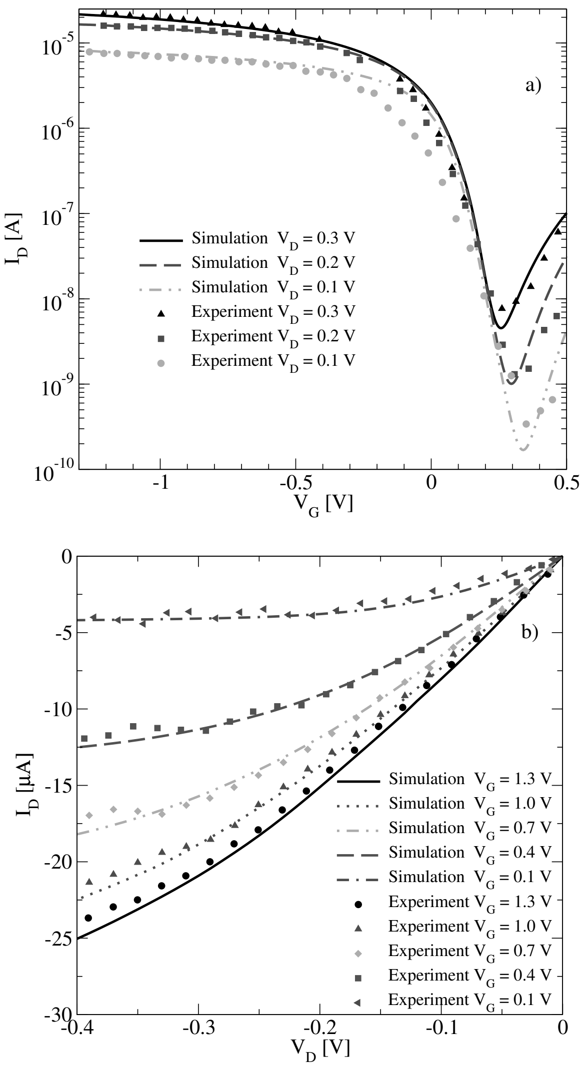

Figure 2: Comparison of the experimental and simulation results a) Transfer characteristics, b) Output characteristics.

2.3 Comparison with Experimental Data

For a fair comparison with experimental results, we used the same material and geometrical parameters as reported in [3]. As shown in Fig. 2, there is a good agreement between simulation and experimental results despite the fact that the cylindrical structure is only an approximation of the real device structure.

3. The Effect of the on the Device Characteristics

First the operation of CNTFETs and the ambipolar behavior is explained. Then the effect of the gate-drain spacer, $\mathrm{L_{GD}}$, (see Fig. 3) on the ambipolar behavior, DC, and AC response of CNTFETs is studied.

We consider a p-type ohmic device, similar to that reported in [3]. As shown in Fig. 2-a, the current has a minimum. This due to the well known ambipolar behavior of these devices, which can be well understood by considering the band edge profiles of the device. As shown in Fig. 4, if the drain voltage becomes higher than the gate voltage, the barrier thickness for electrons at the drain contact is reduced and the tunneling current of electron increases. At the minimum point electrons and holes have the same contribution to the total current and in other regions either electrons or holes contribute mostly to the total current. As shown in Fig. 4, by increasing $\mathrm{L_{GD}}$ the band edge profile near the drain contact is less affected by the gate voltage. Therfore, when the voltage between the gate and drain contacts increases the barrier thickness for electrons near the drain contact is less reduced, and as a result the tunneling current of electrons is suppressed. In Fig. 5 the the effect of increasing this spacer on transfer characteristics of the device is shown. By increasing $\mathrm{L_{GD}}$ the off current decreases, while the on current remains unchanged. The Inset of Fig. 5 shows that the differential transconductance remains also unchanged.

This method can not be applied to conventional MOSFETs. MOSFETs are charge controlled devices, by changing the gate voltage the channel conductivity is modulated. In contrast the channel of CNTFETs exhibits a constant conductivity ($\mathrm{G} = 2\mathrm{q}^2/\mathrm{h}$ per mode) and the gate voltage modulates the transmission coefficient of carriers through the device. The band edge profile near the source contact plays an important role in determining the total current, since at high drain voltages all the carriers which cross the barrier near the source contact will be absorbed by the drain contact (neglecting minor quantum mechanical reflections).

Fig. 6 shows the effect of increasing of $\mathrm{L_{GD}}$ on the mutual capacitances between terminals. As seen in both cases the electrostatic capacitances dominate the quantum capacitances. By increasing the $\mathrm{L_{GD}}$ the electrostatic capacitance of the gate-drain contact is reduced. In general, for a better frequency response the differential transconductance of a device should be increased and the parasitic capacitances should be decreased, see (8). We showed that by increasing $\mathrm{L_{GD}}$, the differential transconductance of the device is not affected, while the gate drain parasitic capacitance is decreased. Based on (8) for the device with $\mathrm{L_{GD}} = 5\mathrm{nm}$ the cutoff frequency is $f_T \approx$ 160 GHz, but for the device with $\mathrm{L_{GD}} = 25\mathrm{nm}$ the cutoff frequency is $f_T \approx$ 210 GHz. The comparison of output characteristics and cutoff frequencies indicates that by increasing $\mathrm{L_{GD}}$ both the DC and AC response of the device are improved.

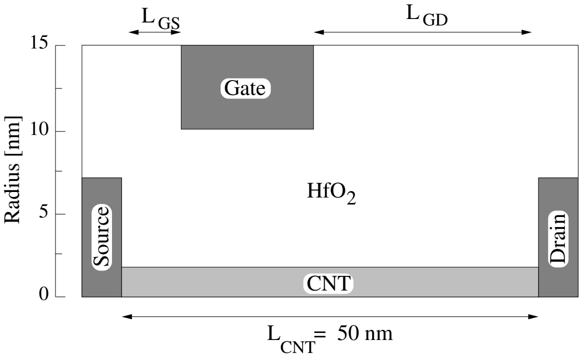

Figure 3: Sketch of the cylindrical device.

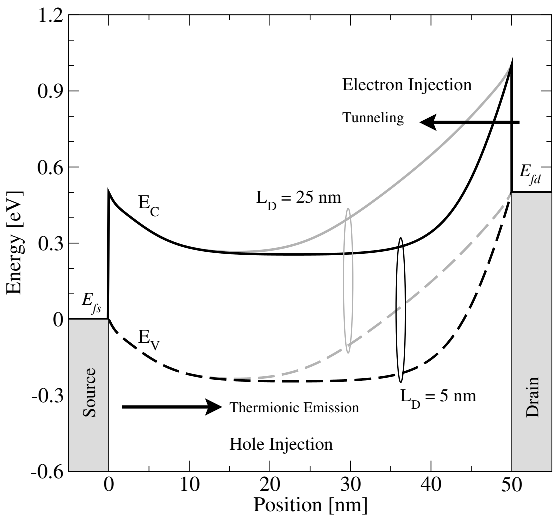

Figure 4: The effect of $\mathrm{L_{GD}}$ on the band-edge profiles of the device. $\mathrm{V_G} = 0.2\mathrm{V}$ and $\mathrm{V_D} = -0.5\mathrm{V}$.

4. Conclusion

By appropriately selecting the gate-drain spacer both the DC and AC response of ohmic contact CNTFETs are improved. By increasing the gate-drain spacer the ambipolar behavior is suppressed and the parasitic capacitance between the gate and drain contacts is reduced. By suppressing the ambipolar behavior the $I_{\mathrm{on}}/I_{\mathrm{off}}$ increases by three-orders of magnitude, and by reducing the parasitic capacitances the cutoff frequency increases about 30%.

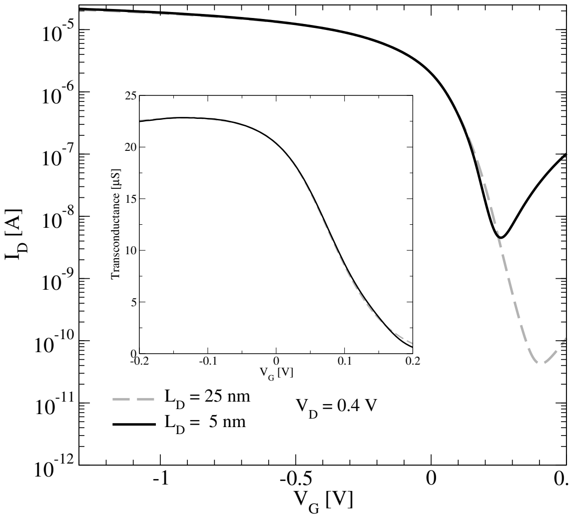

Figure 5: The effect of $\mathrm{L_{GD}}$ on the transfer characteristics. The inset shows the differential transconductance.

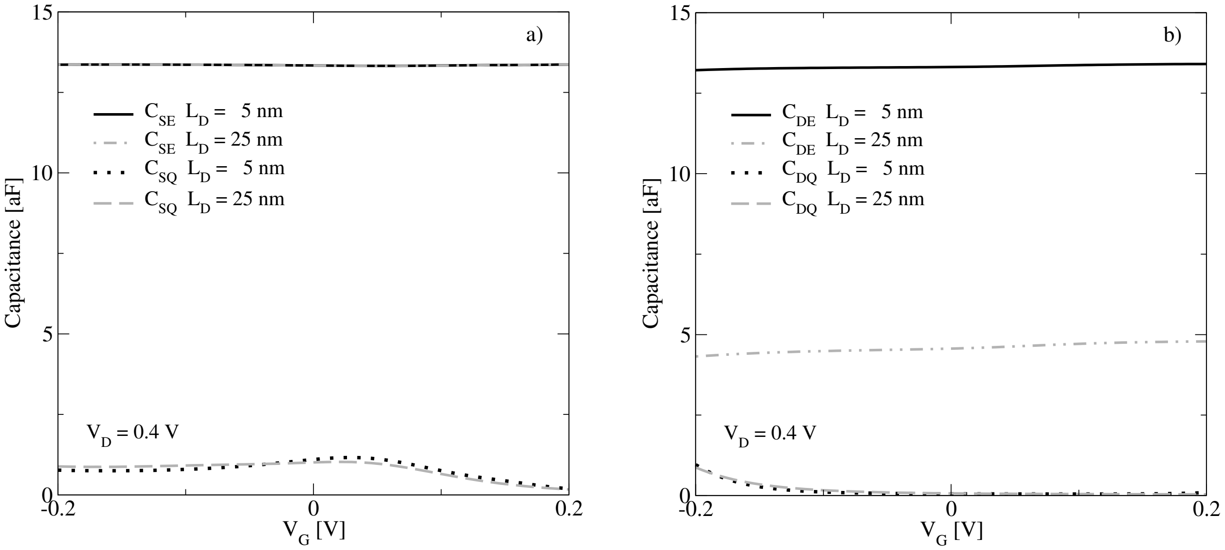

Figure 6: The effect of L_{GD} on the electrostatic and quantum capacitances associated with the a) Source contact, and b) Drain contact.

5. Acknowledgments

This work was partly supported by the European Commission, contract No. 506844 (NoE SINANO), and the National Program for Tera-level Nano-devices of the Korea Ministry of Science and Technology as one of the 21st Century Frontier Programs. Discussions with Prof. David Pulfrey are acknowledged.

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