Material Parameter Identification for Interconnect Analysis

Stefan Holzer and Siegfried Selberherr[1]

Christian Doppler Laboratory for TCAD in Microelectronics at the Institute for Microelectronics, TU Wien

[1] *Institute for Microelectronics, TU Wien, Gußhausstraße 27–29, 1040 Wien, Austria*

E-mail: {Holzer| Selberherr}@iue.tuwien.ac.at

ABSTRACT: State-of-the-art semiconductor process technology nodes in the submicron regime require devices and interconnect structures to operate at dramatically shrinked geometries utilizing new materials. Some structures composed of arrangements of several materials cannot be rigorously described because of limited knowledge of fundamental material parameters and material interactions. For practical applications, however, a parameterized description of certain properties is often sufficient. In order to obtain the required electrical and thermal properties of complex interconnect structures we introduce optimization approaches to compute values for the missing parameters within certain physical constraints.

As an example we present a complex fusing structure made of several materials where some electrical and thermal parameters were not accurately known. For this purpose a sophisticated optimization and simulation framework has been utilized which provides an open interface for arbitrary tool flows.

INTRODUCTION

Continuous enhancements of integrated circuits design require high quality and predictive simulations. Therefore, new methods and models have to be developed which allow to describe the observed phenomena. When some device structures reach a certain level of complexity, the behavior of the included materials and their interactions cannot be rigorously described by simple and basic equations because of limited knowledge of fundamental material parameters. Therefore, parameterized models are required which can sufficiently describe the observed behavior with reasonable computational effort in the desired range of interest. With the help of sophisticated simulation and optimization tools new models can be developed and adjusted by parameter identification methods to the appropriate needs.

To illustrate this procedure we consider as an example a complex fusing structure consisting of several polycrystalline materials. Therefore, we present in the next section the principle of the identification of parameters. Afterwards the mathematical models and equations are sketched, where we introduce the adoptions to the simulator to obtain the temperature-dependent equation systems. In addition, our fusing structure is presented with measurements and the simulation results.

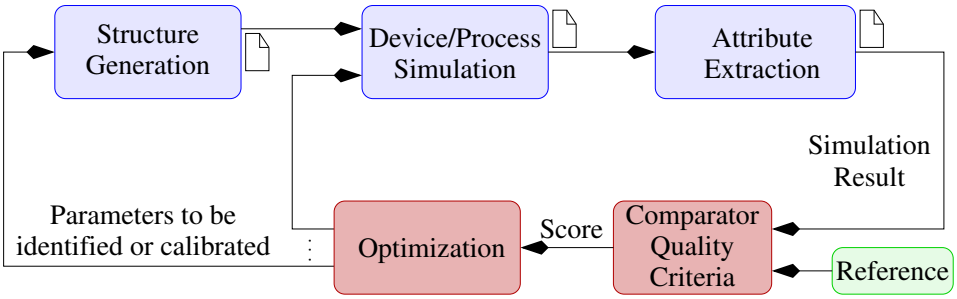

Fig 1: Data flow for the parameter identification of SIESTA.

PARAMETER IDENTIFICATION TOOL

State-of-the-art simulation and optimization frameworks [1, 2, 3, 4] offer a wide range of optimization strategies and interfaces to various simulation tools. The *Simulation Environment for Semiconductor Technology Analysis* (SIESTA) [5] provides numerous optimizers and interfaces to simulators which can be appropriately chosen for a particular problem. An overview of the data flow in SIESTA for parameter extraction is shown in Fig. 1. The core part for parameter extraction is the optimizer and a tool which compares the simulation result with a reference under certain user-defined constraints in order to calculate a score value for the quality of the currently available simulation result. With the calculated score value the optimizer tries to improve the simulation result by varying the unknown parameters with certain strategies in order to optimize the score value and thereby the quality. The other parts of the data processing blocks which are located in the upper half of Fig. 1 are related to the evaluation of the models and their parameters required to obtain the corresponding simulation result. The blocks symbolically depict important parts of typical simulation steps: structure generation which means geometry composition and mesh generation to generate the interconnect device structure, the actual underlying device and process simulation, and the necessary post processing steps to extract attributes which can be compared to measurements or to other reference data. For the example device the shown steps have to be particularly adopted. The following section presents the corresponding mathematical models and equations, which we properly selected.

MATHEMATICAL MODELS

For the simulation of the transient temperature evolution the three-dimensional interconnect simulator STAP [6] has been used. STAP calculates the Joule's self-heating effect by solving Euler's equation (1) and the heat conduction equation (2) which is coupled with the power loss equation.

$$\nabla \cdot (\sigma \nabla \varphi) = 0 \tag{1}$$

$$c_\mathrm{p}\, \rho_\mathrm{m} \frac{\partial T}{\partial t} - \nabla \cdot (\lambda \nabla T) = \sigma (\nabla \varphi)^2 \tag{2}$$

φ denotes the electrical scalar potential, p the power density, and σ and λ the electrical and the thermal conductivities. c_p represents the specific heat capacitance, ρ_m the mass density, and T the temperature. For our investigation we have assumed that the material parameters of the thermal and the electrical conductivity are temperature-dependent and follow the polynomial models

$$\sigma(T) = \frac{\sigma_0}{1 + \alpha_\sigma(T - T_0) + \beta_\sigma(T - T_0)^2} \tag{3}$$

$$\lambda(T) = \frac{\lambda_0}{1 + \alpha_\lambda(T - T_0)}, \tag{4}$$

where σ_0 and λ_0 are the conductivities at a certain reference temperature T_0 and α_σ, β_σ, and α_λ are the corresponding first and second order temperature coefficients.

FUSING STRUCTURE

For processing technologies with 0.35 micron feature size and below fuses made of polycrystalline interconnect materials are an interesting option for programmable memory cells. In technology nodes with larger feature size fusing can cause damage to the passivation layers and iy is thus rated as critical. Arrangements of fuses are used as one-time programmable memory blocks in a range of several kilo bits. Thus, they provide a cheap and efficient alternative to standard non-volatile programmable memory cells, because the additional process costs are very low [7]. Moreover, approaches have been reported to increase the memory density by using multi-layered tri-state fuses [8]. Another important application is to use these fuses as field programmable gate arrays for trimming circuits to obtain a certain analog or digital performance [9]. In addition to these applications, fuses can be used as elements for trimable resistors and capacitor arrays [10]. Furthermore, the fuses can also act as classic protective elements for critical circuit components [11].

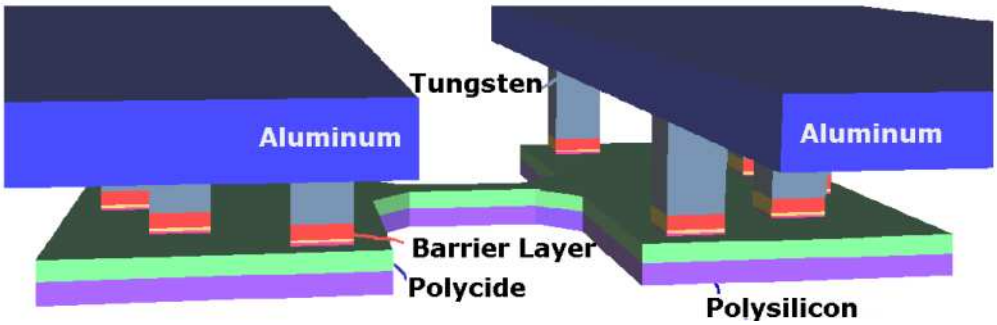

Fig 2: Sketch of a fusing device showing the variety of materials included.

The structure of a typical interconnect fusing device is shown in Fig. 2, where the complex material composition can be seen. The dual-layered rod in the region between the two aluminum pads is the melting region of the fuse. The fuse is programmed by sending a

current pulse through the fuse at an appropriate bias. This results in an opening of the polycrystalline silicon film due to thermal second-breakdown. The transition takes place when parts of the polycrystalline silicon layer reach the melting point. The molten silicon is transported from the negative biased side to the positive side through the drift of ions [12]. In terms of power and area consumption, fuses made of available interconnect materials are more attractive compared to hybrid technologies [13] with other materials. However, scaling down to smaller feature sizes requires also a decreased supply voltages [14]. This constraint demands a careful design and a rigorous optimization of the fusing structure to ensure the reliability of the programming mechanism [15] and to minimize the power consumption during the fusing process.

Since the fusing mechanism takes place within a couple of 10 ns for a voltage step and several micro seconds for a voltage ramp, direct measurements are hard to obtain [7]. Previous work [16] already brought some new insights into the physics of the fusing mechanism. In addition, an optimization of the fusing structure is required for a fast fusing process and to ensure the reliability. Obtaining these required measurements was only possible through costly experiments using test chips.

We focus on achieving a better insight into the electrical and thermal characteristics of the materials used in the interconnect fusing structure shown in Fig. 2. In particular, we are interested in the temperature dependence of the thermal and the electrical conductivity of the key materials polysilicon and the polycide (WSi_x). Better knowledge of these parameters allows to perform a layout optimization for higher reliability of the fusing procedure and a faster fusing operation. With the parameter identification procedure shown in Fig. 1 and the given mathematical models we are able to identify values for certain models within user-defined constraints. In order to obtain reasonable results from the simulation we need accurate information on the test circuit of the fusing device [17].

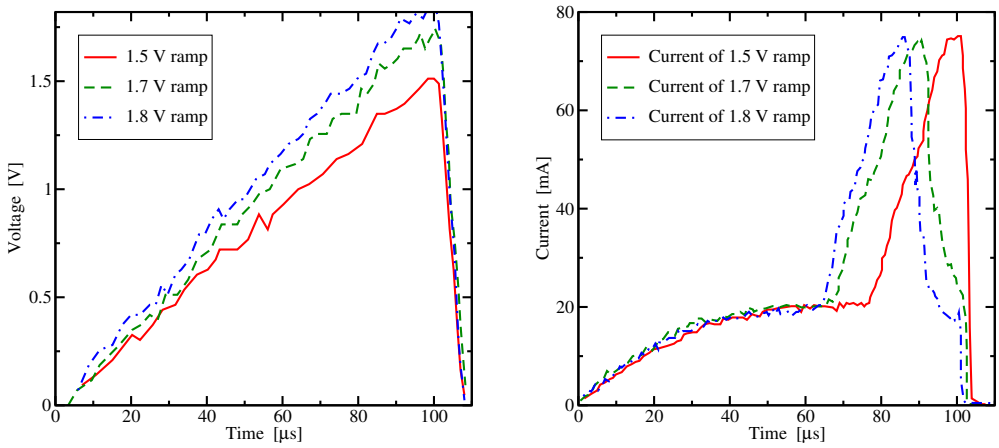

Fig 3: The different voltage ramps and the corresponding fusing currents.

Since the measurements of the fusing mechanism have to be carried out within a couple of 10 ns for several μs we prolongated the fusing time by applying a voltage ramp with a rising slope period of 100 μs, which allows to measure the fusing current with reasonable accuracy (cf. Fig. 3).

These measurement results serve as reference data for the parameter identification procedure. Fig. 3 shows a highly non linear behaviour of the fuse current during the heat-up period of the fuse. After a certain time the current jumps to a value which is only constrained by the parasitics of the fuse and the test circuit. Therefore, this point will confine our currently available capability for the simulation and prediction with the introduced models (3) and (4).

For the parameter identification, initial values for the thermal and electrical conductivity of polysilicon and polycide obtained from literature [18, 19] were used. A gradient-based optimization strategy served well to improve the initial values in order to obtain good agreement with the reference data obtained from the measurements.

RESULTS AND DISCUSSION

We had to include several consistency checks to ensure that also the intermediate simulation data are physically reasonable. After the completion of the optimization task we obtained an excellent agreement with the measurements as shown in Fig. 4.

Table 1: Comparison of extracted parameters with data obtained from literature.

Quantities		Poly Si	Poly Si_{Lit}	Polycide	$\text{Polycide}_{\text{Lit}}$
σ_0	$[1/\mu\Omega\text{m}]$	0.12	-	1.25	$0.1 - 18.8$
α_σ	$[1/\text{K}]$	9.1×10^{-4}	10^{-3}	8.9×10^{-4}	$5 - 10 \times 10^{-3}$
β_σ	$[1/\text{K}^2]$	7.9×10^{-7}	-	8.1×10^{-7}	3.5×10^{-7}
λ_0	$[\text{W/Km}]$	45.4	40	119.4	$100 - 179$
α_λ	$[1/\text{K}]$	2×10^{-2}	10^{-2}	2.98×10^{-2}	-

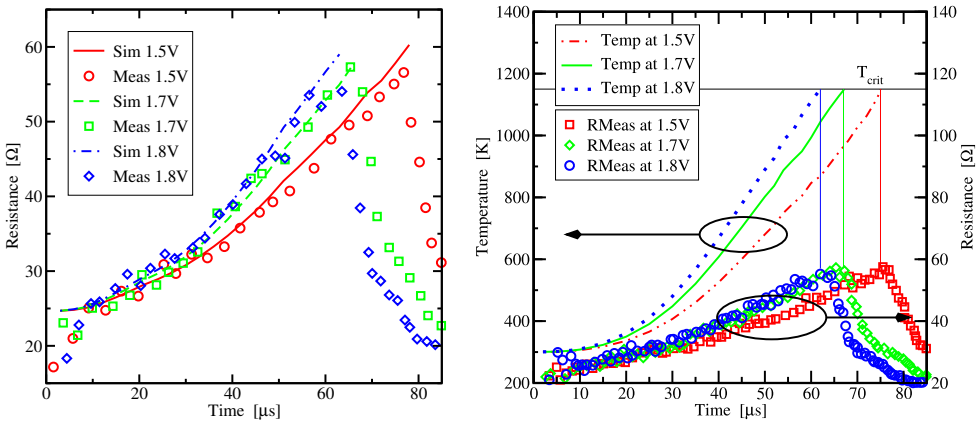

Fig 4: Comparison of the simulation results with the measurements.

In Tab. 1 the corresponding extracted coefficients are compared to data found in the literature [19, 18, 20].

Another interesting outcome of our investigation was that the temperature, at which the resistance drops, is the same for all three different applied voltage ramps. Therefore, we can assume that this particular temperature corresponds to a material-specific phenomenon which is related to the thermal run-away and the starting melting process. As expected the area with the highest local temperature is located at the surface of the fusing area in between the two interconnect pads as shown in Fig. 5.

The extracted parameters can be used for investigation of local temperature distributions and self-heating effects in other interconnect structures using similar materials.

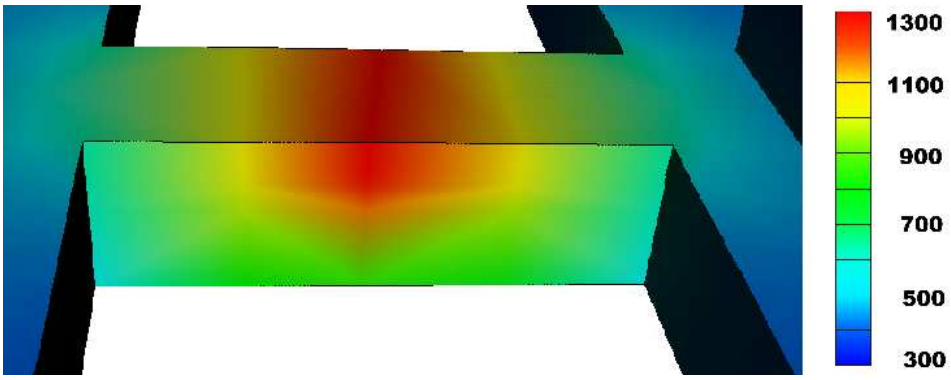

Fig 5: The temperature distribution [K] at the hottest spot in the fusing area.

CONCLUSIONS

We have presented a technique to obtain important electrical and thermal material parameters only from electrical measurements of a complex interconnect structure by the use of parameter extraction. These thereby identified parameters have been used to describe the operation of fusing structures until the melting process starts.

REFERENCES

[1] R. Plasun, M. Stockinger, R. Strasser, and S. Selberherr, "Simulation Based Optimization Environment and Its Application to Semiconductor Devices," in *Intl. Conf. on Applied Modelling and Simulation*, Honolulu, USA, Aug. 1998, pp. 313–316.

[2] Synopsys, *Taurus Work Bench User Manual*, Synopsys, 2003.

[3] ISE Integrated Systems Engineering, *ISE TCAD Manuals*, Integrated Systems Engineering, 2003.

[4] S. Holzer *et al.*, "Optimization and Inverse Modeling for TCAD Applications," in *SNDT 2004, Symposium on Nano Devices Technology 2004*, Hsinchu, Taiwan, May 2004, pp. 113–116.

[5] Institute for Microelectronics, *SIESTA – The Simulation Environment for Semiconductor Technology Analysis, Version 1.1std*, Technische Universität Wien, Austria, 2003.

[6] R. Sabelka and S. Selberherr, "A Finite Element Simulator for Three-Dimensional Analysis of Interconnect Structures," *Microelectronics Journal*, vol. 32, pp. 163–171, 2001.

[7] R. Minixhofer *et al.*, "Optimization of Electrothermal Material Parameters Using Inverse Modeling," in *Proc. 33rd European Solid-State Device Research Conference (ESSDERC 2003)*, J. Franca and P. Freitas, Eds., Estoril, Portugal, Sept. 2003, pp. 363–366, IEEE.

[8] A. Doyle, "A Thick Polysilicon Three-State Fuse," *Motorola Technical Developements 3*, pp. 31–32, 1993.

[9] O. Kim, "CMOS Trimming Circuit Based on Polysilicon Fusing," *Electr.Lett.*, vol. 34, no. 4, pp. 355–356, 1998.

[10] D. J. Nickel, "Element Trimmable Fusible Link," *IBM Technical Disclosure Bulletin*, vol. 26, no. 8, pp. 4415, 1984.

[11] J. R. Lloyd and M. R. Polcari, "Polysilicon Fuse," *IBM Technical Disclosure Bulletin*, vol. 24, no. 7A, pp. 3442, 1981.

[12] D. W. Greve, "Programming Mechanism of Polysilicon Resistor Fuses," *IEEE Trans.Electron Devices*, vol. 29, no. 4, pp. 719–724, 1982.

[13] Y. Fukada, S. Kohda, K. Masuda, and Y. Kitano, "A New Fusible-Type Programmable Element Composed of Aluminum and Polysilicon," *IEEE Trans.Electron Devices*, vol. 33, no. 2, pp. 250–253, 1986.

[14] A. Kalnitsky, I. Saadat, A. Bergemont, and P. Francis, "$CoSi_2$ Integrated Fuses on Poly Silicon for Low Voltage 0.18 μm CMOS Applications," in *Proc.IEDM Tech.Dig*, 1999, pp. 765–768.

[15] D. W. Greve, "Programming Mechanism of Polysilicon Fuse Links," *IEEE Trans.Electron Devices*, vol. 17, no. 2, pp. 349–354, 1982.

[16] S. Das and S. Lahiri, "Transient Response of Polysilicon Fuse-Links for Programmable Memories and Circuits," in *SPIE's Semiconductor Devices*, May 1996, vol. 2733, pp. 232–234.

[17] S. Holzer *et al.*, "Extraction of Material Parameters Based on Inverse Modeling of Three-Dimensional Interconnect Fusing Structures," *Microelectronics Journal*, vol. 35, no. 10, pp. 805–810, 2004.

[18] C. Vahlas, P.-Y. Chevalier, and E. Blanquet, "A Thermodynamic Evaluation of Four Si-M (M = Mo, Ta, Ti, W) Binary Systems," *Computer Coupling of Phase Diagrams and Thermochemistry*, vol. 13, no. 3, pp. 273–292, 1989.

[19] A. McConnell, S. Uma, and K. Goodson, "Thermal Conductivity of Doped Polysilicon Layers," in *Proc. of the Intl. Conference on Heat Transfer and Transport Phenomena in Microscale Structures*, G. C. *et al.*, Ed., New York, 2000, pp. 413–419, Begell House.

[20] D. C. Katsis and J. D. van Wyk, "Experimental Measurements and Simulation of Thermal Performance Due to Aging in Power Semiconductor Devices," in *Proc. Industry Applications Conference, 2002, 37th IAS Annual Meeting*, Pittsburgh, USA, 2002, pp. 1746–1751.