Strain Effects on Quasi-Bound State Tunneling in Advanced SOI CMOS Technologies

M. Karner*, E. Ungersboeck*, A. Gehring†, S. Holzer‡, H. Kosina*, and S. Selberherr*
* Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, 1040 Wien, Austria
Phone: +43-1-58801/36016, Fax: +43-1-58801/36099, E-mail: karner@iue.tuwien.ac.at
†AMD Saxony, Wilschdorfer Landstrasse 101, D-01109 Dresden, Germany
‡Christian Doppler Laboratory for TCAD in Microelectronics at the Institute for Microelectronics

Abstract— **We study the influence of uniaxial <110> stress on the gate leakage current in advanced silicon-on-insulator (SOI) CMOS devices. The strain-induced shifts of the conduction band valleys and the valence bands are calculated using linear deformation potential theory. After the evaluation of the band edge profile, using a numerical Schrödinger Poisson (S/P) solver, the leakage current is estimated with the quasi-bound states tunneling formalism in a post processing step. The energy shifts of the primed and unprimed subband ladders due to the applied stress yield a re-population of the subbands. This results in a slight decrease for tensile stress and an increase for compressive stress of the leakage current, respectively. These results are in agreement with experimental studies on n-MOS devices.**

I. INTRODUCTION

The continuous progress in the development of semiconductor devices within the last decades has gone hand in hand with down-scaling the device feature size [1]. For 90 nm gate length and below, strained silicon has become a *sine qua non* to achieve leading-edge transistor performance. However, as the device feature sizes approach the wave length of free electrons, the influence of quantum mechanical effects gains importance. Especially quantum mechanical tunneling has significant impact on the characteristics of state-of-the-art microelectronic devices. Thus, gate leakage remains one of the major limitations to further down scaling. Recently, the stress techniques of state-of-the-art partially depleted silicon-on-insulator (SOI) transistors in 90 nm technology have been scaled to 65 nm. A stress memorization process and a tensile-stressed liner are used to introduce strain in the n-MOS transistor [2] (see Fig.1).

A detailed experimental study of mobility enhancement techniques for uniaxial/biaxial strain was shown in [3]. The effect of uniaxial and biaxial tensile stress on the threshold voltage of n-MOS devices has been studied in detail in [4]. Some basic considerations on the modeling of the strain-induced changes in the gate leakage current density for Si films on $Si_{1-x}Ge_x$ substrates (biaxially strained Si channel) have been reported in [5]. An experimental study of the leakage characteristics of partially depleted (PD) SOI MOSFETs has shown a linear dependence between the tunneling current density and the applied tensile stress [6].

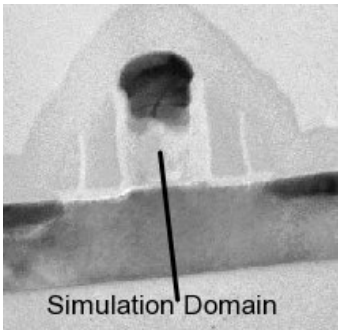

Figure 1: State-of-the-art PD SOI n-MOS Transistor in 65 nm technology (40 nm gate length) with stress memory and tensile-stressed liner (Si film thickness 77 nm) [2].

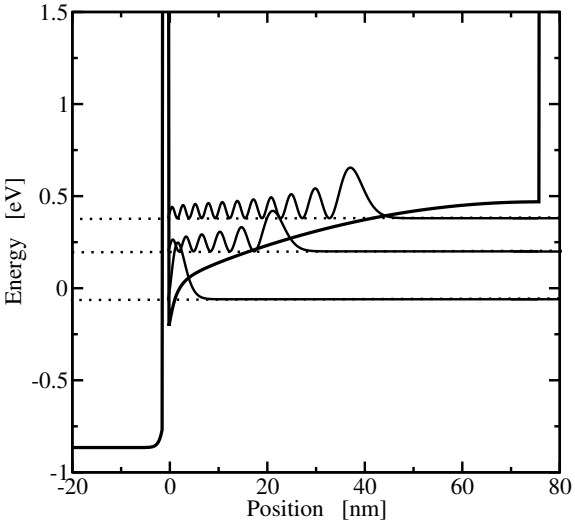

Figure 2: The conduction band edge energy of the n-MOS device at a gate bias of 0.8 V. Energy levels and wavefunctions of some QBS are shown.

We present a model for the efficient simulation of gate currents in highly-scaled MOS devices including strain effects. The effect of strain on the band structure is taken into account using linear deformation potential theory. The outlined methodology is used to investigate the influence of uniaxial stress in <110> direction of a state-of-the-art PD SOI MOSFET as shown in Fig. 1 and Fig. 2.

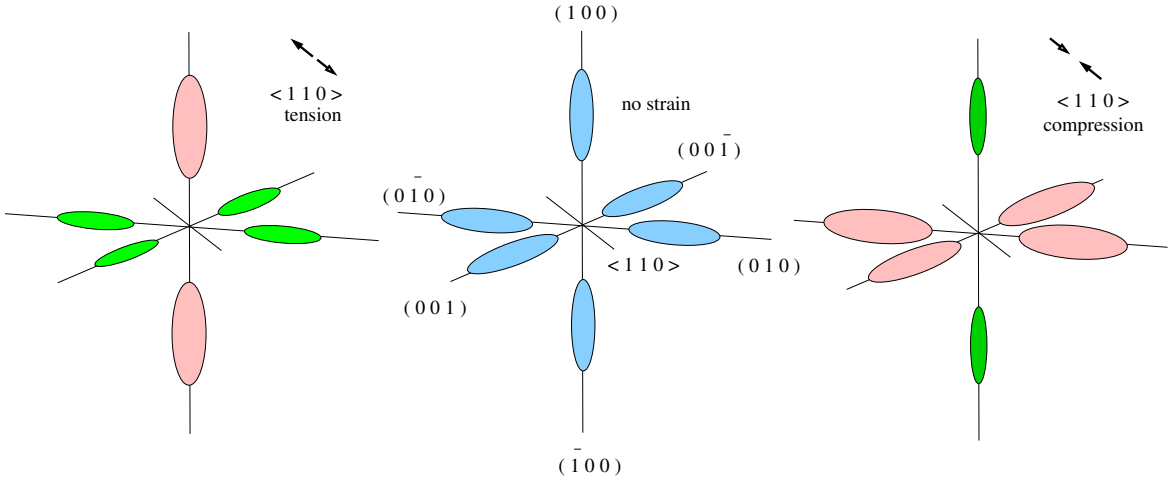

Figure 3: The equi-energy surfaces of the first conduction band of unstrained silicon are shown in the middle part. The effect of the valley shifts for (100) Si due to compressive and tensile stress in <110> direction is shown in the left and in the right part, respectively.

II. EFFECT OF UNIAXIAL STRESS ON THE BANDSTRUCTURE

Within the effective mass framework the conduction band of <100> silicon substrates is characterized by one six-fold degenerate valley including the four-fold primed and the two-fold unprimed valleys. The effective masses are $m_l = 0.916\, m_0$ and $m_t = 0.196\, m_0$, where m_0 is the mass of a free electron [7]. The valence band is treated by a single valley, assuming an isotropic mass $m_v = 0.50\, m_0$.

According to deformation potential theory [8][9], uniaxial stress P along <110> induces a shift between the primed and unprimed subbands as displayed in Fig. 3. To calculate the valley shifts, the strain tensor is related to the stress P for the <110> direction by

$$e_1 = e_2 = P\,(s_{11} + s_{12})/2\,, \tag{1}$$
$$e_3 = P\,s_{12}\,, \tag{2}$$
$$e_4 = e_5 = 0\,, \tag{3}$$
$$e_6 = P\,s_{44}/2\,. \tag{4}$$

Here, the elastic compliance tensor $\tilde{s}$ and the strain tensor $\tilde{e}$ are given in the contracted notation.

Using the shear deformation potentials $\Xi_u = 9.16\,\text{eV}$, $b = -2.35\,\text{eV}$, $d = -5.08\,\text{eV}$, and the hydrostatic deformation potentials $\Xi_d = 9.16\,\text{eV}$, $a = 2.46\,\text{eV}$ [4], the total shift of the valence band ΔE_V, the primed $\Delta E'_C$, and the unprimed ΔE_C valleys are

$$\Delta E'_C = \Xi_d(e_1 + e_2 + e_3) + \Xi_u e_1\,, \tag{5}$$
$$\Delta E_C = \Xi_d(e_1 + e_2 + e_3) + \Xi_u e_3\,, \tag{6}$$
$$\Delta E_V = a(e_1 + e_2 + e_3) + \sqrt{b^2(e_2 - e_3)^2 + (d/2)^2 e_6^2}\,. \tag{7}$$

Using expressions (1) to (7) and setting $e_2 - e_3 = P/2(s_{11} + s_{12} - 2s_{12}) = P/2(s_{11} - s_{12})$, one can express the valley shifts

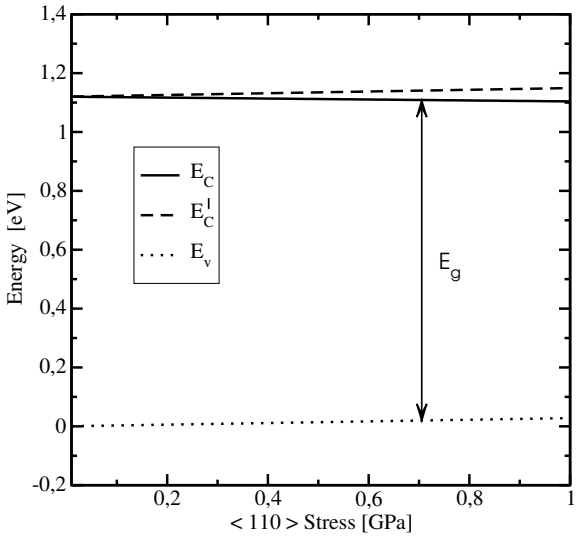

Figure 4: The shift of the conduction band edge and the valence band as a function of the applied stress in <110> direction.

in terms of the stress P in <110> direction as

$$\Delta E'_C = P\left(\Xi_d\,(s_{11} + 2s_{12}) + \Xi_u\,(s_{11} + s_{12})\,/\,2\right), \tag{8}$$
$$\Delta E_C = P\left(\Xi_d\,(s_{11} + 2s_{12}) + \Xi_u\,s_{12}\right), \tag{9}$$
$$\Delta E_V = P\,a\,(s_{11} + 2s_{12}) + (P/2)\sqrt{b^2(s_{11} - s_{12})^2 + (d/2)^2 s_{44}^2}\,. \tag{10}$$

The shifts of the valence bands, of the primed and unprimed conduction band valleys, and the resulting band gap are shown as a function of the applied stress in Fig. 4. A remarkable shift in the threshold voltage of n-MOS devices caused by to strain effects has been reported in [4]. Due to quantum confinement on (001) silicon substrates, the six-fold degenerate conduction

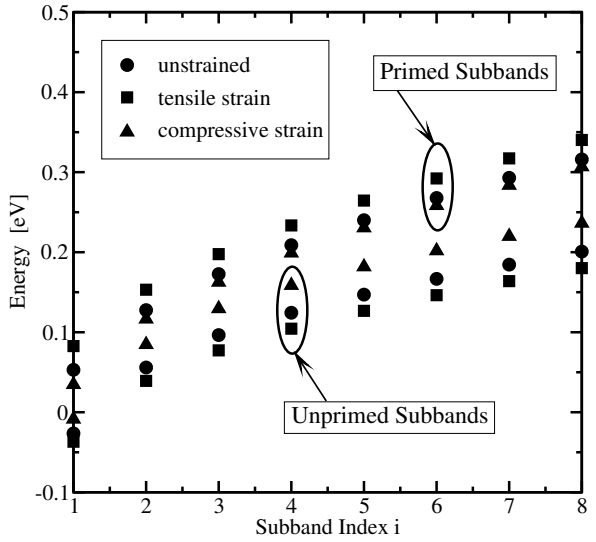

Figure 5: The energies for the primed and unprimed subband ladders as a result of the self-consistent simulation for a PD MOSFET at a gate bias of $0.8\,\mathrm{V}$ are displayed. The shift of the energy levels due to strain can be seen clearly.

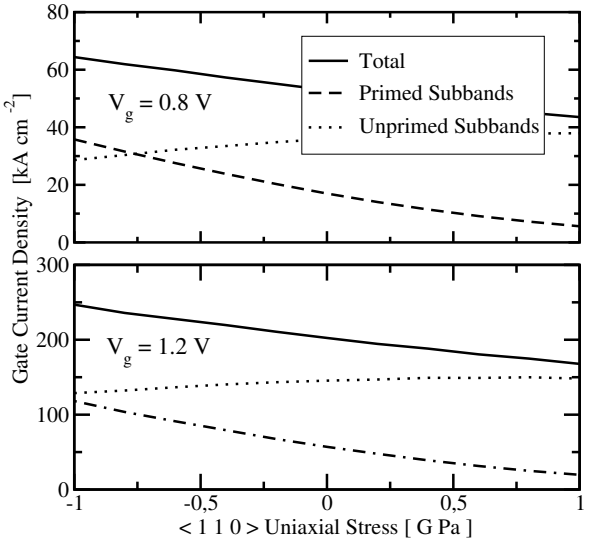

Figure 6: The leakage current as a function of the applied stress is shown. Shifting the valley subband ladders directly results in a change of the contribution to the total QBS tunneling current.

band splits up into a two-fold degenerate (primed) subband ladder with quantization mass $m_\mathrm{q} = m_\mathrm{l}$ and a four-fold degenerate (unprimed) subband ladder with $m_\mathrm{q} = m_\mathrm{t}$.

III. EVALUATION OF THE BAND EDGE PROFILE

Having calculated the valley shift, the electrostatic potential can be acquired using a numerical self-consistent SCHRÖDINGER-POISSON solver [10].

To take into account the strain effects on the conduction band, the resulting band edge energy for each valley is given as the minium energy of the unstrained values E^0_C, the shift of the valleys $\Delta E'_\mathrm{C}$, ΔE_C, and ΔE_V, and the electrostatic potential ϕ as:

$$E'_\mathrm{C} = E^0_\mathrm{C} - \mathrm{q}_0\,\phi + \Delta E'_\mathrm{C}\,, \tag{11}$$

$$E_\mathrm{C} = E^0_\mathrm{C} - \mathrm{q}_0\,\phi + \Delta E_\mathrm{C}\,, \tag{12}$$

The valence band edge energy follows from

$$E_\mathrm{V} = E^0_\mathrm{V} - \mathrm{q}_0\,\phi + \Delta E_\mathrm{V}\,, \tag{13}$$

using the maximum energy of the valence band for the unstrained case E^0_V and the shift given by (10). The shift of the minimum energy of the valleys is calculated in a pre-processing step. The subband ladders follow from the SCHRÖDINGER equation. The self-consistent band edge profile is calculated using an iterative procedure [11].

IV. CALCULATION OF GATE LEAKAGE CURRENTS

It is assumed that the gate leakage current does not influence the electrostatic solution, so that the current can be calculated in a post-processing step. In the channel of SOI MOSFETs, the confinement due to the strong electric field as well as the geometrical confinement lead to a formation of quasi-bound states (QBS) [12]. It has been shown that tunneling via these states can exceed the tunneling from the continuum by orders of magnitude [13], allowing the continuum tunneling to be safely neglected. Each QBS gives rise to a tunneling current determined by the number of electrons occupying the state and the corresponding QBS lifetime of the state (see Fig. 2). A summation over all contributing subband ladders gives the total leakage current.

$$J_\mathrm{2D} = \frac{\mathrm{k_B}T\mathrm{q}}{\pi\hbar^2}\sum_{i,\nu}\frac{g_\nu m_\parallel}{\tau_\nu(\mathcal{E}_{\nu,i}(m_\mathrm{q}))}\ln\left(1+\exp\left(\frac{\mathcal{E}_\mathrm{F}-\mathcal{E}_{\nu,i}}{\mathrm{k_B}T}\right)\right)$$

Here, g_ν denotes the valley degeneracy, $m_\parallel$ the parallel mass, and m_q the quantization masses ($g = 2$: $m_\parallel = m_\mathrm{t}$, $m_\mathrm{q} = m_\mathrm{l}$ for the unprimed valleys and $g = 4$: $m_\parallel = \sqrt{m_\mathrm{l} m_\mathrm{t}}$, $m_\mathrm{q} = m_\mathrm{t}$) for the primed valleys. $\mathcal{E}_{\nu,i}$ and $\tau_{\nu,i}$ denote the energy level and the lifetime of the i^{th} QBS of the ν^{th} valley, respectively.

Fig. 2 shows the investigated MOS structure and some of the quasi bound wavefunctions considering the transversal mass. Within our simulation framework the QBS are obtained from the single particle, time-independent effective mass SCHRÖDINGER equation:

$$-\frac{\hbar^2}{2}\nabla\cdot\left(\tilde{m}^{-1}\nabla\Psi(\mathbf{x})\right)+V(\mathbf{x})\Psi(\mathbf{x})=\mathcal{E}\Psi(\mathbf{x})\,. \tag{14}$$

For the evaluation of the QBS lifetimes, a semi-classical approximation based on corrected closed-boundary eigenvalues using a classical formulation of the escape time (lifetime) [14] can be used. We applied a more rigorous formulation posing open-boundary conditions for the SCHRÖDINGER equation [15].

QBS	$\mathcal{E}_r$ [eV]	N(E_r) [1]	τ_l [ps]	J_G [A cm^{-2}]
1	0.14	6.3×10^{-3}	210	1.7×10^{6}
2	0.27	2.5×10^{-5}	160	8.6×10^{3}
3	0.38	3.4×10^{-7}	140	1.4×10^{2}
10	0.86	3.1×10^{-15}	56	3.2×10^{-6}
15	1.01	5.0×10^{-18}	93	3.1×10^{-9}

Table 2: The QBS of the MOS device for a gate bias of 0.8 V, lifetimes, values of the supply function, and their contribution to the gate current density.

V. APPLICATION AND RESULTS

The PD SOI MOS device structure shown in Fig. 1 has been investigated with the described methodology. The simulation domain is a one-dimensional cross section across the inversion channel of the device. To account for the strain effects on the band structure, the shift of the valleys has been calculated in a pre-processing step. The self-consistent band edge is displayed in Fig. 2. The contribution of some QBS to the leakage current is shown in Tab. 1. Fig. 5 depicts the energy levels of the subband ladders. The shift of the subband energies in the strain is slightly reduced due to the self-consistent calculation, but the upshift and downshift for the primed and unprimed subband ladder, respectively, can be clearly seen.

These shifts result in a re-population of the valleys: As the tensile strain increases, the primed valleys move up and become less occupied, while the unprimed valleys move down and become stronger occupied. As a direct consequence, the gate current increases for the unprimed subbands with increasing tensile strain, while it is reduced for the primed subbands, see Fig. 6. These two competing processes tend to compensate each other. The total electron tunneling current is slightly reduced for tensile stress, while it is slightly increased for compressive stress, as shown in Fig. 7. The same trend has been experimentally observed [6].

VI. SUMMARY AND CONCLUSION

We presented the investigation of the effect of uniaxial stress on the gate leakage current of advanced CMOS devices. The band edge profile is calculated from a self-consistent Schrödinger Poisson solution, taking into account the strain effect on the band structure. The QBS have been calculated from the Schrödinger equation assuming open boundary conditions.

It has been found that the leakage current changes linearly with the applied <110> stress. The major physical effect is the re-population of the primed and unprimed subband ladders. which yields a higher/lower gate leakage current for compressive/tensile strain. Hence, for tensile strain the gate tunneling current slightly decreases, while for compressive strain, the current increases, which is in accordance with experimental results.

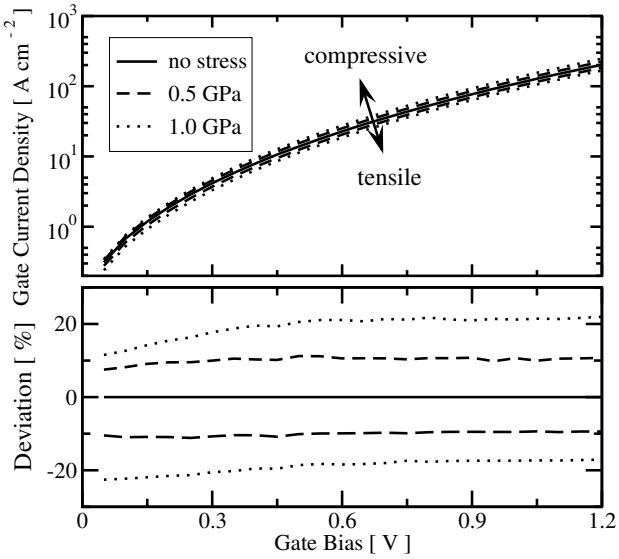

Figure 7: The gate leakage behavior of the investigated device structure for arbitrary stress is shown. The lower figure depicts the influence of compressive and tensile stress on the total current.

ACKNOWLEDGMENT

This work has been partly supported by the European Commission, project SINANO, IST 506844 and from the special research project IR-ON (F2503).

REFERENCES

[1] International Technology Roadmap for Semiconductors - 2005 Edition, 2005, http://public.itrs.net.

[2] M. Horstmann *et al.*, in *Proc. Intl. Electron Devices Meeting* (2005), pp. 233–236.

[3] H. Irie, K. Kita, K. Kyuno, and A. Toriumi, in *Proc. Intl. Electron Devices Meeting* (2004), pp. 225-228.

[4] J. Lim, S. E. Thompson, and J. G. Fossum, IEEE Electron Device Lett. **25**, 731 (2004).

[5] E. Cassan, J.Appl.Phys. **87**, 7931 (2000).

[6] W. Zhao *et al.*, IEEE Electron Device Lett. **26**, 410 (2005).

[7] F. Stern, Phys.Rev.B **5**, 4891 (1972).

[8] C. Herring and E. Vogt, Phys.Rev. **101**, 944 (1956).

[9] I. Balslev, Phys. Rev. **143**, 636 (1966).

[10] M. Karner *et al.*, in *International Workshop on Computational Electronics* (Vienna, 2006), pp. 255-256.

[11] A. Trellakis, A. T. Galick, A. Pacelli, and U. Ravaioli, J.Appl.Phys. **81**, 7880 (1997).

[12] R. Clerc, A. Spinelli, G. Ghibaudo, and G. Pananakakis, J.Appl.Phys. **91**, 1400 (2002).

[13] A. Gehring and S. Selberherr, in *Proc. SISPAD* (2004), pp. 25–28.

[14] A. Dalla Serra *et al.*, IEEE Trans.Electron Devices **48**, 1811 (2001).

[15] M. Karner, A. Gehring, H. Kosina, and S. Selberherr, in *Proc. SISPAD* (2005), pp. 35–38.