Impact of Random Bit Values on NBTI Lifetime of an SRAM Cell

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1. Introduction

Conventional six-transistor CMOS SRAM cell structures are dominantly employed in today's cache memory blocks for advanced microprocessors. The long-term stability of such a CMOS memory cell is strongly affected by NBTI induced degradation of MOSFET parameters (e.g. threshold voltage) which leads to a reduction in the static noise margin (SNM) of the cell [1]. Although the degradation of the Si/SiO_2 interface in p-MOSFET devices caused by negative bias temperature instability (NBTI) has been known for a long time [2], NBTI has become a major reliability problem for newer CMOS technologies [3,4]. It turned out that heavily nitrided gate oxides exhibit a significantly higher NBTI degradation compared to pure SiO_2 for the same physical oxide thickness and voltage condition [5,6]. NBTI induced interface traps affect the key device parameters, V_T and I_{Dsat}, and therefore NBTI reduces the device lifetime. Under dynamic operation, the interface traps generated during the on-state of the MOSFET are partially annealed in the off-state. Therefore the AC degradation is significantly lower than the DC degradation for any given stress time. The magnitude of the NBTI-driven parameter shift over time is also significantly reduced for higher frequency operation or smaller "on" duty cycles [7,8]. While transistor degradation in CMOS-based NAND circuits depends on the AC operating conditions (e.g. clock frequency), in SRAM cells it is possible that a stored bit value does not change for a long time. On the other hand, it would be too strict to equate the lifetime of an SRAM transistor with its DC lifetime. The two p-MOSFETs used in a 6T-SRAM cell are unsymmetrically NBT stressed by the stored bit values. The split of on-state times between the two devices (only either of them is "on") lies well within the boundaries of pure DC stress (100/0 stress-split) and symmetric AC stress (50/50 stress-split). Only a periodically flipping of the bit with comparable on-times would lead to equal parameter degradation of both devices and hence to the longest lifetime of the SRAM cell. The worst-case lifetime of an SRAM cell can be determined by storing a random bit sequence where the probability is, for instance, 90% for storing a "one" (or 90% for storing a "zero") which corresponds to a 90/10 NBT stress-split. In this work, NBTI responses to random bit sequences are studied by using a calibrated reaction-diffusion model.

2. Experimental Details

The investigated SRAM cell was fabricated using a 90nm process. The gate oxide was annealed in an NO_x gas ambient and has a physical oxide thickness of 24Å and an equivalent oxide thickness (EOT) of 20Å. NBTI measurements were performed for the p-MOSFET device under DC and AC gate voltage stress at a constant temperature of 125°C with the source, drain and n-well grounded. For AC stress the used amplitude is identical to the negative DC voltage during the pulse "on" phase and zero during the pulse "off" phase. The NBT stress was interrupted at certain times to measure the threshold voltage and drain saturation current. The threshold voltage V_T was extracted by using a linear extrapolation of $I_D - V_G$ data from the point of maximum transconductance, and the saturation current I_{Dsat} was determined at V_G = -1.2V and V_D = -1.2V.

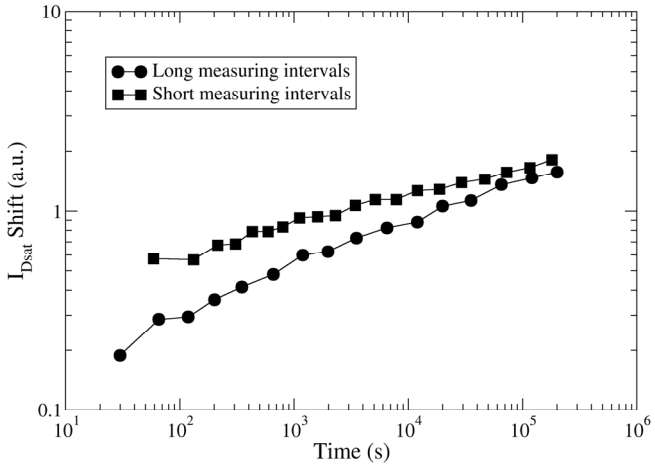

Fig. 1: Influence of relaxation during long measuring intervals on the slope of I_{Dsat} shift at V_G = -1.5V.

Note that the measuring intervals of the tester used for monitoring the key device parameters should be kept as short as possible to minimize the influence of relaxation on the measurement results. Fig. 1 demonstrates that stronger annealing of interface traps occurs during longer relaxation phases in the shorter stress time range, which reduces significantly the device parameter shift. In the longer stress time regime the influence of the relatively short measuring intervals plays a secondary role and the results of long and short intervals become comparable. The longer measuring interval lasts ten times longer than the shorter interval which is beyond one second (Fig. 1).

Voltages were applied from -1.5V up to -2.7V to the gate of the transistor and frequencies were used in the range from DC to 1MHz. The MOSFET parameters V_T and I_{Dsat} were monitored for a maximum stress time of $2 \cdot 10^5$s. The measured NBTI data were then used to calibrate the numerical simulations for the 90nm p-MOSFET device.

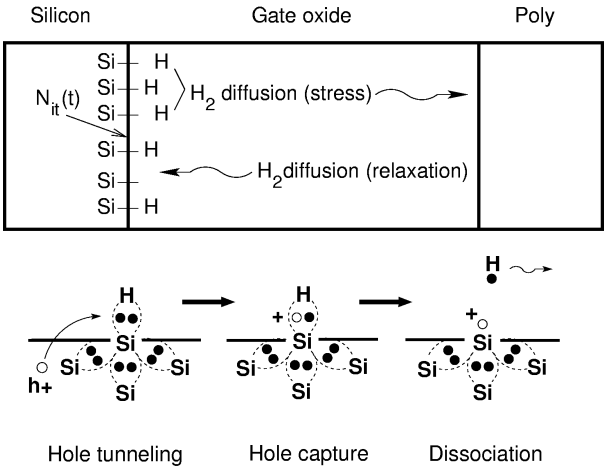

Fig. 2: Schematic description of the one-dimensional R-D model and possible mechanism of breaking interfacial Si-H bonds by inversion-layer holes.

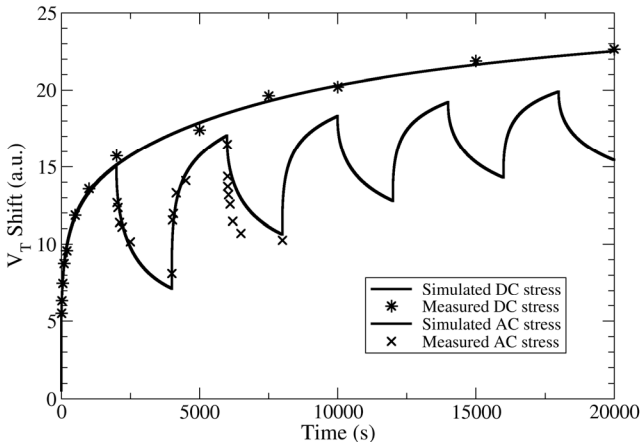

Fig. 3: Comparison of the numerical solution of the calibrated R-D model to measured DC and AC data (stress time: 2000s, relaxation time: 2000s).

3. NBTI Modeling

Although several NBTI models have been developed to explain the physics of interface trap generation based on electrochemical reactions and activation energies, only the reaction-diffusion (R-D) model can explain the power-law time dependence of NBTI induced degradation. The R-D model is well suited for the simulation of NBTI degradation, because this model is capable to predict static and dynamic NBTI data [11-13]. Jeppson and Svensson developed the first model approach in 1977 [2], Ogawa and Shiono generalized the R-D model equations [10], Alam performed numerical simulations for gate oxides of newer technologies [11], and finally Mahapatra verified the model [12,13].

The R-D model states that the NBTI induced p-MOSFET degradation is driven by breaking of hydrogen-passivated silicon bonds at the substrate interface and subsequent diffusion of hydrogen. The formation of interface traps is described by two coupled differential equations:

$$\frac{\partial N_{it}(t)}{\partial t} = k_f [N_0 - N_{it}(t)] - k_r N_{it}(t)\, C_H(x=0,t) \qquad (1)$$

$$\frac{\partial N_{it}(t)}{\partial t} = -D \left.\frac{\partial C_H(x,t)}{\partial x}\right|_{x=0} + \frac{\delta}{2}\frac{\partial C_H(x,t)}{\partial t} \qquad (2)$$

Equation (1) states that the N_{it} generation is determined by a chemical hydrogen release reaction (const. dissociation rate k_f), when the p-MOSFET is biased in inversion. When the transistor is switched off, the forward rate k_f becomes zero and the reverse rate k_r stays unchanged. The parameter N_0 denotes the total Si-H bond density at the interface before stress. Equation (2) is obtained by integration of the standard diffusion equation across the Si/SiO_2 interface with a thickness δ. The diffusion coefficient D is the average diffusivity of the diffusing hydrogen species (atomic and molecular hydrogen). Note that the generated interface traps $N_{it}(t)$ are equal to the number of released hydrogen atoms at any given time t.

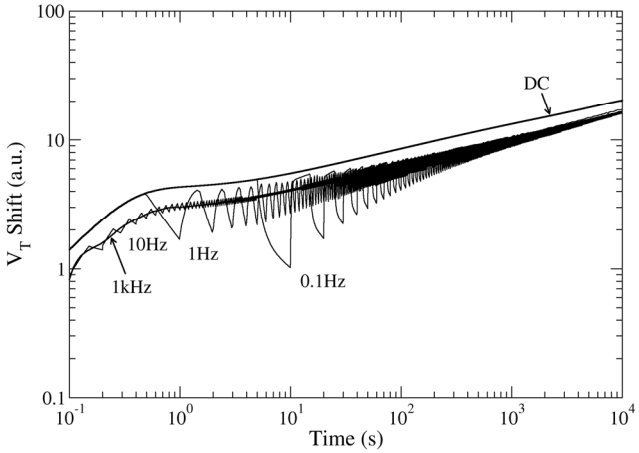

Fig. 4: Simulated NBTI responses to rectangular gate signals for the 90nm p-MOSFET in the frequency range from DC – 1kHz.

The upper sketch in Fig. 2 shows that released hydrogen diffuses into the gate oxide and returns back to the Si/SiO_2 interface when the stress is removed. The active region of the NBTI mechanism is uniformly distributed over the channel according to a one-dimensional problem. The used simulation domain for the diffusing hydrogen is the gate oxide. The discretization of the model equations (1) and (2) is based on a one-dimensional finite differences method with the boundary condition of a partially absorbing wall at the oxide/poly interface [9].

Fig. 3 compares the numerical solution of the calibrated R-D model for DC and AC operation to experimental data of the investigated MOSFET. The V_T degradation under static and dynamic NBT stress was simulated with the same model parameter set. Fig. 4 demonstrates that the calibrated model can be used to study the evolution of the MOSFET parameter degradation over time under DC and symmetric

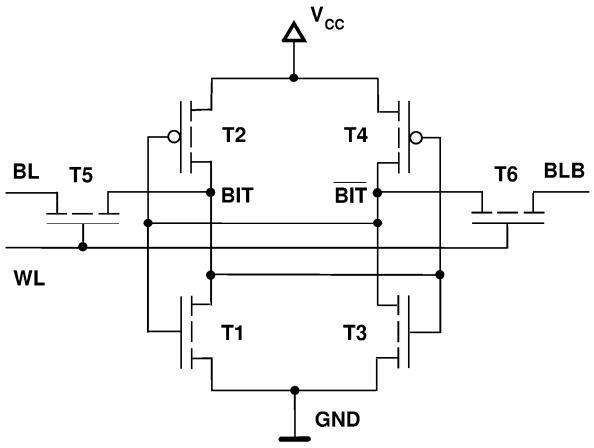

Fig. 5: Schematic of the investigated 6T-SRAM cell.

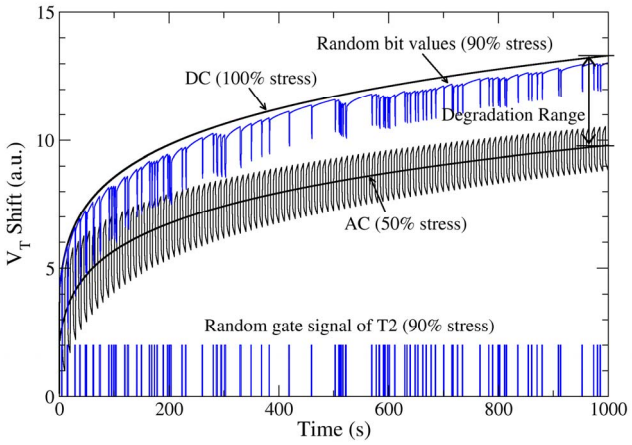

Fig. 6: Comparison of storing random bit values every second with 90% probability for a one to DC and AC degradation of transistor T2.

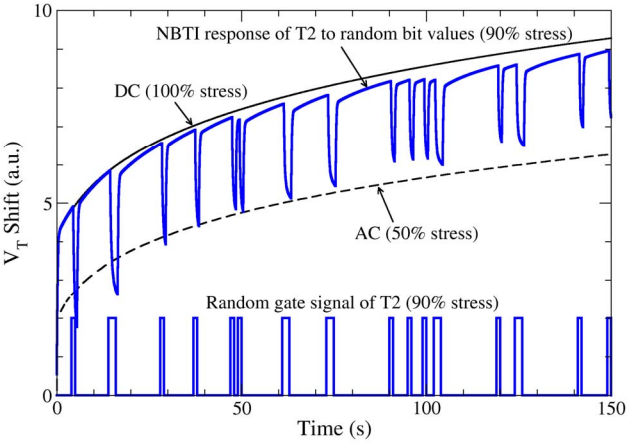

Fig. 7: Comparison of storing random bit values every second with 90% probability for a one to DC and AC degradation of T2 in the early stress time regime.

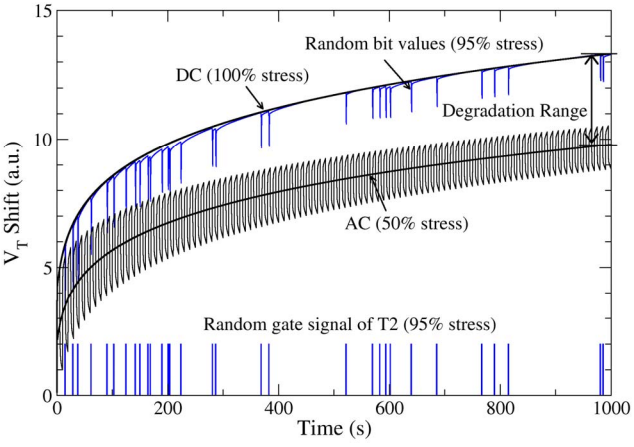

Fig. 8: Comparison of random bit sequence with 95% probability for one to DC and AC degradation of T2.

AC operation. Up to now, there is no agreed industry specification available for the characterization of NBTI lifetime. A reasonable failure criterion for the 90nm CMOS technology is, for instance, to tolerate a maximum shift of 10% for the device parameters V_T and I_{Dsat}.

4. Degradation Analysis of the SRAM Cell

Fig. 5 shows the investigated static RAM cell in schematic form. The memory cell consists of two cross-coupled CMOS inverters (T1, T2 and T3, T4) and the access transistors T5 and T6. While the p-MOSFETs T2 and T4 are affected by NBTI as long as the power is supplied to the cell (at least either of them), the parameter degradation of the comprised n-MOSFETs is neglected in this study. In the high state of the flip-flop (node BIT is high) T2 is under NBT stress and in the other state (BIT low), T4 is stressed.

Fig. 6 shows the NBTI induced V_T parameter degradation of the MOSFET T2 for storing a bit value every second in the memory cell, whereby the probability is 90% for storing a "one". The worst-case parameter degradation of T2/T4 lies always in the range between the envelope degradation curves under DC and under symmetric AC stress. Due to the high unsymmetry between the turn on and off times at a ratio of 90/10 for T2, the V_T degradation lies closer to the DC boundary than to the symmetric AC boundary. Fig. 7 shows the zoomed-in time diagram of the beginning phase from Fig. 6 (first 150 seconds), where the progression of the NBTI response of T2 and the corresponding random gate drive signal can be seen more clearly. The rectangular gate signal of the simulation was derived from a random-number generator which produces uniformly distributed random variates in the interval [0,1].

In the simulation presented in Fig. 8, the overall stress-time of T2 is further increased by storing a random bit sequence with a probability of 95% for a one. It can be observed that the NBTI response curve converges to the DC degradation envelope since the annealing of interface traps during the unfrequent "high" states of the gate signal is not sufficient to reduce the parameter degradation significantly from the degradation under DC stress.

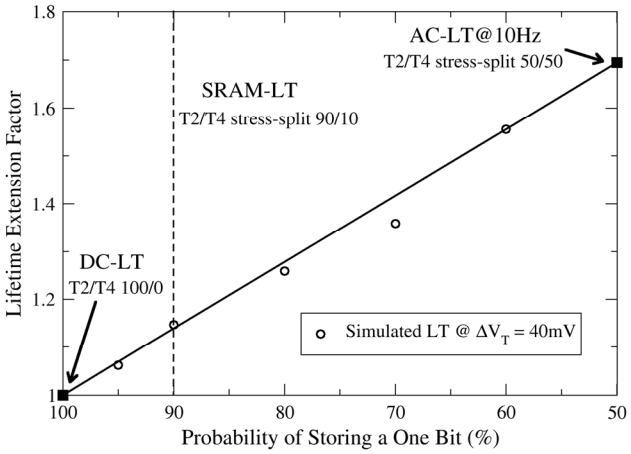

Fig. 9: Simulated lifetime extension of the SRAM cell related to the DC lifetime of the cell for different on-time probabilities of T2.

A data flipping technique for SRAM arrays is proposed in [1] to solve the problem of highly unsymmetrical NBTI degradation of the p-MOSFET devices in SRAM cells. The periodic flipping of the contents of all SRAM cells every 10^5 seconds can be performed either by software or hardware. The presented software and hardware solutions are evaluated by simulations based on the R-D model.

Long-time simulations were performed at a supply voltage of 1.5V under DC and under symmetric AC stress with a 10Hz rectangular gate signal to determine the boundaries for the SRAM cell lifetime. In Fig. 9 we investigate the lifetime extension of the SRAM cell due to the dynamic NBTI effect. The SRAM lifetime is defined here by a V_T shift of 40mV for the device T2 and T4, respectively. The AC lifetime for a symmetric gate signal operation at 10Hz would be 1.7 times longer than the DC lifetime of the memory cell. We found that the SRAM lifetime for storing a random bit sequence with a probability of 90% for storing a one bit (or 90% for a zero bit) is 1.14 times longer than the DC lifetime.

5. Summary and Conclusion

Companies estimate the NBTI lifetime of SRAM memories usually by extrapolation of the DC degradation. This method underestimates the lifetime of the memory cell since the bit change in the cell over time is neglected. In this work we have analyzed the impact of storing random bit values in a 6T-SRAM memory cell by using probabilities of storing a one bit between the boundaries of 100% (fully unsymmetric stress) and 50% (symmetric stress). It turned out that the SRAM lifetime for using an unsymmetry of 90% in the stress-split between T2 and T4 is 1.14 times longer than the DC lifetime. We have also demonstrated that the NBTI degradation of the cell converges to the DC degradation for highly unsymmetric stress levels with a probability of over 90% for a one bit. It turned out that the calibrated reaction-diffusion model is useful to study the NBTI response not only for driving the gate with periodic rectangular signals but also for storing random bit sequences in an SRAM cell.

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