MOS-AK: Open Compact Modeling Forum

Invited IWCM Paper

Wladek Grabinski[1] (editor), Tibor Grasser[2], Gennady Gildenblat[3], Gert-Jan Smit[4], Matthias Bucher[5], Annemarie Aarts[6], Alireza Tajic[4], Yogesh Singh Chauhan[7], Andrzej Napieralski[8], Tor A.Fjeldly[9], Benjamin Iniguez[10], Giuseppe Iannaccone[11], Maher Kayal[7], Werner Posch[12], Gerhard Wachutka[13], Fabien Prégaldiny[14], Christophe Lallement[14], Laurent Lemaitre[15]

[1]MOS-AK.ORG, [2]TU Wien, [3]ASU Phoenix, [4]NXP Semiconductors, [5]TU Crete, [6]TU Eindhoven, [7]EPF Lausanne,[8]TU Lodz, [9]UniK Kjeller, [10]Universidad Rovira i Virgili, [11]Uni Pisa, [12]austriamicrosystems, [13]Munich University of Technology, [14]InESS/ENSPS Illkirch, [15]Freescale

Abstract - MOS-AK is an European, independent compact modeling forum created by a group of the engineers, researchers and compact modeling enthusiasts to promote advanced compact modeling techniques and the model standardization using the high level behavioral modeling languages such as VHDL-AMS and Verilog-A. This invited paper summarizes recent MOS-AK activities and presents advanced topics on the MOSEFTs modeling for low power, analog/RF as well as high voltage applications, gate-all-around MOSFETs ballistic nanoscale modeling solutions, multidomain microsystem modeling, discusses links between compact models and design methodologies and finally introduces elements of the compact models standardization.

***Index Terms* — Standard compact model, surface potential based model, charge based model, MOSFET, HVMOS, PIN Diode, VDMOS, IGBT, MCT, VHDL-AMS, Verilog-AMS**

I. INTRODUCTION

MOS-AK (**MOS**-Modelle und Parameterextraktion **A**rbeits**k**reis) is an European, independent compact modeling (CM) forum [1] created by a group of the engineers, researchers and compact modeling enthusiasts to promote advanced CM techniques and the model standardization using the high level behavioral modeling languages such as VHDL-AMS and Verilog-A. The MOS-AK aims to encourage interaction and sharing of all information related to the CM at all levels of the device and circuit characterization, modeling and simulations. The MOS-AK aspires to build a community with global connections by: promoting standardization of the compact models and its implementation into software tools; connecting national and local modeling groups on European level; building strong bilateral ties with similar organizations around the world. The group conducts regular meetings with European industry and academia to exchange information on the strengths and weaknesses of the industrialization of the compact models [1]. Activities include: drafting of standards and providing a center of competence for engineers, designers, managers and decision makers [2]; evaluating world-wide best practice and success stories; delivering a comprehensive view of the European CM [3]. The MOS-AK believes that the transfer of the advanced CM methodologies to industry can be accelerated by providing the comprehensive reports and reference papers on the subjects of: basic issues and concepts of the device characterization and compact modeling; global CM issues advanced CMOS processes; examples and analysis of best practice of the commercialization of compact models.

This invited paper summarizes recent MOS-AK activities and presents state of the art topics on the MOSEFTs modeling for low power, analog/RF as well as high voltage/power applications, gate-all-around MOSFETs, ballistic nanoscale modeling solutions, multidomain microsystem modeling, discusses links between compact models and design methodologies and finally introduces elements of the compact models standardization.

II. MIXED-MODE DEVICE/CIRCUIT SIMULATION

The accurate description of the various physical mechanisms interacting in modern semiconductor devices has become extremely complicated. While a decade ago the solution of the standard semiconductor equations [4] was sufficient in most cases, this has changed dramatically. Nowadays, accurate device models must be able to capture a plethora of effects which used to be only of secondary importance. The most important of these effects are quantum effects such as confinement in the channel and gate tunneling currents in MOSFETs, non-equilibrium dynamics such as hot carriers and velocity overshoot, self-heating effects due to the increased power-density, and the influence of modern material systems on the device performance, for instance due to the introduction of ultrathin layers and the inclusion of strain.

A highly accurate but still feasible description of such a complicated system is provided by a solution of Boltzmann's transport equation using a proper band structure model, either bulk-like [5] or on quantized energy-levels [6]-[7], coupled to the Schrödinger equation. Quantum effects in transport direction are likely of minor importance for MOSFETs with channel-lengths larger than 10 nm [8]. Unfortunately, the solution of the coupled Boltzmann-Schrödinger system is very time consuming and as such unsuitable for studying the dynamic behavior of a device in a realistic circuit. As a simplification, moment-based models are used in state-of-the-art device simulators [9], which allow for a much faster evaluation, in particular if the solution of the Schrödinger equation is replaced by simplified descriptions [9]. Still at the expense of significantly increased computation time compared to compact models, such a description allows one to include realistic geometries and doping profiles in two or three dimensions [11], and also to use much more accurate models for the physical parameters such as the mobility and their temperature dependences, although not at the same level of accuracy as can be obtained from Boltzmann's equation [12].

An important advantage of moment-based models, such as the classic drift-diffusion model, is that they lend themselves naturally to an inclusion into a mixed-mode device/circuit setting where device and circuit equations are assembled into a single system matrix and solved self-consistently [13][14] using an extension of the modified nodal approach [15]. Although such an approach is feasible and has a number of advantages over compact models, it has to be kept in mind that each numerical device introduces several thousand unknowns to the equation system. This approach is thus limited to a relatively small number of numerical devices embedded into a circuit. However, all techniques originally developed for circuit analysis can be extended to mixed-mode analysis, including large-signal dc, transient [14], small-signal ac [16], harmonic balance [17] and noise analysis [12]. Furthermore, the applicability of this approach can be extended by using compact models for uncritical or already well characterized components restricting the relatively expensive numerical description to the critical devices [11][14][18].

Despite these advantages, however, mixed-mode simulation might be too expensive for the evaluation of realistic circuits in a

production and circuit design environment. However, mixed-mode device/circuit simulators have proven to be excellent complimentary tools [19] which can be particularly useful during the development cycle of a new technology and also for compact models. Since many different physical effects have to be captured by modern compact models the assessment of the final accuracy has become rather involved. In particular, as physically based compact models are derived from the very equations numerical models solve, it is a comparatively easy task to evaluate each aspect individually against its numerical solution. Also, the accuracy of compact models subject to dynamic boundary conditions can be evaluated in a straight-forward manner.

III. Advances in MOSFET Compact Modeling

A. PSP-International Industry Standard

Over the last few years consensus has been reached that the next generation compact MOSFET models must be surface-potential-based. Essentially, only this approach allows one to accurately reproduce device characteristics in a wide range of biases including the accumulation and weak inversion regime and to physically model the source-drain overlap regions increasingly important in scaled-down MOS transistors. In fact, other approaches to MOSFET modeling can be regarded as approximations describing special cases of the surface-potential-based formulation [20].

The PSP model [21] is the latest and most advanced MOSFET model obtained by merging and developing the best features of the two surface-potential-based models: SP [20] and MM11 [22]. In May 2006 it was selected by Compact Model Council as the new industry standard MOSFET model targeted to replace BSIM3/4 for the advanced CMOS designs. As such it includes all effects essential in state of the art of MOS transistors from the reverse short-channel effect to the degradation of the long channel output conductance by the halo doping in advanced MOSFET designs. The PSP model contains both quasi-static [21] and non-quasi-static [23] modules, the most advanced junction model ever and the most complete noise model found in any compact model of MOSFET. Verification of PSP has been achieved by detailed comparison with several technology nodes from a variety of semiconductor companies down to 65 nm processes with 45 nm applications being developed at the present time.

From the theoretical point of view, the development of the PSP model was enabled by the solution of several long-standing problems of MOSFET physics and modeling. These include symmetric linearization method that allows one to develop very simple expressions for both the current and the terminal charges without sacrificing any accuracy relative to the traditional formulations. This has been demonstrated by extensive comparison [21] with the charge-sheet and Pao-Sah models [24], [25]. Another significant theoretical breakthrough underlying the PSP formulation is the rigorous inclusion of the drift velocity fluctuations in the presence of the velocity saturation [26]. Further theoretical advances include the original spline collocation method for solving continuity equation in the PSP NQS model. An interesting feature of PSP is the elimination of the iterative loops inevitably present in all other surface-potential-based MOSFET models. This is accomplished by developing extremely accurate analytical approximations for the solution of the first integral of the Boltzmann-Poisson equation commonly known as implicit surface potential equation. The latter has been modified in [27] to correct the problems encountered in the original formulation. The availability of the surface potential in the source-drain overlap region is another unique feature of PSP leading to physical models of the overlap capacitances, gate tunneling currents, GIDL and GISL and other second-order effects.

Apart from fitting the data, in the process of evaluation by the CMC, PSP has successfully passed a battery of benchmark tests including both the original and newly developed symmetry tests. It enables RF designer to address such issues as intermodulation effects, modeling of passive mixers and variable transconductance circuits previously off limits to the users of models other than SP and PSP [28]. Both the code and documentation for PSP are in public domain and are available for download [29].

B. The EKV3 MOS transistor compact model

The EKV3 MOSFET model is a charge-based compact model for analog/RF IC design. Its origins go back to the 1970ies when weak and moderate inversion in CMOS started to be used among other in Swiss watchmaking [30]. Its early versions were among the first compact models to successfully address moderate inversion, by using an empirical current-voltage relationship [31]. Form very early on, it introduced normalization quantities for current and voltage, later expanded to charge, frequency etc.. It was also among the first to adopt reference to substrate instead of source, and exploits the symmetrical forward-reverse operation of MOS transistors [32]. A design methodology based on the level of inversion (or inversion coefficient, IC) was developed [33]. Altogether, the EKV model approach is much more than a “black box” compact model. Also, special characterization techniques were developed. The pinch-off voltage measurement technique [34] provides immediate information on channel-doping related effects, such as threshold voltage, vertical non-uniform doping [35], and substrate effect. Small-signal transconductances in CMOS technology are characterized versus level-of-inversion and channel length [36], providing a direct aid to circuit designers. Finally, design-aids exploiting the above techniques [97] were developed (see also Section VII.A).

The initial voltage-charge relationship [37]-[38] was then refined to provide an accurate fit to the initial surface potential model, without the use of fitting parameters [39]. This approach is then extended to include polydepletion [40], quantum effects [41], and non-uniform doping [35]. Vertical mobility effects are addressed via three effective-field dependent scattering terms, intimately related to the charge model [38]. Velocity saturation and channel length modulation effects are handled in a symmetric way so as to preserve continuity of higher-order derivatives at VD=VS [38]. Further important specificities of the EKV3 model [42] include developments for non-quasi static (NQS) operation [43], RF operation [44], NQS thermal noise [45] and handling of short-thermal noise [46]. Further detail on EKV3 may be found in [47][48].

IV. High Voltage LDMOS Modeling

A. MOS Model 20

MOS Model 20 [49]-[52] is a compact model for high-voltage LMDOS devices. The model can be used for LDMOS devices with a short drift region (under the thin gate-oxide only), as well as for those with an extended drift region under a thick field oxide. MOS Model 20 is equipped with a dc-model, including impact-ionization, a nodal charge model, and a noise model. In the model, all main characteristics of an LDMOS device are included, like the effect of the gate extending over the drift region and quasi-saturation [52]. Furthermore, MOS Model 20 is completed with both length- and width scaling, as well as with temperature scaling and self-heating. The documentation and source code (in both C and Verilog-A) of the model are available in the public domain [53].

MOS Model 20 is a surface-potential-based model, which

combines the MOSFET channel region with the drift region in one model. The potential at the internal drain at the end of the MOSFET channel region is computed inside the model itself [50]. In the channel region of the device the effects of mobility reduction, velocity saturation and channel length modulation, as well as drain-induced barrier lowering (DIBL) and static feedback are included. In the drift region both accumulation and depletion are included, as well as mobility reduction, velocity saturation and pinch-off. Furthermore, impact-ionization occurring in both the channel region and the drift region is included.

MOS Model 20 has extensively been verified in comparison to measurements, for a wide range of LDMOS devices [49]-[52]. It has proven to give accurate results in all regimes of operation, ranging from sub-threshold to far above threshold, in both the linear and saturation regime. The model demonstrates excellent fits to measured I-V and g-V curves, as well as to capacitances from S-parameter measurements. Typical effects like quasi-saturation, a negative output conductance due to self-heating, and the drop of the gate-drain-capacitance above threshold are accurately described.

MOS Model 20 has been successfully used in circuit simulations, where it has proven its robustness and fastness for use in circuit design. By having all currents, conductances, charges and capacitances continuous, it shows excellent convergence behaviour during circuit simulations. Thus, MOS Model 20 combines accurate descriptions of LDMOS devices with robust and fast circuit simulations.

B. HV-EKV Compact Model

The HV-EKV model has been developed in the framework of 'ROBUSPIC' European Commission project (IST-507653) [54]. The HV-EKV model [55]-[57] is a scalable general high voltage MOSFET model, which can be used for any high voltage MOSFET with extended drift region. This model includes major physical effects like the quasi-saturation, impact-ionization and self-heating. The model has been implemented in the Verilog-A language to make it portable on any commercial circuit simulator. It has been demonstrated [55]-[59] that the accuracy of the model is better than 10% for DC I-V and g-V characteristics and shows good behavior for all capacitances which are unique for these devices showing peaks and shift of peaks with bias variation. The model also exhibits excellent scalability with all physical and electrical parameters such as transistor width, drift length, number of fingers and temperature. The model provides excellent trade-off between speed, convergence and accuracy, being suitable for circuit simulation in any operation regime of high voltage MOSFETs.

Any high voltage MOSFET is considered divided into an intrinsic MOS region and a drift region, as the intrinsic drain voltage (V_K) always remains at low values for the entire bias domain [57]. The intrinsic transistor is modeled using low voltage EKV model (EKV2.6) [95] while modeling of drift region is carried out by the scalable bias dependent resistance [57]. The main reason behind using EKV model for intrinsic channel is that it has physical expressions for current and charges, continuous from weak to strong inversion and, it uses less number of parameters, which can be easily extracted.

The charge associated with gate is the sum of the charges related to intrinsic-drain (V_K), source, body and drift. The charges associated with the intrinsic MOS are directly obtained from EKV model. The drift accumulation charge is obtained by integrating the drift charge density over the gate overlap length, assuming surface potential varies linearly in the drift region. The simulated transfer characteristics of the high voltage VDMOS transistor show that the accuracy is excellent for the entire bias range. The same applies to the C_{GD} vs. V_G curves, demonstrating that the peaks in capacitances are well modeled by the model. Furthermore, the accuracy on capacitances can be improved by implementing the lateral non-uniform doping in the intrinsic MOS channel of high voltage devices [60]-[62].

V. POWER DEVICES COMPACT MODELS

Many CAD programs have been developed in microelectronics and successfully applied to circuit analysis. The question arises, why until now there are no CAD programs suitable for power circuit analysis?

The basic parameters of modern power devices are presented in Table 1.

Table 1. The basic parameters of the most commonly applied modern power devices.

	VDMOS	IGBT	GTO	GCT
V_M [V]	1000	4500	6000	6000
I_T [A]	350	900	6000	6000
t_{ON} [µs]	0.1	0.2	10	-
storage time [µs]	0	6	30	5
f_T [kHz]	2000	100	1	1
V_{ON} [V]	very high	low	very low	very low

In all types of these devices, the blocking capability is a function of the large base width - W and its doping concentration - N_D. For a high value of blocking voltage, the semiconductor devices must have a low doping and a large width of the base. The charge transport through the base cannot be instantaneous and the voltage drop over such structure cannot be neglected.

For example, on-state resistance R_{ON} for a unipolar 1600V device (N_D=1.25E14cm^{-3}) will be equal to 0.462 Ω. In the case of high current, this value is definitely too high.

In the case of a bipolar device, due to the diffusion, maximum current density is much higher and consequently the corresponding voltage drop much lower than in the case of unipolar devices. Additionally, in the bipolar structure some effects resulting from effective base doping changes can appear, for example: the base widening effect, and thyristor effect rendering in the additional current capability.

In the case of power devices with a high value of the electric field, one can assume that all the charge carriers are able to attain their maximum speed. In the case of unipolar devices even for a very large base the transit time is very short and, in the majority of cases, the internal time constant of the device can be neglected, comparing with the time constant of the external circuit.

The situation is different in the case of the bipolar devices. The transit time through the large base is very long and the internal time constant of bipolar devices can be much larger than the time constants of the external circuit. In such a case, a simple lumped model cannot be any longer used. It is necessary to take into account the carrier transport inside the bipolar devices and a distributed model should be applied. Until now such a model has not existed in the commonly used circuit CAD simulation programs.

In the case of the unipolar devices like VDMOS, in the normal mode of operation, majority carriers are responsible for the current conduction. Therefore, it is possible to build a relatively simple compact model [64][69][70] taking into account all internal elements of unipolar structure.

In the case of unipolar devices we have:

- no problem with the diffusion phenomena
- very good accuracy with the lumped models
- clear physical/geometrical interpretation of model parameters
- distributed models are necessary only for modelling of the body diode operation.

Such a simple approach cannot be applied in the case of a bipolar structure such as PIN diode, BJT, thyristor, or IGBT. All the important phenomena occur in the large base (in this case in the N^- region):

- there is a problem with the diffusion (minority carriers)
- the accuracy of computation is very poor with the lumped models, therefore new compact models are very welcome
- for correct simulation, distributed models are still necessary

The designers of power circuits need relatively simple models which can be applied in standard SPICE-like circuit simulation programs with the possibility of high power circuit simulation. In order to make the power device simulation possible, a new type of the PIN diode compact model has been proposed [72], where the so-called 'modular' approach is applied with several regions of different physical and/or electrical nature. This approach allows for decreasing the simulation time considerably without any important loss of accuracy [65]-[67].

The well known, one-dimensional Benda-Spenke model [63] has been adopted for this purpose. The behaviour of stored charge carriers can be described by means of the ambipolar diffusion equation, solution of which is obtained with a numerical algorithm. A new efficient, the CWENO[1] scheme [68], is used to ensure high computational stability and good accuracy.

The negative voltage drop in the space charge region can be calculated applying the Poisson's equation [72] with application of Newton-Raphson method. In the proposed approach, the simulation software runs on a network server and the user interface is provided by a web page ensuring data entry point and result presentation [73][74].

The circuit simulation core has been based on SPICE because of high popularity and strong position of SPICE-like simulators. Simulation results obtained with the proposed model and the developed simulation environment show a good agreement with 2D simulations performed with other simulators [66] based on the finite boxes method. Erroneous results are obtained however with the built-in SPICE diode model with fitted parameters.

Having developed a better PIN diode model, it is possible to simulate a realistic behaviour of circuits containing power diodes and VDMOS transistors. One should note that a professional design process might require the designer to consider the electro-thermal couplings in power devices. However, it seems that the developed tool offers new possibilities in comparison to currently available commercial CAD packages.

VI. New CM Architectures

A. Short-channel DG and GAA MOSFET Modeling

Nanoscale double gate (DG) and cylindrical gate-all-around (GAA) MOSFETs have been identified as strong candidates for replacing the conventional bulk MOSFET in the coming five to ten years, to meet the ever growing demand for high-speed, low-power CMOS circuitry [75]. A major impetus for this advance is the improved gate control and the concomitant reduction in short-channel behavior offered by these device designs.

To achieve the needed accuracy, the multi-dimensionality of the potential and inversion charge distributions has to be taken into account. In the subthreshold regime of operation, the electrostatics in the device body is dominated by the capacitive coupling between the source, drain and gate electrodes. We have found that for the DG MOSFET, the 2D Laplace's equation can be conveniently solved by conformal mapping techniques [76]-[81], yielding analytical results in a complex, transformed plane. The mapping back to the real device geometry is performed by means of first order elliptic integrals.

The GAA MOSFET is basically a 3D structure and cannot be analyzed directly the same way. One possibility is to solve Poisson's equation in cylindrical coordinates by means of a series expansion in Bessel functions [82]. However, we have found that the above analytical results for the DG structure can be successfully applied to the GAA as well, by performing an appropriate scaling of the device to compensate for the difference in gate control between the two devices [83]. Important parameters in this procedure are the characteristic lengths of penetration λ_{DG} and λ_{GAA} of electrostatic influence from the source and drain towards the device center for the DG and GAA geometries, respectively. Hence, for modeling a GAA device of length L, we calculate the potential distribution for a DG device with length $L' = L\lambda_{DG}/\lambda_{GAA}$. The resulting potential distribution is then compressed uniformly in the length direction using the scaling factor $\lambda_{GAA}/\lambda_{DG}$ and assigned to the GAA MOSFET.

In strong inversion, the electrostatics of the DG and the GAA MOSFET approach the long-channel behavior described in [84] and [85], respectively. The potential distribution is then dominated by the inversion charge, allowing it to be self-consistently described by a 1D Poisson's equation in Cartesian (DG) or polar (GAA) coordinates. A drain current model based on the classical drift- diffusion formalism was used. The modeling was applied to nanoscale DG and GAA MOSFET with gate length of 25 nm, silicon film thickness of 12 nm, and insulator of thickness 1.7 nm and a relative dielectric permittivity of 7. A midgap gate metal was assumed. Both the modeled electrostatics and drain current have been verified by comparisons with numerical device simulations from the Silvaco's Atlas device simulator.

B. Ballistic Nanoscale MOSFETs

In ballistic transistors, charge carriers traverse the channel without suffering inelastic and undesired elastic scattering events. The only type of scattering occurring is due to the potential barrier in the channel modulated via the gate voltage. In the channel two populations of carriers are present: those injected by the source and still in equilibrium with the source reservoir (forward states), and those injected by the drain and therefore in equilibrium with the drain reservoir (reverse states). Transport is controlled only through the maximum potential energy in the channel, corresponding to the peak of the barrier formed by conduction band edge between source and drain [86]. Electrostatics in the device is dominated by the charge density at the peak of the conduction band edge barrier, which is controlled by the voltage applied to the terminals both through geometrical capacitances and by the so-called "quantum" capacitances, i.e., the derivatives of the charge injected through each contact as a function of the potential at the barrier peak. A closed form solution for ballistic MOSFETs has been derived by Natori [87] and reformulated by Ren et Lundstrom [88] and Wang et Gindelblat [89]. A closed-form solution similar to the Natori model, with the advantage of being analytical, explicit and inherently symmetric, has been proposed in [90].

A partial degree of scattering has been addressed by introducing a "backscattering coefficient" which takes into account the ratio of forward charge carriers that are backscattered in the channel and contribute to the reverse flux [91]. Alternatively, it has been recently shown that starting from the Büttiker probes interpretation of dissipative transport [92], a description of DGMOSFETs in the intermediate regime between ballistic and drift diffusion transport is rigorously possible in terms of a chain of ballistic MOSFETs [90]. When the MOSFET is fully ballistic, the equivalent chain reduces to one single ballistic MOSFET; when transport occurs in a quasi-equilibrium regime, such as that described by drift-diffusion

[1] CWENO – Centered Weighted Essentially Non-Oscillatory.

currents, the equivalent chain consists of a large number N of ballistic transistors in series, where N is approximatively the ratio of the channel length to the mean free path. A chain with a small number N corresponds to a quasi ballistic MOSFET. Further, it has been demonstrated that a chain of N ballistic transistors can be effectively reduced to a series of only two transistors with a common gate: a drift-diffusion transistor close to the source and a ballistic transistor close to the drain. In such a way, the series of the drift-diffusion transistor and of the ballistic transistor is a compact macromodel capable of describing transistors with any degree of scattering, and is suitable for circuit simulation with an acceptable overhead. The case of degenerate carrier statistics in ballistic transistors has been addressed in [93].

VII. TRANSISTOR LEVEL DESIGN

A. Procedural Analog Design Tool - PAD

PAD is a chart-based design environment dedicated to the design of analog circuits aiming to optimize design and quality by assisting designers to find good tradeoffs [94]. The charts approach enables the transcription of a set of mathematical relations into an appropriate interactive graphical representation. This interactive tool allows step-by-step the design of analog cells by using guidelines for each analog topology. At each step, the user modifies interactively one subset of the design parameters and observes the effect on other circuit parameters. At the end, an optimised design is ready for Spice like simulation, verification and fine-tuning. The analog basic structures design embedded in PAD uses the complete set of equations of the EKV MOS model [95], which links the equations for weak and strong inversion in a continuous way. In addition to this, the present version of PAD covers the procedural design of transconductance amplifiers (OTAs) and different operational amplifiers topologies. This design methodology is based on g_m/I_D [96], and therefore uses the inversion factor as a main design parameter.

At basic cell level, an analog structures library is embedded in PAD, such as: single NMOS or PMOS device, current mirror, differential pair, cascode stage, cascode current mirrors, etc. For each structure, a set of general parameters (small signal model, DC biasing values, parasitic capacitances, noise, speed, etc.) is graphically displayed. Some specific parameters are also shown (maximum DC offset for diff. pair, current mismatch for current mirror, etc). This enables to analyze basic structures behavior in the environment of a given circuit, and observe parameters that are important for design trade-offs. The basic analog structure sizing consists in setting priority targets (gain, noise, speed, etc). After the bias current is set and the g_m/I_D ratio is chosen, according to the electrical circuit specifications, the only variables to change are: transistor width W and transistor length L. Simultaneously, the changes of all other parameters can be observed. This methodology can be used for sizing, as well as for optimization and resizing of circuit blocks.

The current PAD tool version enables systematic design of operational transconductance amplifiers (OTAs) and different operational amplifiers structures and linear voltage regulators. Each of these cells is partitioned into basic analog structure and the procedural design methodology is applied. The procedural design flow is illustrated here on the example of a folded cascode OTA circuit. The procedural analog design flow implemented in PAD for this design consists of: circuit partitioning into basic analog structures, basic analog structures sizing and circuit level design. For each topology proposed in PAD, a set of circuit level design equations is integrated in PAD, at each step of design the reached circuit performances is presented in a graphical way to the designer [97][98][99].

In addition to the PAD tool, an automatic converter engine from BSIM to EKV module has been realized. This last one extracts the EKV MOS model parameters used in PAD from BSIM parameters. This tool uses Spice simulator to perform an extensive simulation of different MOS devices dimensions. Then implemented mathematical fleeting algorithms are provided to realize the extraction of EKV MOS model. Finally, included benchmarks OTA cells are used to display and allow the designer to compare simulation results obtained from BSIM original parameters and EKV generated one [100].

B. Random Mismatch in Compact Models

The functionality and circuit yield of analog semiconductor circuits (e.g. operational amplifiers, bandgap reference circuits, A/D converters, etc.) relies on good matching properties of devices used. Random mismatch caused by local variations of the production process strongly influences the critical electrical parameters of the circuit components. Considering device mismatch during the design phase enables yield prediction and improved circuit robustness. Based on extensive statistical measurements of matched pairs using special test structures, mismatch parameters are extracted to be part of circuit simulation libraries for Monte Carlo simulation.

Random mismatch is defined as the local parameter variation of semiconductor devices with identical layout placed close to each other and describes electrical differences of a matched pair. The mismatch is caused by the random nature of the process steps (e.g. ion implantation or dopant diffusion).

This leads to a local variation of important electrical parameters of the device, such of the threshold voltage V_{TH} and the current gain factor K_P in case of a MOSFET.

For any matched pair of transistors and the electrical parameter P, let P_1 and P_2 denote parameter values for each individual device. The mismatch of P is described by the statistical distribution of $\Delta P = P_1 - P_2$. In case of pure random mismatch, $\Delta P \sim N(\mu,\sigma)$ is normal distributed and the mean value μ is close to zero indicating no systematic offsets. The standard deviation $\sigma(\Delta P)$ is the relevant mismatch parameter.

Generally, large devices show small random mismatch [106] which holds up to a specific device area. For larger device area mismatch becomes even worse when global parameter variations within the device are reached. Special assigned pair structures, like common centroid and interleaved layouts are used to compensate these systematic effects [103]. This technique additionally reduces the influence of temperature gradients on the wafer, which may cause considerable mismatch [107].

As can be expected, the parameter variations ΔP are quite small quantities and the crucial points for mismatch parameter extraction are the application of a proper model and the according parameter extraction strategy. It can be distinguished between direct methods, where model parameters P_1, P_2, are extracted separately for each transistor of the matched pair and so called current-mismatch-fitting methods, where the variance $\sigma(\Delta P)$ is determined by a fit to $\sigma(\Delta I_D/I_D)$ versus V_{GS} characteristics [101]-[106]. In both cases the accuracy of the used drain current model and the accuracy of the measurement strongly influence the results achieved. Generally, simple drain current models are used and the extraction is performed for less correlated parameters. Simple models reduce the extraction effort and additionally provide well determined results due to small or negligible parameter correlation. On the other hand the model does not consider e.g. parasitic contact resistances and for the saturation region DIBL effects and velocity saturation.

Commonly used direct methods to extract mismatch of the

threshold voltage and current gain factor are the maximum slope method, the three points method and the four points method [101]. The indirect current-mismatch-fitting method fits a simple model over a large bias range, where modeling errors are averaged out over several parameters. It gives a reasonable estimate of the mismatch behaviour.

The measurement data for ΔP consists of the mismatch part and additionally of unwanted parts due to measurement noise and contact resistance fluctuations. Large devices are most susceptible to measurement noise because their intrinsic mismatch is quite low. A figure of merit is the correlation coefficient between the original and a repeated measurement. Further, a change to a larger current measurement range will decrease the measurement repeatability drastically [101].

The current-mismatch-fitting method fits a simple model over a large bias range, where modeling errors are averaged out over several parameters. It gives a reasonable estimate of the mismatch behaviour.

VIII. Multi-Energy domain-Coupled Microsystem Models

A. Specific Aspects of MEMS Modeling

In spite of what they have in common, there are several aspects in which microsystems technology largely differs from integrated circuit (IC) technology. ICs are composed of a rather limited number of elementary device structures, fabricated by means of quasi-standardized design rules and process technologies. In the field of MEMS, however, an ever growing variety of different device types has emerged, based on a large number of widely differing (and sometimes quite unconventional) fabrication technologies. Therefore, today's challenge in the computer-aided IC design consists in mastering very complex system topologies built up by a huge number of simple basic elements, whereas in the computer-aided design of micromechatronical systems we face the problem of describing systems with simple topology built up by a comparably small number of constituent devices which, however, exhibit a high functional complexity based on quite sophisticated physical operating principles.

The complexity of microsystems originates in particular from the intricate coupling between different energy and signal domains which, on the one hand, is the inherent and much desired property of any sensor or actuator element in a microsystem and, on the other hand, is an undesired detrimental property when it occurs as parasitic cross-coupling between the system components. Hence the accurate analysis of all kinds of physical coupling effects has a major impact on the optimization of microsystems and is, thus, the most important issue that has to be tackled in the computer-aided design of microsystems.

B. Lumped Element and Compact Models

On physical device level, MEMS simulation is based on continuous-field models (CFM), where one deals with spatially distributed field quantities, if needed as a function of time. However, with a view to assessing the performance of a microsystem, the analysis primarily aims at integral quantities such as input-output characteristics, response functions and transients characterizing the function of the constituent components. To this purpose, the degrees of freedom in the CFM description have to be largely reduced by proper approximations. This makes it possible to calculate the operational behavior of the real microsystem component by an equivalent but much simpler "reduced order model" that still reproduces all important physical effects of the device operation correctly, but allows, by virtue of its relative simplicity, the simulation of the component behavior on the system level [107][109]. The usual approach is to derive an equivalent lumped element network from the simulated field distributions. The dynamic behavior is then described by a set of coupled compact models, where the model parameters have been extracted from physics-based but much more complicated continuous-field device simulations.

C. Microsystem Macromodels Based on Kirchhoffian Network Description

Finally, on system level, all the compact models representing the individual constituent elements of a microsystem are linked together in order to study the behavior of the system as a whole under the operating conditions of interest. An elegant and powerful physics-based methodology for this is provided by a thermo-dynamic system description in terms of driving forces and resulting fluxes of the relevant physical quantities [110][111]. Partitioning the system into blocks and lumping the exchange of flux quantities between adjacent blocks along common interfaces into single nodes eventually yields a full system description as "Generalized Kirchhoffian Network", which is governed by generalized mesh rules and node rules for each pair of conjugate fluxes and driving forces (e.g., electric current – voltage, heat flow – temperature, mass flow – pressure, etc.). This constitutes a natural approach to microsystem simulation, because the coupling between the different energy and signal domains is governed by basic physical balance equations for energy, particle numbers, mass, charge, and other extensive quantities. The resulting full system macromodel is equivalent to a system of ordinary algebro-differential equations for the node variables, which can be straightforwardly solved using a standard analog network simulator.

One should note that only one of a pair of conjugate quantities is determined inside the blocks, whereas the respective conjugate one can be calculated from the conservation laws governing the network. So the Kirchhoffian network description is, in a certain sense, the natural extension of electric circuit theory, where the branch currents and node voltages are determined by the systematic application of the "current sum rule" at the nodes and the "voltage mesh rule" along a closed loop of the network, but now with the extension that also physical quantities other than electrical charge are allowed to flow through the network.

The Kirchhoffian network description is also useful for testing the function of one (or a few) system element(s) on the device level (i.e. continuous-field level), when they are embedded in the full system environment (for instance, a sensor element coupled to the electric circuitry [112]). To this end, a few selected single components are modeled using the device-level (CFM) description, while the rest of the system is treated using conventional system-simulation techniques. This approach is referred to as "mixed mode" simulation, since physically-based numerical models and semi-analytical compact models are used concurrently.

A generic software approach to MEMS compact modeling based on generalized Kirchhoffian networks is a hardware description language like VHDL-AMS, which represents a standardized model interface in analog network simulators and, furthermore, allows the description of arbitrary physical energy and signal domains in addition to the electrical quantities.

IX. CM Standardization

A. Compact Modeling of Emerging Technologies with VHDL-AMS

The modeling team of the InESS research institute [113] deals with the compact modelling of bulk MOSFET and advanced

technologies such as double-gate (DG) MOSFET and CNTFET (Carbon NanoTube FET), for a use in design of analog and mixed circuits. Its major goal is to bring simple solutions, numerically efficient and close to the physics of the device. InESS compact modelling group also studies the capabilities of VHDL-AMS for developing compact models [114]-[116].

VHDL-AMS [117] is a HDL language which supports the modeling and the simulation of analog and mixed-signal systems. It supports the description of continuous-time behavior. For compact modeling, the most interesting feature of the language is that it provides a notation for describing Differential Algebraic Equations (DAEs) in a fairly general way [114]. The *simultaneous* statements and the way the quantities (bound to terminals or free) are declared allow the designer to write equations in either implicit or explicit format. VHDL-AMS supports the description of networks as conservative-law networks and signal-flow networks. As such, it supports the description and the simulation of multi-discipline systems at these two levels of abstraction. Conservative-law relationships assume the existence of two classes of specialized quantities, namely *across* quantities that represent an effort (e.g., a voltage for electrical systems), and *through* quantities that represent a flow (e.g., a current for electrical systems).

For the model end-user (circuit designer), the most important part of the VHDL-AMS model is the interface, contained in what is called an *entity* in VHDL-AMS. The model interface includes the specification of generic parameter and interface port. The *generic* statement allows the designer to define its own values for the model parameters. Typically, geometrical W and L transistor parameters are defined as generic for bulk and DG MOSFET.

Following its involvement in the development of the EKV v2.6 MOSFET model [95], InESS compact modeling group has developed different VHDL-AMS codes of this model, including or not thermo-electrical interactions and extrinsic aspects [114]-[115]. Some -beta- versions of these VHDL-AMS models of EKV v2.6 can be downloaded in [116].

Another study aimed at developing in VHDL-AMS a simplified version of the MM11 Philips model taking into account the quantum mechanical effects [114][115][118]. Currently, InESS group is working on the compact modeling with VHDL-AMS of nano-electronic devices such as double-gate MOSFET [119]-[121] and CNTFET [122]-[124].

In addition to the above-mentioned works, InESS group and co-workers achieved a detailed study on commonalities and differences between the two mixed-signal hardware description languages, VHDL-AMS and Verilog-AMS, in the case of modeling heterogeneous or multidiscipline systems [114]. The VHDL-AMS and Verilog-AMS source files of [114] can be downloaded in [116].

In conclusion, InESS compact modeling team has demonstrated, during the last years, the usefulness and efficiency of VHDL-AMS as a powerful tool for circuit simulation including emerging semiconductor devices.

B. Bring Today's Compact Models into Simulators using ADMS

This section gives a brief overview of the solutions currently available to bring compact models into simulators. Compact models can be viewed as a set of electrical equations that describe at different levels of precision the electrical properties of semiconductor micro-structures [125][126]. MOS transistors and bipolar transistors are amongst the most familiar examples of semiconductor micro-structures. Recently the Compact Modeling Council (CMC) adopted Verilog-AMS [127] as the standard language to write the electrical equations of compact models. In the last two years more and more companies and universities are using this language to code the electrical equations of compact models. NXP (formerly Philips Semiconductors) and the Arizona State University are delivering the successive releases of PSP [29] – the new CMC-approved standard MOS transistor model in the Verilog-AMS format. They also provide a release in the C format language automatically derived from the Verilog-AMS code. The Technical University of Dresden (HICUM team [131]) and the Technical University of Delft (MEXTRAM team [132]) are proposing a Verilog-AMS-based implementation of their bipolar compact models on their respective download web sites. It is interesting to note that just recently the MEXTRAM team decided to move the source code of MEXTRAM to sourceforge.net - an open-source development web site [132]. Using a high-level behavioral description language for compact modeling makes far easier the development of compact models. All the fine-tuning work of bringing compact models into simulators goes to the shoulders of the EDA companies. This allows the compact model developers to better focus on the modeling performances of their models. Today the major EDA companies offer a solution to run on the fly simulations of electrical circuits that include Verilog-AMS coded files. An open source software tool—called automatic device model synthesizer (ADMS)—that supports and simplifies compact model development, implementation, distribution, maintenance, and sharing has been proposed by Freescale [128]-[130]. ADMS has been designed to make these tasks simple, efficient, and robust. The ADMS tool parses the Verilog-AMS code and saves the code into an intermediate representation. Then the intermediate representation is translated into a new format. The way the new format is created is entirely specified by xml scripts. To each simulator interface is associated a set of xml scripts. Some companies (i.e. Cadence) make freely available the xml scripts that they wrote for their simulator interfaces.

Acknowledgements

This paper is the result of the joint contribution of independent reaserch teams. The following reaserchers have spent a considerable amount of time and effort contributing to the scientific discussions during our common work on the manuscript: A. Bazigos, H. Børli, T.-C. Chen, A. Jha, R. Entner, R. van Langevelde, X.Li, E. Kazazis, S. Kolberg, F. Krummenacher. G. Mugnaini, M. Napieralska, F. Pecheux, A. Roy, J.-M. Sallese, A.-J. Scholten, Ł. Starzak, D. Stefanovic, S. Sukharev, B. Świercz, O. Triebl, M. Zubert, H. Wang, W. Wu.

The editor (WG) would like to personaly acknowledge following individuals for the international promotion of the MOS-AK activities: J. Assenmacher, P. Bendix, G. Coram, S. Cristoloveanu, C. Enz, A.Ionescu, A. Juge, T. Gneiting, D.B.M. Klaassen, G. Knoblinger, W. Kraus, W. Kuzmicz, P. Martin, P. Mawby, P. Mawet, M. Mierzwinski, D. Tomaszewski, E. Seebacher, S. Schmidt, F. Sischka, V. Spitsyn, A. Vachoux, S. Yoshitomi.

Grateful thanks are extended to Prof. Giorgio Baccarani and the ESSDERC/ESSCIRC Steering Committee for offering posibility to organize sersies of the MOS-AK Workshops as well as to Prof. Hiroshi Iwai and the IEEE ED Society.

The MOS-AK activities would not be possible without continuous support provided by the academic organizations (EPFL, IMEC, InESS/ENSPS Illkirch, Uni Hannover, K.U.Leuven, Uni Stuttgart), commercial companies (AMS, AMIS, Atmel, Cascade Microtech, CSEM, Bosch, Infineon, Freescale (formerly Motorola), NXP (formerly Philips Semiconductors), STM, Xfab), as well as software vendors (Ansoft, Agilent, CST, Mentor Graphics, Synopsys)

References

[1] Web site: www.mos-ak.org

[2] Withe Paper: http://www.mos-ak.org/hvmos_white_paper.php

[3] W. Grabinski, B. Nauwelaers, D. Schreurs (Eds.), "Transistor Level Modeling for Analog/RF IC Design", Springer-SBM, 2006, ISBN 1-4020-4555-7

[4] S. Selberherr, Analysis and Simulation of Semiconductor Devices, Springer, Wien-New York, 1984.

[5] A. Abramo et al., "A Comparison of Numerical Solutions of the Boltzmann Transport Equation for High-Energy Electron Transport Silicon," IEEE ED., vol. 41, no. 9, pp. 1646-1654, 1994.

[6] M.V. Fischetti and S.E. Laux, "Monte Carlo Study of Electron Transport in Silicon Inversion Layers," Phys.Rev.B, vol. 48, no. 4, pp. 2244-2274, 1993.

[7] C. Jungemann, A. Emunds, and W.L. Engl, "Simulation of Linear and Nonlinear Electron Transport in Homogeneous Silicon Inversion Layers," ., vol. 36, no. 11, pp. 1529-1540, 1993.

[8] V. Sverdlov, T. Grasser, H. Kosina, and S. Selberherr, "Scattering and Space-Charge Effects in Wigner Monte Carlo Simulations of Single and Double Barrier Devices," in 11th International Workshop on Computational Electronics Book of Abstracts, Wien, May 2006, pp. 29-30.

[9] T. Grasser, C. Jungemann, H. Kosina, B. Meinerzhagen, and S. Selberherr, "Advanced Transport Models for Sub-Micrometer Devices," in Proc. SISPAD, Munich, Germany, Sept. 2004, pp. 1-8.

[10] C. Jungemann, C.D. Nguyen, B. Neinhs, S. Decker, and B. Meinerzhagen, "Improved Modified Local Density Approximation for Modeling of Size Quantization in NMOSFETs," in Proc. 4th Intl. Conf. on Modeling and Simulation of Microsystems, Hilton Head Island, South Carolina, USA, Mar. 2001, pp. 458-461.

[11] M. Stockinger, A. Wild, and S. Selberherr, "Drive Performance of an Asymmetric MOSFET Structure: The Peak Device," Microelectronics Journal, vol. 30, no. 3, pp. 229-233, 1999.

[12] C. Jungemann and B. Meinerzhagen, Hierarchical Device Simulation: The Monte-Carlo Perspective, Springer, Wien-New York, 2003.

[13] K. Mayaram and D.O. Pederson, "Coupling Algorithms for Mixed-Level Ciruit and Device Simulation," IEEE Trans.Computer-Aided Design, vol. 11, no. 8, pp. 1003-1012, 1992.

[14] T. Grasser, Mixed-Mode Device Simulation, Dissertation, TU Wien, 1999, http://www.iue.tuwien.ac.at.

[15] C.W. Ho, A.E. Ruehli, and P.A. Brennan, "The Modified Nodal Approach to Network Analysis," IEEE Trans.Circuits and Systems, vol. CAS-22, no. 6, pp. 504-509, 1975.

[16] S.E. Laux, "Techniques for Small-Signal Analysis of Semiconductor Devices," IEEE TED., vol. 32, no. 10, pp. 2028-2037, 1985.

[17] F. Bonani, S.D. Guerrieri, G.Ghione, and M. Pirola, "A TCAD Approach to the Physics-Based Modeling of Frequency Conversion and Noise in Semiconductor Devices under Large-Signal Forced Operation," IEEE TED, vol. 48, no. 5, pp. 966-977, 2001.

[18] T. Grasser and S. Selberherr, "Fully-Coupled Electro-Thermal Mixed-Mode Device Simulation of SiGe HBT Circuits," IEEE TED., vol. 48, no. 7, pp. 1421-1427, 2001.

[19] V. Palankovski, N. Belova, T. Grasser, H. Puchner, S. Aronowitz, and S. Selberherr, "A Methodology for Deep Sub-0.25 um CMOS Technology Prediction," IEEE TED., vol. 48, no. 10, pp. 2331-2336, 2001.

[20] G. Gildenblat, H. Wang, T.-L. Chen, X. Gu, and X. Cai, "SP: An advanced surface-potential-based compact MOSFET model," IEEE J Soild-State Ciruits, vol. 39, no. 9, pp. 1394-1406, Sep. 2004.

[21] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, G.D.J. Smit, A.J. Scholten and D.B.M. Klaassen, "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation ", IEEE TED, Vol. 53, No. 9, September 2006, pp. 1979-1993

[22] R. van B. Nauwelaers, D. Schreurs (Eds.), , A. J. Scholten, and D. B. M. Klaassen, MOS11 Compact MOSFET Model Summary. Available online: http://www.nxp.com/Philips_models/mos_models/model11/

[23] H. Wang, X. Li, W. Wu, G. Gildenblat, R. van Langevelde, G.D.J. Smit, A.J. Scholten and D.B.M. Klaassen, "A Unified Nonquasi-Static MOSFET Model for Large Signal and Small-Signal Simulation", IEEE TED, Vol. 53, No. 9, September 2006, pp. 2035-2043

[24] H.C. Pao and C.T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors," S-SE., vol. 9, no. 10, pp. 927-937, Oct. 1966.

[25] J. R. Brews, "A charge-sheet model of the MOSFET," S-SE, vol. 21, no. 2, pp. 345-355, Feb. 1978.

[26] J. C. J. Paasschens, A. J. Scholten, and R. van Langevelde, "Generalizations of the Klaassen-Prins equation for calculating the noise of semiconductor device," IEEE TED, vol. 52, no. 11, pp. 2463-2472, Nov. 2005.

[27] W. Wu, T.-L. Chen, G. Gildenblat, and C. C. McAndrew, "Physics-based mathematical conditioning of the MOSFET surface potential equation," IEEE TED, vol. 51, no. 7, pp. 1196-1199, Jul. 2004.

[28] P. Bendix, P. Rakers, P. Wagh, L. Lemaitre, W. Grabinski, C.C. McAndrew, X. Gu, and G. Gildenblat, Proc., "RF Distortion Analysis with Compact MOSFET Models", Proc. IEEE 2004 CICC pp. 9-12

[29] Available: http://pspmodel.asu.edu/

[30] E. Vittoz, "Micropower Techniques", Design of VLSI Circuits for Telecommunication and Signal Processing, ed. J.E. Franca and Y.P.Tsividis, Chapter 5, Prentice Hall, 1993.

[31] C. C. Enz, F. Krummenacher, E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", J. Analog Int. Circ. Signal Processing, Vol. 8, pp. 83-114, 1995.

[32] E. Vittoz, C. Enz, F. Krummenacher, „A Basic Property of MOS Transistors and its Circuit Implications, Workshop on Compact Models -- 6th Int. Conf. on Modeling and Simulation of Microsystems (MSM 2003), San Francisco, California, USA, February 23-27, 2003.

[33] D. M. Binkley, C. E. Hopper, S. D. Tucker, B. C. Moss, J. M. Rochelle, D. P. Foty, "A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design", IEEE Trans. Computer-Aided Design of Int. Circ. & Syst., pp. 225-237, Vol. 22, N° 2, February 2003.

[34] M. Bucher, C. Lallement, C. Enz, "An Efficient Parameter Extraction Methodology for the EKV MOSFET Model", Proc. IEEE Int. Conf. on Microelectronic Test Structures (ICMTS'96), Vol. 9, pp. 145-150, Trento, Italy, March 25-28, 1996.

[35] C. Lallement, M. Bucher, C. Enz, "Modelling and Characterization of Non-Uniform Substrate Doping", S-SE, Vol. 41, N° 12, pp. 1857-1861, December 1997.

[36] M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, Y. Papananos, "Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS", Proc. 9th IEEE Conf. on Electronics, Circ. & Syst. (ICECS 2002), Vol. III, pp. 1183-1186, Dubrovnik, Croatia, September 15-18, 2002.

[37] M. Bucher, C. Enz, C. Lallement, F. Theodoloz, F. Krummenacher, "Scalable GM/I Based MOSFET Model", Int. Semicond. Device Research Symp. (ISDRS'97), pp. 615-618, Charlottesville, Virginia, December 1997.

[38] M. Bucher, “Analytical MOS Transistor Modeling for Analog Circuit Simulation”, Ph. D. Thesis N°2114 (1999), Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland, 2000.
[39] J.-M. Sallese, M. Bucher, F. Krummenacher, P. Fazan, “Inversion Charge Linearization in MOSFET Modeling and Rigorous Derivation of the EKV Compact Model”, S-SE, Vol. 47, pp. 677-683, 2003.
[40] J.-M. Sallese, M. Bucher, C. Lallement, “Improved Analytical Modelling of Polysilicon Depletion for CMOS Circuit Simulation”, S-SE, Vol. 44, N°6, pp. 905-912, June 2000.
[41] C. Lallement, J.-M. Sallese, M. Bucher, W. Grabinski, P. Fazan, “Accounting for Quantum Effects and Polysilicon Depletion from Weak to Strong Inversion in a Charge-Based Design-Oriented MOSFET Model”, IEEE TED, Vol. 50, N° 2, pp. 406-417, February 2003.
[42] M. Bucher, C. Enz, F. Krummenacher, J.-M. Sallese, C. Lallement, A.-S. Porret, “The EKV 3.0 MOS Transistor Compact Model: Accounting for Deep Submicron Aspects” (Invited Paper), WCM, 5th Int. Conf. on Modeling and Simulation of Microsystems (MSM 2002), pp. 670-673, San Juan, Puerto Rico, USA, April 2002.
[43] A.-S. Porret, J.-M. Sallese, C. Enz, "A Compact Non Quasi-Static Extension of a Charge-Based MOS Model", IEEE TED, Vol. 48, N° 8, pp. 1647-1654, 2001.
[44] C. Enz, “An MOS Transistor Model for RF IC Design Valid in All Regions of Operation”, IEEE Trans. Microwave Theory and Tech., Vol. 50, N° 1, pp. 342-359, 2002.
[45] A.-S. Porret, C. C. Enz, “Non-Quasi-Static (NQS) Thermal Noise Modeling of the MOS Transistor”, IEE Proc. Circuits, Devices and Syst., Vol. 151, N° 2, pp. 155-166, 2004.
[46] A. S. Roy, C. C. Enz, “Compact Modeling of Thermal Noise in the MOS Transistor”, IEEE TED, Vol. 52, N° 4, pp. 611-614, April 2005.
[47] M. Bucher, A. Bazigos, F. Krummenacher, J.-M. Sallese, C. Enz, “EKV3.0: An Advanced Charge Based MOS Transistor Model”, in W. Grabinski, B. Nauwelaers, D. Schreurs (Eds.), Transistor Level Modeling for Analog/RF IC Design, pp. 67-95, ISBN 1-4020-4555-7, Springer, 2006.
[48] C. C. Enz, E. A. Vittoz, “Charge-based MOS Transistor Modeling”, John Wiley & Sons, ISBN 0-470-85541-X, 2006.
[49] A.C.T. Aarts and R. van Langevelde, “A robust and physically based compact SOI-LDMOS Model”, in Proc. ESSDERC, pp. 455-458, 2002.
[50] A.C.T. Aarts, N. D’Halleweyn and R. van Langevelde, “A surface-potential-based high-voltage compact LDMOS transistor model”, IEEE TED, Vol. 52, No. 5, pp. 999-1007, 2005.
[51] A.C.T. Aarts, R. van der Hout, R. van Langevelde, A.J. Scholten, M. Willemsen, and D.B.M. Klaassen, “Compact modelling of high-voltage LDMOS devices”, Tech. Proc. NSTI Nanotech, pp. 93-98, 2005.
[52] A.C.T. Aarts and W.J. Kloosterman, “Compact Modeling of High-Voltage LDMOS Devices including Quasi-Saturation”, IEEE TED, Vol. 53, No. 4, pp. 897-902, 2006.
[53] www.nxp.com/Philips_Models
[54] *ROBU*st mixed signal design methodologies for *S*mart *P*ower *IC*s (http://www-g.eng.cam.ac.uk/robuspic/).
[55] Y. S. Chauhan et al., "A Compact DC and AC Model for Circuit Simulation of High Voltage VDMOS Transistor", IEEE International Symposium on Quality Electronic Design (ISQED), March 2006.
[56] Y. S. Chauhan et al., "A Highly Scalable High Voltage MOSFET Model", IEEE European Solid-State Device Research Conference (ESSDERC), Sept. 2006.
[57] Y. S. Chauhan et al., "Scalable General High Voltage MOSFET Model inlcuding Quasi-Saturation and Self-Heating effect", article in press at S-SE.
[58] C. Anghel et al., "A Physical Analysis of High Voltage MOSFET Capacitance Behaviour", IEEE International Symposium on Industrial Electronics (ISIE), June 2005.
[59] C. Anghel et al., "New Method for Threshold Voltage Extraction of High Voltage MOSFETs based on Gate-to-Drain Capacitance Measurement", IEEE Electron Device Letters (EDL), Vol. 27, No. 7, pp. 602-604, July 2006.
[60] Y. S. Chauhan et al., "Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs", accepted at IEEE International Electron Devices Meeting (IEDM), Dec. 2006.
[61] Y. S. Chauhan et al., "A New Charge based Compact Model for Lateral Asymmetric MOSFET and its application to High Voltage MOSFET Modeling", accepted at IEEE International Conference on VLSI Design, Jan. 2007.
[62] A. S. Roy et al., "Partitioning Scheme in the Lateral Asymmetric MOST", IEEE European Solid-State Device Research Conference (ESSDERC), Sept. 2006.
[63] H. Benda, A. Hoffmann, E. Spenke, “Switching processes in alloyed PIN rectifiers”, S-SE, Vol. 8, pp. 887–906, 1965.
[64] K. Djellabi, M. Napieralska, H. Tranduc, P. Rossel, K. Kassmi, “Modèles du transistor MOS de puissance,” Revue Générale de l'Electricité, N° 6, Juin 1992, pp. 8 16.
[65] H. Goebel, “A unified method for modeling semiconductor power devices,” IEEE Trans. Power Electronics, Vol. 9, No. 5, pp. 497-505, 1994.
[66] M. Grecki, G. Jablonski, A. Napieralski, “MOPS – parallel environment for simulation of electronic circuits using physical models of semiconductor devices,” 4th European PVM/MPI Users’ Group Meeting, Krakow, Poland, pp. 478-485, 1997.
[67] Ph. Leturcq, M.O. Berraies, J.-P. Laur, P. Austin, “Full dynamic power bipolar device models for circuit simulation”, Power Electronics Specialists Conference (PESC), Fukuoka, Japan, pp. 1695-1703, 1998.
[68] D. Levy, G. Puppo, G. Russo: “Central WENO schemes for hyperbolic systems of conservation laws,” Mathematical Modelling and Numerical Analysis, Vol. 33, No. 3, pp. 547-571, 1999.
[69] M. Napieralska, H. Tranduc, C. E. Cordonnier, J. P.Berry, P. Rossel, “Power MOSFET's library builder for switching circuits simulation and design,” Symposium on Materials and Devices for Power Electronics (MADEP), Florence, Italy, September 2-6 1991.
[70] A. Napieralski., M. Napieralska, “New Approach to Power Semiconductor Devices Modeling,” 6th International Symposium Diagnostics and Yield: Advanced Silicon Devices and Technologies for ULSI Era, Warsaw, Poland, June 22-25, 2003
[71] T. L. Quarles, A. R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli: SPICE3 version 3F5 user’s manual. Department of EECS, University of California, Berkeley, USA, 1994.
[72] L. Starzak, M. Zubert, A. Napieralski, “The new approach to the power semiconductor devices modelling,” International Conference on Modeling and Simulation of Microsystems (MSM), April 22-25 2002, San Juan, Puerto Rico, pp. 640-644.
[73] B. Swiercz, L. Starzak, M. Zubert, A. Napieralski, “An interactive website as a tool for CAD of power circuits,” Technical Proceedings of the 2003 Nanotechnology Conference and Trade Show (NanoTech), San Francisco, CA, U.S.A., 2003, pp. 346 349.
[74] B. Wilamowski, A. Malinowski, J. Regnier, “Internet as a new graphical user interface for the SPICE circuit simulator,” IEEE Transactions on Industrial Electronics, Vol. 48, No. 6, pp. 1266–1268, Dec. 2001.
[75] J. S. Woo, K. W. Terrill, P. K. Vasudev, "Two- dimensional analytic modeling of very thin SOI MOSFETs," IEEE TED, Vol. 37, pp. 1999-2005, 1990.
[76] E. Weber, Electromagnetic fields, vol. 1 - Mapping of fields, Wiley, New York, 1950.

[77] S. Kolberg, T. A. Fjeldly, "2D Modeling of nanoscale DG SOI MOSFETs in the subthreshold regime," J. Comp. Electronics, Vol. 5, pp. 217-222, 2006.
[78] S. Kolberg, T. A. Fjeldly, "2D Modeling of nanoscale double gate SOI MOSFETs using conformal mapping", Physica Scripta, Vol. T125, pp. 1-4, 2006.
[79] S. Kolberg, T. A. Fjeldly, B. Iñiguez, "Self-consistent 2D compact model for nanoscale double gate MOSFETs, Lecture Notes in Comp. Science, Springer, Berlin, Vol. 3994, pp. 607-614, 2006.
[80] T. A. Fjeldly, S. Kolberg, B. Iñiguez, "Precise 2D compact modeling of nanoscale DG MOSFETs based on conformal mapping techniques," Proc. NSTI Nanotech, Workshop on Compact Modeling, Boston, May 7-11, 2006, V. 3, pp. 668-673, 2006.
[81] B. Iñiguez, T. A. Fjeldly, A. Lazaro, F. Danneville, M. J. Deen, "Compact modeling solutions for nanoscale double-gate and gate-all-arpond MOSFETs,"IEEE TED, Vol 53, pp. 2128-2142, 2006.
[82] H. A. Hamid, B. Iñíguez, D. Jiménez, J., Roig, J., Pallarès, L. F. Marsal, "Two-dimensional analytical theshold voltage roll-off and subthreshold swing for undoped cylindrical gate all around MOSFET," S-SE., Vol. 50, pp. 805-812, 2006.
[83] S. Kolberg, H. Børli, T. A. Fjeldly, "Modeling, verification and comparison of short-channel double gate and gate-all-around MOSFETs" accepted for publication. J. Math. and Comp. in Simulations,.
[84] Y. Taur, X. Liang, W. Wang, H. Lu, "A continuous, analytic drain-current model for DG MOSFETs," IEEE Electron Device Letters, Vol. 25, pp. 107-109, 2004.
[85] B. Iñiguez, D. Jiménez, J. Roig, H. A. Hamid, L.F. Marsal, J. Pallarès, "Explicit continuous model for long- channel undoped surrounding gate MOSFETs," IEEE Trans. on Electron Devices, Vol 52, pp. 1868-1873, 2005.
[86] C. R. Crowell, M. Hafizi, "Current transport over parabolic potential barriers in semiconductor devices," IEEE TED, Vol. 35, pp. 1087-1095, 1988.
[87] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistors", J. Appl. Phys., Vol. 75, pp. 4879-4890, 1994.
[88] Z. Ren, M. Lundstrom "Simulation of nanoscale MOSFETs: a scattering theory interpretation", Superlatt. Microstruct. Vol. 27, 177-189, 2000.
[89] H. Wang and G. Gildenblat, "Scattering matrix based compact MOSFET model", IEDM Tech Dig, pp. 125-128, 2002.
[90] G. Mugnaini and G. Iannaccone "Physics-Based Compact Model of nanoscale MOSFETs—Part I: Transition from drift-diffusion to ballistic transport", IEEE TED, vol. 52, pp. 1795-1801, 2005.
[91] A. Rahman and M. Lundstrom, "A Compact Scattering model for the nanoscale Double Gate MOSFET", IEEE TED, Vol. 49, pp. 481-489, 2002.
[92] M. Buttiker, "Role of quantum coherence in series resistors", Phys. Rev. B., Vol. 33, pp. 3020-3026, 1986.
[93] G. Mugnaini and G. Iannaccone, "Physics-based Compact Model of Nanoscale MOSFETs - Part II: Effects of Degeneracy on Transport.
[94] PAD web site:
legwww.epfl.ch/CSL/PAD/PAD_pages/DesignToolHome.html
[95] M. Bucher, C. Lallement, C. Enz, F. Théodoloz and F. Krummenacher, "The EPFL-EKV MOSFET Model Equations for simulation, Version 2.6" Technical Report, EPFL, July 1998, available on-line: http://legwww.epfl.ch/EKV
[96] F. Silveira, D. Flandre, P.G.A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a Silicon-on-Insulator micropower OTA", IEEE Journal of Solid-State Circuits, 31 (1996) 1314-1319.
[97] D. Stefanovic, M. Kayal, M. Pastre, "PAD: A New Interactive Knowledge-Based Analog Design Approach", Analog Integrated Circuits and Signal Processing, 42, 291-299,2005. Special Issue of Journal on International Symposium on Quality Electronic Design. pp.292-299.
[98] M. Kayal, Stefanovic D., Pastre M., "CMOS Analog Design Educational Tool". 5th Europen Workshop on Microelectronics Education, Lausanne, Switzerland. April 15-16, 2004. Klower Academic Publishers pp.133-138.
[99] M. Kayal and M. Blagojevic, Design Methodology Based on the Analog Blocks Retargeting from Bulk to FD SOI Using EKV Model. MIXDES- Gdynia - Poland , 22-24 June 2006.
[100] Danica Stefanovic, François Krummenacher, Marc Pastre, Maher Kayal, "BSIM2EKV: a tool for automatic conversion from BSIM to EKV model". TAISA 04 5ème colloque sur le Traitement Analogique de l'Information, du Signal et ses Applications. Lausanne, Suisse, 30 Septembre et 1 Octobre 2004. pp 85-88
[101] J. A. Croon, W. Sansen, H. E. Maes, Matching Properties of Deep Sub-Micron Mos Transistors, Springer, 2005.
[102] J. Bastos, M. Steyaert, A. Pergoot and W. Sansen: Mismatch Characterisation of Sub micron MOS Transistors, Analog Integrated Circuits and Signal Processing, 12, 95-106(1997), Kluwer Academic Publisher, Boston, 1997.
[103] J.Bastos, M. Steyaert, B. Graindourze, W. Sansen: Matching of MOS Transistors with Different Layout Styles, Proceedings of the 1996 IEEE International Conference on Microelectronic Test Structures, Vol.9, March 1996.
[104] S. J. Lovett, R. Clancy, M. Welten, A. Mathewson and B. Mason: Characterising the Mismatch of Sub micron MOS Transistors, Proceedings of the 1996 IEEE International Conference on Microelectronic Test Structures, Vol.9, March 1996.
[105] U. Grünebaum, J. Oehm, K. Schumacher, „Mismatch Modelling for Large Area MOS Devices", Universität Dortmund, AG Mikroelektronik, Germany, 1997.
[106] M. Pelgrom, A. Duinmaijer and A. Welbers: Matching Properties of MOS Transistors, IEEE Journal of Solid-State Circuits, Vol.24, October 1989.
[107] H. Camenzind, Designing Analog Chips, 2005
www.designinganalogchips.com
[108] P. Voigt, G. Schrag, G. Wachutka, "Methods for model generation and parameter extraction for MEMS", in Simulation of Semiconductor Processes and Devices, K. De Meyer and S. Biesemans, Eds., pp. 149-152, Wien, New York: Springer, 1998.
[109] P. Voigt, G. Wachutka, "Compact MEMS Modeling for Design Studies", Proc. of 3rd Int. Conf. on Modeling and Simulation of Microsystems (MSM-2000), San Diego, CA, U.S.A., March 27-29, 2000, pp. 134-137
[110] G. Wachutka, "Tailored modeling of miniaturized electro-thermomechanical systems using thermodynamic methods", in Micromechanical Sensors, Actuators, and Systems, Eds.: D. Cho, J. P. Peterson, A. P. Pisano, C. Friedrich, DSC-40, ASME, New York, pp. 183-197, 1992.
[111] G. Wachutka, "Coupled Field Modeling of Microdevices and Microsystems", in Simulation of Semiconductor Processes and Devices 2002 (Proc. of SISPAD 2002), Kobe, Japan, Sept. 4-6, 2002, pp. 9-14.
[112] M. Handtmann, R. Aigner, R. Nadal, G. Wachutka, "Methodology of Macromodeling Demonstrated on Force Feedback Σ/Δ-Architectures", Proc. of 3rd Int. Conf. on Modeling and Simulation of Microsystems (MSM-2000), San Diego, CA, U.S.A., March 27-29, 2000, pp. 138-141.
[113] http://www-iness.c-strasbourg.fr/Axe4-ModComp.htm
[114] F. Pêcheux, C. Lallement, and A. Vachoux, "VHDL-AMS and Verilog-AMS as alternative hardware description languages for efficient modelling of multi-discipline systems," IEEE Trans.

Computer-Aided Design, vol. 24, no. 2, pp. 204–224, 2005.
[115] C. Lallement, F. Pêcheux, A. Vachoux, and F. Prégaldiny, Transistor Level Modeling for Analog/RF IC Design, Chapter 9, pp. 243-269, edited by W. Grabinski, B. Nauwelaers, and D. Schreurs, Springer Verlag 2006, ISBN 1-4020-4555-7.
[116] http://lsmwww.epfl.ch/tcad_paper/
[117] 1076.1-1999 IEEE Standard VHDL Analog and Mixed-Signal Extensions Language Reference Manual, IEEE press edition, 1999, ISBN 0-7381-1640-8.
[118] F. Prégaldiny and C. Lallement, "Fourth generation MOSFET model and its VHDL-AMS implementation, Int. Journ. of Numerical Modelling: Elec. Networks, Devices and Fields, vol. 18, pp. 39-48, 2005.
[119] J-M. Sallese, F. Krummenacher, F. Prégaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," S-SE., vol. 49, no. 3, pp. 485-489, 2005.
[120] F. Prégaldiny, F. Krummenacher, J-M. Sallese, B. Diagne, and C. Lallement, "An explicit quasi-static charge-based compact model for symmetric DG MOSFET," in Proc. NSTI-Nanotech 2006, WCM, vol. 3, pp. 686–691, 2006, ISBN 0-9767985-8-1.
[121] F. Prégaldiny, F. Krummenacher, B. Diagne, F. Pêcheux, J-M. Sallese, and C. Lallement, "Explicit modelling of the double-gate MOSFET with VHDL-AMS," Int. Journ. of Numerical Modelling: Elec. Networks, Devices and Fields, vol. 19, no. 3, pp. 239-256, 2006.
[122] F. Prégaldiny, C. Lallement, B. Diagne, J.-M. Sallese, and F. Krummenacher, "Compact Modeling of Emerging Technologies with VHDL-AMS," in Proc. Specification & Design Languages (FDL'06), pp. 23-30, Sept. 19-22, 2006, Darmstadt, Germany.
[123] F. Prégaldiny, C. Lallement, and J.-B. Kammerer, "Design-oriented compact models for CNTFETs," in Proc. IEEE Int. Conf. Design & Test of Integrated Systems in nanoscale technology (DTIS'06), pp. 34-39, Sept. 05-07, 2006, Tunis, Tunisia.
[124] F. Prégaldiny, J.-B. Kammerer, and C. Lallement, "Compact Modeling and Applications of CNTFETs for Analog and Digital Circuit Design," to be presented at 13th IEEE Int. Conf. Electronics, Circuits and Systems (ICECS'06), Dec. 10-13, Nice, France.
[125] W. Grabinski, L. Lemaitre, C. Mcandrew, "Compact Device Modeling Using Verilog-Ams and ADMS", Electron Technology vol. 35 (2003), No.3, pp. 1-5
[126] W. Grabinski, D. Tomaszewski, L. Lemaitre, and A. Jakubowski, "Standardization of the compact model coding: non-fully depleted SOI MOSFET example", Journal of Telecommunications and Information Technology, (2005), No.1, pp.135-141
[127] Web site: http://www.eda.org/verilog-ams/
[128] L. Lemaitre, C. McAndrew, S. Hamm, "ADMS-automatic device model synthesizer" Custom Integrated Circuits Conference, 2002. Proceedings of the IEEE 2002, 12-15 May 2002 pp.27 – 30
[129] L. Lemaitre, G. Coram, C. McAndrew, K. Kundert, "Extensions to Verilog-A to support compact device modeling", Behavioral Modeling and Simulation, 2003. BMAS 2003. Proceedings of the 2003 International Workshop on 7-8 Oct. 2003 pp.134 - 138
[130] ADMS web site: http://mot-adms.sourceforge.net/
[131] M. Schroter, "High-Frequency Circuit Design Oriented Compact Bipolar Transistor Modeling with HICUM", IEICE Transactions on Electronics 2005 E88-C(6), pp.1098-1113;
[132] MEXTRAM web site http://sourceforge.net/projects/mextram