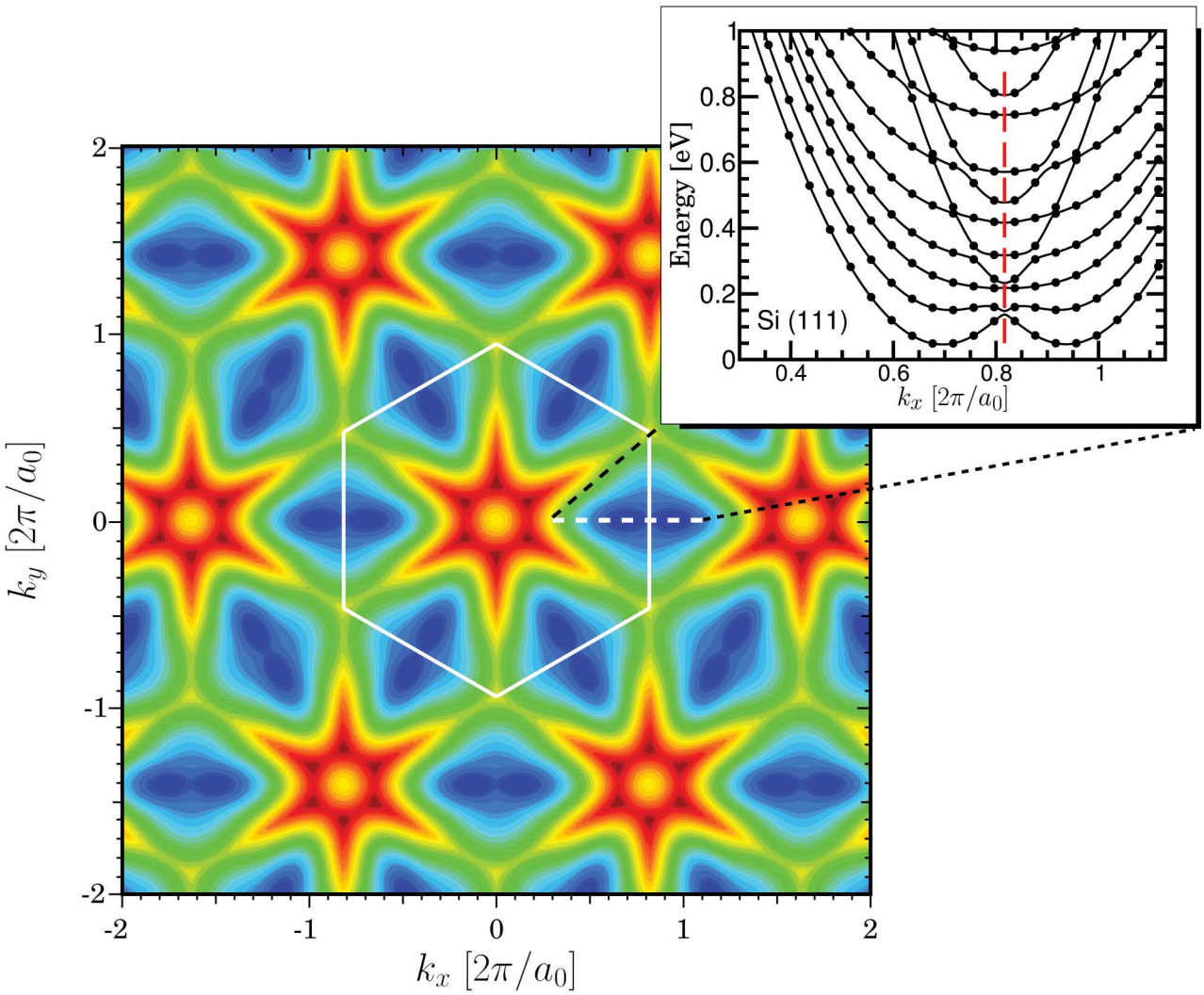
IEEE TRANSACTIONS ON

ELECTRON DEVICES

A PUBLICATION OF THE IEEE ELECTRON DEVICES SOCIETY

SEPTEMBER 2007 VOLUME 54 NUMBER 9 IETDAI (ISSN 0018-9383)

SPECIAL ISSUE ON SIMULATION AND MODELING OF NANOELECTRONICS DEVICES



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SPECIAL ISSUE ON SIMULATION AND MODELING OF NANOELECTRONICS DEVICES

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About the Cover: Two-dimensional energy to wavevector relation for a Si(111) nFET calculated with the LCBB method: The hexagon indicates the two-dimensional Brillouin zone, k_x and k_y denote the $[\bar{2}, 1, 1]$ and $[0, \bar{1}, 1]$ crystal direction, respectively.

Foreword
Special Issue on Simulation and Modeling of Nanoelectronics Devices

THIS SPECIAL Issue is devoted to research activities in the field of simulation and modeling of nanoscale electronic devices. According to the 2006 update of the International Technology Roadmap for Semiconductors (ITRS), microprocessing units with physical gate lengths of 18, 10, and 6 nm will be produced in 2010, 2015, and 2020, respectively. New device architectures will be required to reach the performance of the future technology generations that the ITRS prescribes. In addition, control of gate leakage current requires the introduction of gate insulators with high dielectric constants, and the need for increased carrier mobility pushes the use of unconventional channel materials and processing to induce appropriate stresses. Finally, in the longer term, the traditional MOSFET concept might be replaced by other structures like nanowire MOSFETs and/or carbon nanotubes (CNTs).

In order to steer the above developments, the availability of advanced models and simulation tools is of utmost importance for the following:

1) Early evaluations of the most promising device architectures and materials in terms of performance and potential for continued scaling.
2) Assessments of processing and design strategies.
3) Reductions of cycle time and of R&D costs. Measurements and tests at the nanoscale tend to be much more expensive than at the microscale and macroscale.

If models and simulation tools are to be suitable for the analysis of future-generation CMOS and post-CMOS devices, such models and tools will have to cope with important issues that are presently recognized as *difficult challenges* by the Modeling and Simulation section of the ITRS. In view of the rapid technological changes in the CMOS and "beyond CMOS" areas that involve novel device structures and materials, the aim of this Special Issue is to bring together the advances in the topic of "Simulation and Modeling of Nanoscale Devices" to a device-oriented academic and industrial community represented by the readers of the IEEE TRANSACTIONS ON ELECTRON DEVICES. This Special Issue consists of 25 carefully selected papers, 5 of which are invited and 20 of which are contributed, that discuss topics like process modeling, device modeling, and atomistic modeling, and address issues like reliability, manufacturability, and variability. The Special Issue starts with the five invited papers. In the first paper, entitled "Atomistic Simulation of Realistically Sized Nanodevices Using NEMO 3-D—Part I: Models and Benchmarks," Klimeck *et al.* discuss the essential components of the atomistic simulator called NEMO and demonstrate its successful use in the calculations of single-particle electronic states of self-assembled quantum dots, stacked quantum dot systems used in quantum cascade lasers, SiGe quantum wells for quantum computation, and SiGe nanowires. Using the nonequilibrium Green's function (NEGF) method to model nanotransistors, Anantram *et al.* review recent work in the next paper entitled "Multidimensional Modeling of Nanotransistors." After giving a motivation for the need for quantum mechanical modeling, the authors give an account of the equations and implementation for both 1-D and 2-D modeling, and illustrate examples on the use of the developed models. They highlight possible future directions in the quantum mechanical modeling of transport in nanotransistors and summarize the computational challenges. In the third paper, which is entitled "Theoretical Study of Some Physical Aspects of Electronic Transport in nMOSFETs at the 10-nm Gate-Length," Fischetti *et al.* discuss selected aspects of the physics of electronic transport in MOSFETs at the 10-nm scale, such as long-range Coulomb interactions, scattering with high-κ insulator interfacial modes, and use of a high-mobility substrate that is accompanied by the detrimental effect of a limited density of states. The fourth paper by Birner *et al.*, which is entitled "nextnano: General Purpose 3-D Simulations," presents several applications that highlight the capabilities of the Nextnano simulation software. Nextnano is a versatile software package for the simulation of nanometer-scale semiconductor quantum structures that focuses on nanostructures where quantum mechanical effects such as electronic band structures, optical matrix elements, magnetic field effects, or tunneling effects play a vital role. In the last invited paper, which is entitled "Recent Issues in Negative-Bias Temperature Instability: Initial Degradation, Field Dependence of Interface Trap Generation, Hole Trapping Effects, and Relaxation," Islam *et al.* discuss recent advances in measurement techniques, availability of new data, and refinements in the modeling approach that allow the authors to provide a systematic analysis of experimental data based on a comprehensive theoretical foundation of negative-bias temperature instability degradation.

Next, there are 20 contributed papers included in this Special Issue. The first one, which is entitled "Predictive Simulation of Advanced Nano-CMOS Devices Based on kMC Process Simulation" by Mok *et al.*, deals with process simulation. In this paper, accurate and advanced CMOS process and device simulations based on an atomistic kinetic Monte Carlo (kMC) process simulator are presented. First, the methodology used to predict continuum 2-D/3-D doping profiles from 3-D atomistic distribution that can be directly transferred from process to device simulator is described. Then, a comparison

Digital Object Identifier 10.1109/TED.2007.905342

with a wide range of electrical device characteristics shows that the experimental results were remarkably well reproduced by the simulations.

The next five papers cover new model developments with the first one by De Michielis *et al.*, which is entitled "A Semi-analytical Description of the Hole Band Structure in Inversion Layers for the Physically Based Modeling of pMOS Transistors," which presents a new semi-analytical model for the energy dispersion of holes in the inversion layer of pMOS transistors. In the next paper, which is entitled "Physics-Based Modeling of Hole Inversion Layer Mobility in Strained SiGe on Insulator," Pham *et al.* model the hole inversion layer mobility of strained SiGe on the insulator in ultrathin-body heterostructure MOSFETs by a microscopic approach that takes into account the subband structure of the 2-D hole gas and three important scattering mechanisms, i.e., optical and acoustic phonons, and surface roughness. The third paper, which is entitled "The Effect of General Strain on Band Structure and Electron Mobility of Silicon" by Ungersboeck *et al.*, presents a model that captures the effect of general strain on the electron effective masses and band edge energies of the lowest conduction band of silicon (Si). The model includes analytical expressions for the effective mass change induced by shear strain and valley shift splitting, which is obtained using a degenerate k·p-theory at the zone boundary X point. In the fourth paper, which is entitled "Modeling of Surface-Roughness Scattering in Ultrathin-Body SOI MOSFETs," Jin *et al.* present a rigorous surface roughness scattering model for ultrathin-body silicon-on-insulator (SOI) MOSFETs, which reduces to the well-known Ando's model in case of bulk MOSFETs. The last paper of this group, which is entitled "Low-Field Electron Mobility Model for Ultrathin-Body SOI and Double-Gate MOSFETs With Extremely Small Silicon Thicknesses" by Reggiani *et al.*, presents a compact model for mobility that is suited for implementation in device simulators, which accurately predicts the low-field mobility in SOI single- and double-gate MOSFETs with Si thickness down to 2.48 nm.

Next, four papers dealing with modeling approaches follow. The first paper of this group, which is entitled "A Self-Consistent Full 3-D Real-Space NEGF Simulator for Studying Nonperturbative Effects in Nano-MOSFETs" by Martinez *et al.*, presents a full 3-D real-space quantum transport simulator based on the Green's function formalism that is developed to study the nonperturbative effects in nanotransistors in the ballistic transport approximation. In the next paper, which is entitled "Scaling Behaviors of Graphene Nanoribbon FETs: A Three-Dimensional Quantum Simulation Study," Ouyang *et al.* study the scaling behavior of Graphene nanoribbon Schottky barrier FET by using the NEGF approach in an atomistic basis set self-consistently with a 3-D Poisson equation. The third paper of this group, which is entitled "On the Ability of the Particle Monte Carlo Technique to Include Quantum Effects in Nano-MOSFET Simulation" by Querlioz *et al.*, reports on the possibility to use particle-based Monte-Carlo techniques to incorporate all relevant quantum effects in the simulation of semiconductor nanotransistors. Starting from the conventional Monte-Carlo approach within the semiclassical Boltzmann approximation, the authors develop a multi-subband description of transport to include quantization in ultrathin-body devices. This technique is then extended to the particle simulation of quantum transport within the Wigner formulation. In the last paper of this group, which is entitled "Band-Structure Effects in Ultrascaled Silicon Nanowires," Gnani *et al.* investigate the effects of the full-band structure on the transport properties of ultrascaled silicon nanowire FETs operating under the quantum-ballistic limit assumption.

The final ten papers cover various applications. The first paper, which is entitled "Scaling Limits of Double-Gate and Surround-Gate Z-RAM Cells" by Butt *et al.*, evaluates the scaling limits of capacitorless single-transistor DRAM cells having surrounded gate and double-gate structures. The paper shows that the scaling is limited for both structures to the channel length of 25 nm due to the combined effects of short channel, quantum confinement of carriers in the body, and band-to-band tunneling at the source/drain to body junctions. In the next paper, which is entitled "Low-Power High-Performance Asymmetrical Double-Gate Circuits Using Back-Gate-Controlled Wide-Tunable-Range Diode Voltage," Kim *et al.* present a new power reduction scheme using a back-gate-controlled asymmetrical double-gate device for high-performance logic/SRAM power gating or variable/dynamic supply applications. Numerical mix-mode device/circuit simulations confirm that the proposed scheme can be applied for low-power high-performance circuit applications in the 65-nm technology node and beyond. In the third paper, which is entitled "Extraction of Substrate Resistance in Multifinger Bulk FinFETs Using Shorted Source/Drain Configuration" by Jung *et al.*, the substrate resistances of highly scaled bulk FinFETs are extracted by using a new RF equivalent circuit verified by 3-D device simulations. The proposed method shows frequency-independent substrate resistances in highly scaled devices and has been verified up to 50 GHz in devices operating in the saturation region. In the fourth paper, which is entitled "Empirically Verified Thermodynamic Model of Gate Capacitance and Threshold Voltage of Nanoelectronic MOS Devices With Applications to HfO_2 and ZrO_2 Gate Insulators" by Hamadeh *et al.*, a thermodynamic variational model derived from minimizing the Helmholtz free energy of the MOS device is presented. The model incorporates an anisotropic permittivity tensor and accommodates a correction for quantum mechanical charge confinement at the dielectric/substrate interface. The model is verified using empirical and TCAD capacitance–voltage data obtained on MOS devices with ZrO_2, HfO_2, and SiO_2 gate insulators. In the fifth paper by Eminente *et al.*, which is entitled "Small-Signal Analysis of Decananometer Bulk and SOI MOSFETs for Analog/Mixed-Signal and RF Applications Using the Time-Dependent Monte Carlo Approach," a state-of-the-art Monte Carlo simulator is applied to the investigation of RF performance of bulk and ultrathin-body single-gate SOI MOSFETs designed for analog and mixed-signal applications. A comparison with a standard drift diffusion approach is presented in order to discuss the main differences between the two transport models in terms of high-frequency ac analysis. In the next paper, which is entitled "An Analytic Potential-Based Model for Undoped Nanoscale Surrounding-Gate MOSFETs," He *et al.* present a complete potential-based analytic model of the

undoped nanoscale surrounding-gate MOSFETs derived from a fully self-consistent physical description between potential, charge, and current formulations. The derivation is based on the rigorous Poisson equation solution and drain current procedure equivalent to the Pao-Sah current double integral formulation. The validity of the analytic model has been verified by comparison with TCAD simulations. The seventh paper, which is entitled "A Simulation Study of the Switching times of 22- and 17-nm Gate-Length SOI nFETs on High Mobility Substrates and Si" by Laux, reports the analysis of the switching times of ultrathin-body SOI nFETs with 22- and 17-nm gate lengths, and compares the results obtained for four high-mobility substrates (Ge, GaAs, InP, and In0.53Ga0.47As) to Si. From the extrinsic device results, it is found that at a 22-nm gate length, the switching times for the considered semiconductors vary at most by a factor of 2, while at 17 nm, they vary by at most a factor of 2.5. In both cases, In0.53Ga0.47As provides the best and Si the worst switching times. In the next paper, which is entitled "Modeling of Strained CMOS on Diposable SiGe Dots: Strain Impacts on Devices' Electrical Characteristics," Fregonese *et al.* propose a novel CMOS device concept formed on a disposable SiGe dot structure, in which the degree of local strain effect on the performance of both NMOS and PMOS can be optimized by incorporating with silicon-on-nothing technology. Verified from a detailed simulation study including a dual stress liner process, the paper demonstrates a step to the next-generation CMOS performance to be taken without reducing channel lengths. In the ninth paper, which is entitled "Simulation of Ultrasubmicrometer-Gate $In_{0.52}Al_{0.48}As/In_{0.75}Ga_{0.25}As/In_{0.52}Al_{0.48}As/InP$ Pseudomorphic HEMTs Using a Full-Band Monte Carlo Simulator," Ayubi-Moak *et al.* model pseudomorphic delta-doped 0.07-μm-gate HEMTs using a full-band cellular Monte-Carlo simulator. A peak transconductance of 1679 mS/mm is extracted from simulation results, and an fT of 212 GHz is estimated from the gate capacitance, which shows excellent agreement with recent device measurements. In the next paper, which is entitled "Nonequilibrium Green's Function Treatment of Phonon Scattering in Carbon-Nanotube Transistors," Koswatta *et al.* explore the dissipative quality of quantum transport in carbon nanotube FETs. They find that the effect of phonon scattering on device performance has a bias dependence. Up to moderate gate biases device current is reduced due to elastic backscattering by acoustic phonons and low-energy radial breathing mode phonons. At large gate biases the current degradation is mainly due to high-energy optical phonon scattering. In the last paper of this Special Issue, which is entitled "Simulation of Carbon Nanotube FETs Including Hot-Phonon and Self-Heating Effects," Hasan *et al.* study the effects of nonequilibrium population of optical phonon (hot-phonon effect) and acoustic phonon (self-heating effect) on the dc performance of CNT MOSFET by solving coupled, semiclassical electron, and phonon transport equations. Full-band electron and phonon Boltzmann transport equations are solved to simulate the electron and phonon transports. The results of this paper show that the dc ballisticity of a CNT MOSFET degrades by approximately 10% due to hot-phonon effects.

The members of the IEEE Electron Device Society TCAD Technical Committee, Guest Editors for this Special Issue, would like to thank the authors for their work in submitting and revising their manuscripts. We would also wish to express our deepest gratitude to our reviewers for their efforts and dedication. This issue would not have been possible without their expert advice. The supporting work from Jo Ann Marsh of the EDS Office is also greatly appreciated.

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In 1983, 1984, and 1991, he was a Visiting Scientist at Stanford University for approximately three years. From 1985 to 2001, he was a consultant at Bell Laboratories Murray Hill, where he was a Resident Visitor for more than three years. In 1993, he was appointed Full Professor of Electronics at the University of Udine, Italy. In 2002, he joined the University of Bologna, where he is currently in charge of the nano- microelectronics group at the II School of Engineering. In 2005 he was appointed Director of IU.NET (Italian Universities Nanoelectronic Team), a Legal Consortium grouping eight University Groups. Since 2006 he is the Vice Chairman of the Scientific Community Council (SCC) of the European Technology Platform for Nanoelectronic "ENIAC." He coauthored 33 papers presented at IEDM, and overall more than 150 papers on journals and conference proceedings. His research interests include the physics, characterization, modeling, and fabrication of silicon solid-state devices and integrated circuits. In particular he has been working on several aspects of device scaling, its technological, physical, and functional limits, as well as device reliability for silicon CMOS and bipolar transistors.

Dr. Sangiorgi has been a member of the Technical Committees of several International Conferences on Electron Devices including: IEDM, ESSDERC, INFOS, and ULIS. Since 1994 he has been an Editor of the IEEE ELECTRON DEVICE LETTERS. He is a Distinguished Lecturer of the Electron Device Society, and Chairman of the Electron Device Society TCAD Technical Committee.

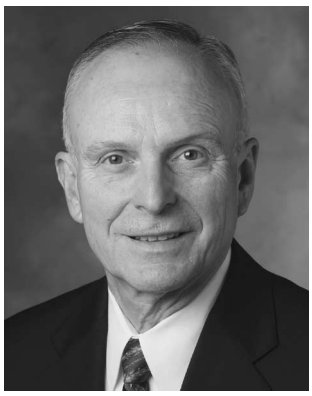
Asen Asenov (SM'03) received the M.Sc. degree in solid-state physics from Sofia University, Sofia, Bulgaria, in 1979 and the Ph.D. degree in physics from The Bulgarian Academy of Science, Sofia, in 1989.

As the leader of the Glasgow Device Modeling Group, he coordinates the development of quantum, Monte Carlo, and classical device for advanced and novel CMOS devices. He has pioneered the simulations and study of various sources of intrinsic parameter fluctuations in decanano- and nano-CMOS devices including random dopants, interface roughness, and line edge roughness. He has over 380 publications in process and device modeling and simulation, semiconductor device physics, "atomistic" effects in ultrasmall devices, and impact of variations on circuits and systems.

Herbert S. Bennett (M'72–SM'85–F'97–LF'04) received the A.B. (*magna cum laude*) and Ph.D. degrees in physics from Harvard University, Cambridge, MA, in 1958 and 1964, respectively, and the M.S. degree in physics and mathematics from University of Maryland, College Park, in 1960. He held management and research positions at the National Institute of Standards and Technology (NIST), Department of Commerce (DoC), and the National Science Foundation (NSF).

He was a DoC Science and Technology Fellow from 1971 to 1972 and was Director of the Division of Materials Research at NSF from 1978 to 1980. Currently, he is a NIST Fellow and Executive Advisor at NIST, Gaithersburg, MD. He has written over 130 archival technical publications on magnetic phase transitions in semiconductors and insulators, the Faraday effect, color centers in ionic crystals, damage mechanisms in laser materials, semiconductor device physics, optoelectronics, video technologies, and medical imaging technologies for assessing bone health. He contributes to industrial consensus-based planning for the International Technology Roadmap for Semiconductors (ITRS) in the areas of computer simulations, emerging research materials and devices, and RF semiconductors. He serves as the Technical Advisor for the U.S. National Committee Technical Advisory Group to the International Electrotechnical Commission Technical Committee TC 113 on nanotechnology standardization for electrical and electronic products and systems.

Dr. Bennett received Maryland's Outstanding Young Scientist Award for 1970 from the Maryland Academy of Sciences; Chairman of the 1994 International Conference on Numerical Modeling of Processes and Devices; elected Member of the EDS AdCom from 1995 to 2000 and serves on several of its committees; a Guest Editor for the special issue on compound semiconductors of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING in 2003; an IEEE EDS Distinguished Lecturer; and a Fellow of the American Physical Society.



Robert W. Dutton received the B.S., M.S., and Ph.D. degrees from the University of California, Berkeley, in 1966, 1967, and 1970, respectively.

He held summer staff positions with Fairchild, Bell Telephone Laboratories, Hewlett-Packard, IBM Research, and Matsushita in 1967, 1973, 1975, 1977, and 1988, respectively. He is currently a Professor of electrical engineering with Stanford University, Stanford, CA, and the Director of Research in the Center for Integrated Systems. He has published more than 200 journal articles and graduated more than four dozen doctorate students. His research interests focus on integrated circuit process, device, and circuit technologies—especially the use of computer-aided design (CAD) in device scaling and for RF applications.

Dr. Dutton was the Editor of the IEEE JOURNAL ON TECHNOLOGY IN COMPUTER AIDED DESIGN from 1984 to 1986 and was elected to the National Academy of Engineering in 1991. He was the recipient of the 1987 IEEE J. J. Ebers and 1996 Jack Morton Awards, the 1988 Guggenheim Fellowship to study in Japan, and the C&C Prize (Japan) in 2000. Most recently, he received a Career Achievement Award in 2005 from the Semiconductor Industry Association (SIA) for sustained contributions in support of research that is critical to SIA needs.

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In 2000, he was a Visiting Scientist with Bell Labs–Lucent Technologies, Murray Hill, NJ. Since 2005, he has been an Associate Professor with the University of Udine, Udine, Italy. His research contributions have included characterization techniques and modeling activities related to the hot-electron phenomena in MOSFETs and Flash memories, which touched several aspects of the performance and reliability of devices. He has also investigated thin-oxide reliability and the issue of the statistical distribution of SILC nonvolatile memories. More recently, he has been involved in the experimental characterization and modeling of low-field mobility in advanced CMOS technologies and in the semiclassical transport modeling of nanometric MOSFETs.

Dr. Esseni served as a member of the technical committee of the International Electron Devices Meeting (IEDM) in 2003 and 2004, is currently in the technical committee of the European Solid-State Device Research Conference (ESSDERC) and the International Reliability Physics (IRPS), and is a member of the Technology Computer Aided Design Committee of the Electron Devices Society (EDS).

Martin D. Giles received the Ph.D. degree from Stanford University, Stanford, CA, in 1984.

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Masami Hane received the Ph.D. degree from Keio University, Yokohama, Japan, in 2003.

In 1987, he was with the Microelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan. From 1993 to 1994, he was a Visiting Scholar with the Center for Integrated Systems, Stanford University, Stanford, CA. From 1996 to 1999, he was a SELETE 3D-TCAD project member in Japan. Since joining NEC Corporation, Sagamihara, Japan, he has been engaged in ULSI process/device modeling and scaled CMOS technology research and development. He is currently a Principal Researcher in the Device Platforms Research Laboratories, NEC Corporation.

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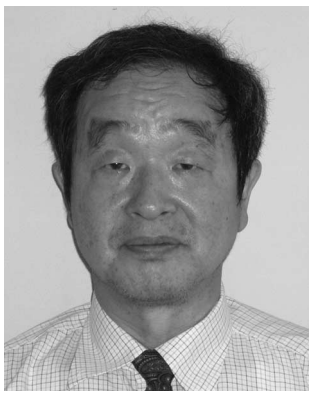
From 1990 to 1995, he was a Research and Teaching Assistant with the "Institut für Theoretische Elektrotechnik," RWTH Aachen. From 1995 to 1997, he was with the Research and Development Facility, Fujitsu Limited, Kawasaki, Japan. From 1997 to 2002, he was a Chief Engineer with the "Institut für Theoretische Elektrotechnik und Mikroelektronik," University of Bremen. From 2002 to 2003, he spent a one-year sabbatical with the Center for Integrated Systems, Stanford University. From 2003 to 2006, he was a Research Associate with the Technical University of Braunschweig, Braunschweig, Germany. Since 2006, he has been a Full Professor of microelectronics with Bundeswehr University, Munich, Germany. His main research interests are full-band Monte-Carlo simulation of Si and SiGe devices, numerical device modeling, transport in inversion layers, and noise modeling.

Prof. Jungemann is a member of the Board of Editors of the IEEE TRANSACTIONS ON ELECTRON DEVICES and has served on the technical program committees of the International Workshop on Computational Electronics (IWCE), the International Electron Devices Meeting (IEDM), and the International Conference on Computer-Aided Design (ICCAD). He was the corecipient of the IEEE EDS Paul Rappaport Award in 2005.



Kenji Nishi (F'01) received the B.Eng. and Ph.D. degrees from Tokyo University, Tokyo, Japan, in 1973 and 1988, respectively, both in applied physics.

From 1973 to 2003, he was with OKI Electric Industry Company, Tokyo, Japan, where he was first engaged in logic simulation and then in process/device development of bipolar devices. In 1979, he started his career in semiconductor process simulation. From 1982 to 1984, he was a Visiting Scientist with the Massachusetts Institute of Technology (MIT), Cambridge. As he was promoted to Manager in the 1990s, his work extended from semiconductor simulation to logic device development, semiconductor characterization, and reliability enhancement. In 1999, he was the project leader of a 3-D simulation system development called ENEXSS with major Japanese semiconductor companies. Since 2003, he has been with Kinki University Technical College, Mie, Japan, where he currently is a Professor and a Senior Vice-President. He coauthored more than 160 books, technical journals, and conference proceedings. He also is the holder of several patents.

Dr. Nishi served as a Technical Committee Member of the International Electron Devices Meeting (IEDM), the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), and the Asia and South Pacific Design Automation Conference (ASP-DAC), including program chair of SISPAD99. He currently serves as a peer-reviewer for New Energy Development Organization (NEDO).

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the "Diplomingenieur" degree in electrical engineering and the Doctoral degree in technical sciences from "Technische Universität Wien," Wien, Austria, in 1978 and 1981, respectively.

Since 1984, he has been holding the "venia docendi" on computer-aided design. Since 1988, he has been the Chair Professor of the "Institut für Mikroelektronik." From 1998 to 2005, he was the Dean of the "Fakultät für Elektrotechnik und Informationstechnik." His current research interests are modeling and simulation of problems for microelectronics engineering.

Shinichi Takagi (M'93) was born in Tokyo, Japan, on August 25, 1959. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1982, 1984, and 1987, respectively. His Ph.D. thesis involved the study on the surface carrier transport in MISFETs based on III–V semiconductors.

He was with the Toshiba Research and Development Center, Kawasaki, Japan, in 1987, where he has been engaged in the research on the device physics of Si MOSFETs, including the carrier transport in the inversion layer, the impact ionization phenomena, the hot carrier degradation, and the electric properties of Si/SiO_2 interface. From 1993 to 1995, he was a Visiting Scholar with Stanford University, Stanford, CA, where he studied the Si/SiGe heterostructure devices. Since returning to the Ultralarge-Scale Integration Research Laboratories, he was also engaged in the physics and technology of the reliability of SiO_2, ferroelectric devices, and strained-Si MOS devices. Since 2001, he has been working for the MIRAI Project, as the leader of Ultra-High Performance New Transistor Structures Theme. In October 2003, he moved to the University of Tokyo, where he is currently working as a Professor in the Department of Electronic Engineering, School of Engineering. His recent interests include the science and the technologies of advanced CMOS devices using new channel materials such as strained Si, Ge, and III–Vs.

Dr. Takagi served on the technical program committee on several international conferences, including International Electron Device Meeting, International Reliability Physics Symposium, International Conference on Solid State Device, and Materials and International Solid State Circuits Conference. He received five awards, 18th IBM Japan Science Award (2004), International Solid State Circuits Conference Takuo Sugano Outstanding Paper Award (2004), 2003 Electron Devices Society George E. Smith Award, International Conference on Solid State Devices and Materials Paper Award (2002), and International Reliability Physics Symposium Outstanding Paper Award (1998). He is a member of the IEEE Electron Device Society and the Japan Society of Applied Physics.