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Geometry optimization for carbon nanotube transistors

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Abstract

The performance of carbon nanotube-based transistors is analyzed numerically, employing the non-equilibrium Green's function formalism. The effect of geometrical parameters on the device performance is investigated. Our results clearly show that device characteristics can be optimized by appropriately selecting geometrical parameters.

1. Introduction

A carbon nanotube (CNT) can be viewed as a rolled-up sheet of graphene with a diameter of a few nano-meters. The way the graphene sheet is wrapped is represented by a pair of indices (n,m) called the chiral vector. The integers n and m denote the number of basis vectors along two directions in the honeycomb crystal lattice of graphene. The CNT is called zigzag, if $m = 0$, armchair, if $n = m$, and chiral otherwise. CNTs with $n - m = 3$ are metals, otherwise they are semiconductors [1]. Semiconducting CNTs can be used as channels for transistors [2] which have been studied in recent years as potential alternatives to CMOS devices because of their capability of ballistic transport.

Depending on the work function difference between the metal contact and the CNT, carriers at the metal–CNT interface encounter different barrier heights. The latter is defined as the potential barrier which is faced by carriers at the Fermi level in the metal, see Fig. 1. Fabrication of devices with positive (Schottky type) [3] and zero (Ohmic) [4] barrier heights for holes have been reported. In a device with zero barrier height, carriers with energies above the metal Fermi level can reach the channel by thermionic emission, those with lower energies have to tunnel to reach the channel. In this work we consider devices with different barrier heights for electrons. Since the dispersion relations for electrons and holes are symmetric, our discussions are valid for holes as well. We employed the non-equilibrium Green's function (NEGF) formalism to perform a comprehensive numerical study of CNT transistors.

The outline of the paper is as follows. In Section 2, our approach is briefly described. Assuming ballistic transport, the influence of geometrical parameters on the device response is studied in Section 3. Methods for optimizing the device performance are presented in Section 4. After a brief discussion in Section 5, conclusions are drawn in Section 6.

2. Simulation approach

Due to quantum confinement along the tube circumference, carrier have bound wave functions around the CNT and can propagate along the tube axis. Under the assumption that the potential profile does not vary sharply along the circumference of the CNT, sub-bands will be decoupled [5]. In this work we assume bias conditions for which the first sub-band contributes mostly to the total current. In the mode-space approach the transport equation for each sub-band can be written as [6]

$$G^{\mathrm{R,A}}_{\mathrm{r,r'}}(E) = [EI - H_{\mathrm{r,r'}}(E) - \Sigma^{\mathrm{R,A}}_{\mathrm{r,r'}}(E)]^{-1}, \quad (1)$$

$$G^{<,>}_{\mathrm{r,r'}}(E) = G^{\mathrm{R}}_{\mathrm{r,r'}}(E)\Sigma^{<,>}_{\mathrm{r,r'}}(E)G^{\mathrm{A}}_{\mathrm{r,r'}}(E). \quad (2)$$

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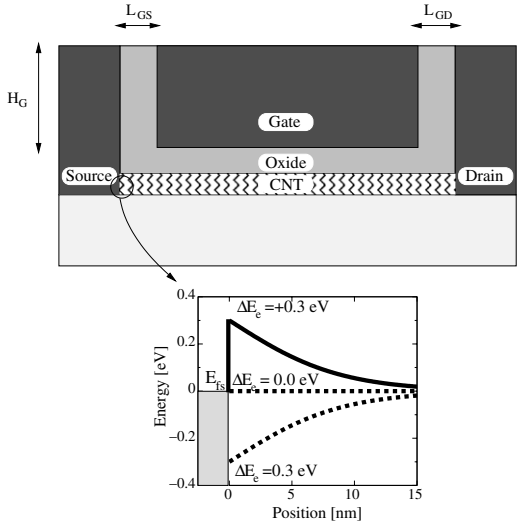

Fig. 1. Cross-section of the investigated CNT based transistor and the band-edge profile at the source-sided metal–CNT interface. Depending on the work function difference between metal and CNT, a positive, zero, or negative barrier height for electrons or holes can be achieved. In this work we assume electrons as majority carriers. Due to the symmetric band structure, the conclusions also hold for holes. $T_{\mathrm{Ins}} = 2$ nm, $H_{\mathrm{G}} = 40$ nm, and $\epsilon_{\mathrm{r}} = 15$.

In (1) an effective mass Hamiltonian was assumed. All our calculations assume a CNT with a band gap of $E_{\mathrm{g}} = 0.6$ eV corresponding to a CNT with a diameter of $d_{\mathrm{CNT}} = 1.6$ nm, and $m^* = 0.05\, m_0$ for both electrons and holes. A recursive Green's function method is used for solving (1) and (2) [7]. The total self-energy in (1) consists of the self-energies due to the source contact, drain contact, and electron–phonon interaction, $\Sigma = \Sigma_{\mathrm{S}} + \Sigma_{\mathrm{D}} + \Sigma_{\mathrm{el-ph}}$. The self-energy due to electron–phonon interaction consists of the contribution of elastic and inelastic scattering mechanisms, $\Sigma_{\mathrm{e-ph}} = \Sigma_{\mathrm{el}} + \Sigma_{\mathrm{inel}}$. Assuming a single sub-band the electron–phonon self-energies are simplified to (3)–(5).

$$\Sigma^{<,>}_{\mathrm{el},(\mathrm{r,r})}(E) = D_{\mathrm{el}} G^{<,>}_{\mathrm{r,r}}(E), \tag{3}$$

$$\Sigma^{<}_{\mathrm{inel},(\mathrm{r,r})}(E) = \sum_{v} D^{v}_{\mathrm{inel}}[(n_{\mathrm{B}}(\hbar\omega_v)+1)G^{<}_{\mathrm{r,r}}(E+\hbar\omega_v) + n_{\mathrm{B}}(\hbar\omega_v)G^{<}_{\mathrm{r,r}}(E-\hbar\omega_v)], \tag{4}$$

$$\Sigma^{>}_{\mathrm{inel},(\mathrm{r,r})}(E) = \sum_{v} D^{v}_{\mathrm{inel}}[(n_{\mathrm{B}}(\hbar\omega_v)+1)G^{>}_{\mathrm{r,r}}(E-\hbar\omega_v) + n_{\mathrm{B}}(\hbar\omega_v)G^{>}_{\mathrm{r,r}}(E+\hbar\omega_v)], \tag{5}$$

where v is the phonon branch, D is the electron–phonon coupling coefficient, $\hbar\omega$ is the phonon energy, and n_{B} is the phonon occupation number which is given by the Bose–Einstein distribution function. The imaginary and real parts of the self-energy broadens and shifts the density of states, respectively. The imaginary part of the retarded self-energy is given by $\Im m[\Sigma^{\mathrm{R}}(E)] = [\Sigma^{>} - \Sigma^{<}]/2i$ while the real part is given by the Hilbert transform of the imaginary part. The transport equations are iterated to achieve convergence of the electron–phonon self-energies, resulting in a self-consistent Born approximation.

Phonons with $|\mathbf{q}| \approx 0$ are referred to as Γ-point phonons, and can belong to the twisting acoustic (TW), the longitudinal acoustic (LA), the radial breathing mode (RBM), the out-of-phase out-of-plane optical branch (ZO), the transverse optical (TO), or the longitudinal optical (LO) phonon branch. Phonons inducing inter-valley transitions have a wave-vector of $|\mathbf{q}| \approx q_{\mathrm{K}}$, where q_{K} corresponds to the wave-vector of the K-point of the Brillouin zone of graphene. K-point phonons, also referred to as zone boundary phonons, are a mixture of fundamental polarizations.

2.1. Numerical implementation

The coupled system of transport and Poisson equations were solved numerically. To solve transport equations numerically, they need to be discretized in both the spatial and the energy domain. Uniform spatial grids with a spacing of 1 Å have been employed. The carrier concentration at some node l and the current density between the node l and $l+1$ of the device are given by

$$n_l = -4i \int \frac{\mathrm{d}E}{2\pi} G^{<}_{l,l}(E), \tag{6}$$

$$j_{l,l+1} = \frac{4q}{\hbar} \int \frac{\mathrm{d}E}{2\pi} 2\Re e\{G^{<}_{l,l+1}(E) t_{l+1,l}\}, \tag{7}$$

where the factor 4 is due to the spin and band degeneracy. In the Poisson equation, carriers are treated as a sheet charge distributed over the surface of the CNT [8]. The energy grid, however, should be non-uniform, since an adaptive integration method is generally required to evaluate quantities such as (6) with sufficient accuracy.

The coupled system of the transport and Poisson equations has to be solved self-consistently [9]. The convergence of the self-consistent iteration is a critical issue. To achieve convergence, fine resonances at some energies in (6) have to be resolved accurately [8,10]. For that purpose an adaptive method for selecting the energy grid is essential [10].

3. The effect of geometrical parameters on the device response

In this section the effect of scaling of the gate-source and gate-drain spacer lengths on the device response is studied. Results for devices with different barrier heights at the metal–CNT interface are discussed.

3.1. Gate-source spacer length

Electrons with energies lower than the barrier height have to tunnel through the source-sided metal–CNT interface barrier to reach the channel, whereas electrons with

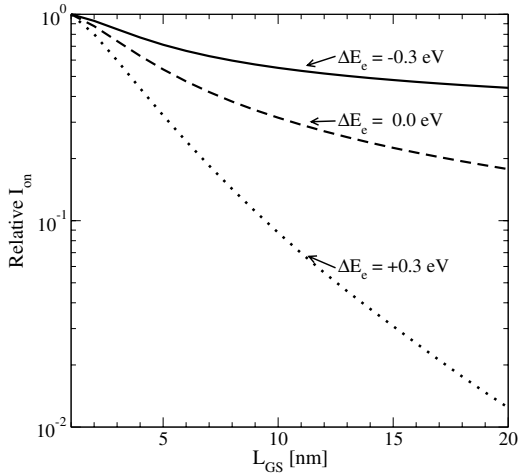

Fig. 2. The relative variation of the on-current versus the gate-source spacer length (L_{GS}) for devices with different barrier heights for electrons. In a device with negative barrier height the tunneling current has a smaller contribution to the total current as compared to other device types. Therefore, the current is less sensitive to the variation of the gate-source spacer length.

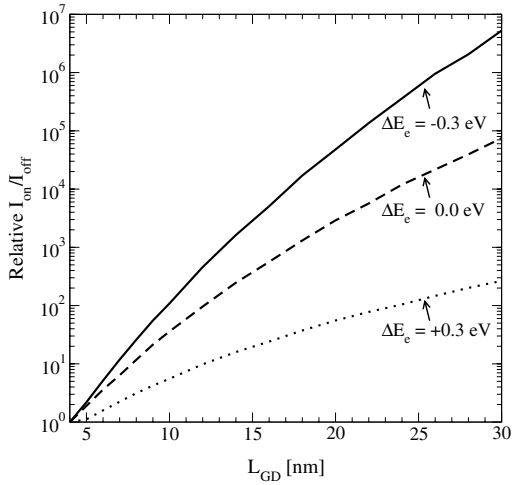

Fig. 3. The ratio I_{on}/I_{off} versus the gate-drain spacer length (L_{GD}) for devices with different barrier heights for electrons. Increasing the gate-drain spacer length improves the I_{on}/I_{off} ratio for all devices. The device with negative barrier height shows the biggest improvement. In a device with negative barrier height for electrons the barrier height for holes is positive. In this case the hole current is more sensitive to the variation of the gate-drain spacer length than it is for other device types. For all results $V_D = 0.6$ V was assumed.

higher energies are injected by thermionic emission. Both the tunneling current and the thermionic emission current contribute to the total current. In general the relative contributions of the thermionic current and the tunneling current strongly depend on the barrier height and the barrier width. The thermionic emission current is controlled by the barrier height and is virtually independent of the barrier width. On the other hand, the tunneling current decreases exponentially with the barrier width. Fig. 2 shows the relative variation of the on-current versus the gate-source spacer length. In a device with negative barrier height the tunneling current has a smaller contribution to the total current as compared to devices with non-negative barrier height. Therefore, it is less sensitive to the variation of the gate-source spacer length.

3.2. Gate-drain spacer length

In the off-regime a considerable drain current can appear due to ambipolar conduction. With increasing drain bias this phenomenon becomes more apparent [11]. If the drain voltage of an *n*-channel device becomes higher than the gate voltage, the thickness of the drain-sided metal–CNT barrier for holes is reduced. As a result, the parasitic band-to-band tunneling current of holes increases [12]. By increasing the gate-drain spacer length, the band-edge profile near the drain contact is less affected by the gate voltage. Therefore, the barrier for holes at the drain-side is thicker and the parasitic tunneling current of holes is suppressed [13]. Fig. 3 compares the increase of the I_{on}/I_{off} ratio as a function of the gate-drain spacer length. In a device with negative barrier height a higher improvement is achieved. A smaller barrier height for electrons results in a larger barrier height for holes. A negative barrier height for electrons gives a positive barrier height for holes, implying that the tunneling process contributes predominantly the hole current. As a result, for a device with negative barrier height for electrons the parasitic hole tunneling current can be more effectively suppressed than for other device types.

Fig. 4 compares the effect of the gate-drain spacer length on the output characteristics for devices with different barrier heights. In the device with positive barrier height for electrons, the current at low drain biases decreases as the gate-drain spacer length increases. In a device with positive barrier height, electrons in the channel face a barrier at the drain-sided metal–CNT interface [13]. Similar to what we discussed for the gate-source spacer length, with increasing gate-drain spacer length the thickness of the drain-sided metal–CNT barrier increases, such that the drain current will be reduced. If the drain voltage becomes higher than the gate voltage, most of the electrons can reach the drain contact by thermionic emission. In devices with negative and zero barrier height this problem does not occur, since even at low drain voltages a drain-side barrier does not form.

It should be noticed that, as opposed to conventional MOSFETs, increasing the length of the un-gated area determined by the gate-drain spacer does not increase the channel resistance. In conventional MOSFETs the resistivity of the channel is modulated when the gate voltage attracts or repels carriers from the channel. For an enhancement-type device the resistance of the un-gated region is high. In contrast, the intrinsic conductance of CNTs is independent from the gate voltage.

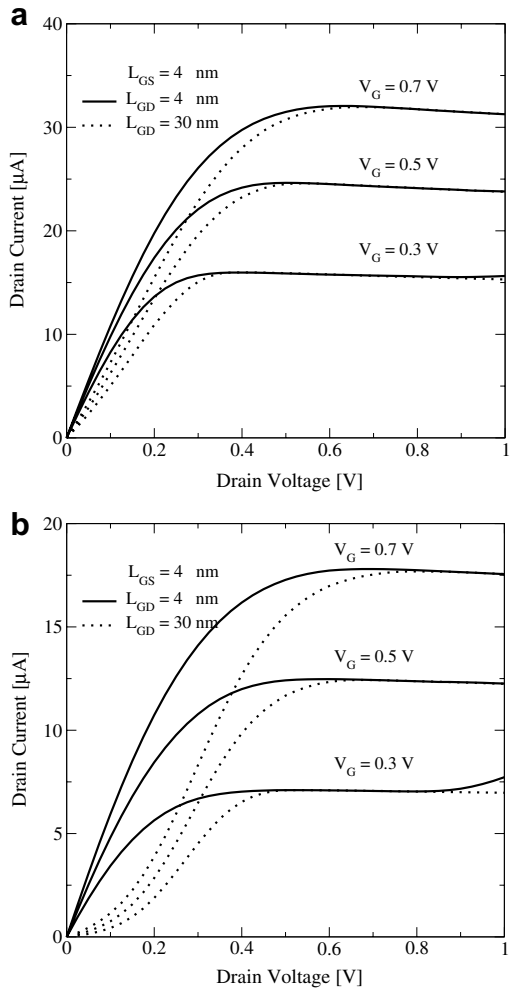

Fig. 4. The effect of the gate-drain spacer length (L_{GD}) on the output characteristics for a device with (a) zero ($\Delta E_e = 0$) and (b) positive barrier height ($\Delta E_e = 0.3$ eV) for electrons. The results indicate that the un-gated region does not increase the channel resistance. The decrease of the current at low biases for a device with positive barrier height is due to the barrier formed at the drain-sided metal–CNT interface.

4. Performance optimization

The gate delay time with respect to the I_{on}/I_{off} ratio can be used to compare devices with different geometries and material properties [14]. The gate delay time defined as

$$\tau = \frac{C_G V_{DD}}{I_{on}}. \tag{8}$$

Here, $C_G = C_{GS} + C_{GD} + C_{GG}$ with ${C_{GG}}^{-1} = {C_{Ins}}^{-1} + {C_Q}^{-1}$. The quantum capacitance is given by $C_Q = 8q^2/h\nu_F \approx 400$ aF/μm, including the twofold band and spin degeneracy [15,16]. The insulator capacitance, occurring between the tube and the planer gate contact, is given by [17]

$$C_{Ins} = \frac{2\pi\kappa\epsilon_0}{\operatorname{arcosh}(T_{Ins}/R_{CNT} + 1)}. \tag{9}$$

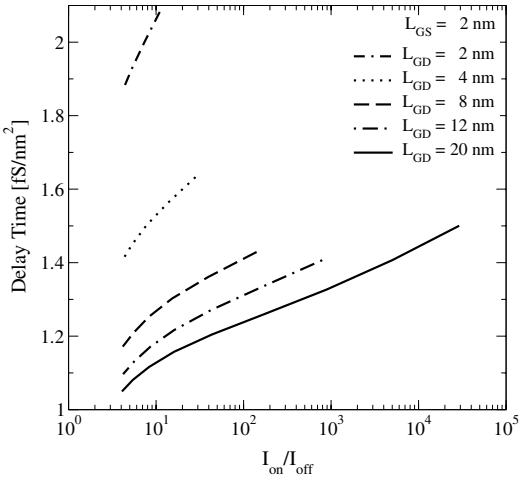

Fig. 5. The effect of L_D on the gate delay time versus the I_{on}/I_{off} ratio for a device with zero barrier height for electrons ($\Delta E_e = 0$). $L_{GS} = 2$ nm and $V_{DD} = 0.8$ V.

For the geometry parameters given in Fig. 1, $C_{Ins} \approx 400$ aF/μm. For a device with 50 nm channel length $C_{GG} \approx 10$ aF. Since this value is very small, the total capacitance is dominated by the parasitic capacitances [18]. The gate-source and gate-drain parasitic capacitances were estimated by the capacitance of two parallel plates[1], $C_{GS,GD} = \kappa\epsilon_0 A/L_{GS,GD}$, (see Fig. 1)

$$C_G \approx C_{GS} + C_{GD} = \kappa\epsilon_0 A\left(\frac{1}{L_{GS}} + \frac{1}{L_{GD}}\right). \tag{10}$$

For a better comparison, throughout this work the results are normalized to the area of the parasitic capacitances (A). In Section 3 it was shown that by increasing the gate-drain spacer length the I_{on}/I_{off} ratio increases. At the same time, by increasing the gate-drain spacer length the parasitic capacitance between these two contacts decreases, which reduces the gate delay time. Fig. 5 shows the effect of the gate-drain spacer length on the gate delay time versus the I_{on}/I_{off} ratio, which shows a significant performance improvement by increasing the gate-drain spacer length.

When increasing the gate-source spacer length, the parasitic capacitance between these two contacts reduces, and so does the on-current. The band-edge profile near the source contact plays an important role in controlling the total current. Increasing the gate-source spacer length reduces the gate control of the band-edge profile near the source contact.

Since the gate delay time is proportional to the parasitic capacitance and inversely proportional to the on-current (8), there is an optimal value for the gate-source spacer length, L_{GS0}, which minimizes the gate delay time. The

[1] This approximation is valid for most cases, however, for larger spacer lengths this relation should be modified. For accurate analysis, one can numerically calculate the parasitic capacitance as a function of the spacer length and replace it in (10). This does not affect the generality of our methodology.

optimal value for the gate-source spacer length is achieved when

$$\left.\frac{\partial \tau}{\partial L_{GS}}\right|_{L_{GS0}} = \frac{1}{C_G}\left.\frac{\partial C_G}{\partial L_{GS}}\right|_{L_{GS0}} - \frac{1}{I_{on}}\left.\frac{\partial I_{on}}{\partial L_{GS}}\right|_{L_{GS0}} = 0. \quad (11)$$

Considering the expression derived for C_G in (10), we have

$$\frac{1}{C_G}\frac{\partial C_G}{\partial L_{GS}} = \frac{-1}{L_{GS}(1 + L_{GS}/L_{GD})}. \quad (12)$$

Fig. 6 shows the sensitivity of the on-current to the gate-source spacer length for devices with zero and positive barrier heights for electrons. However, for a device with zero barrier height for electrons the mentioned sensitivity is not zero. Since at positive gate biases the conduction band-edge is pushed below the source Fermi level, even in devices with zero barrier height the tunneling current can contribute to the total current. For thinner insulators the width of the source-sided barrier decreases, resulting in a higher tunneling current contribution to the total current and a higher sensitivity of the on-current to L_{GS}.

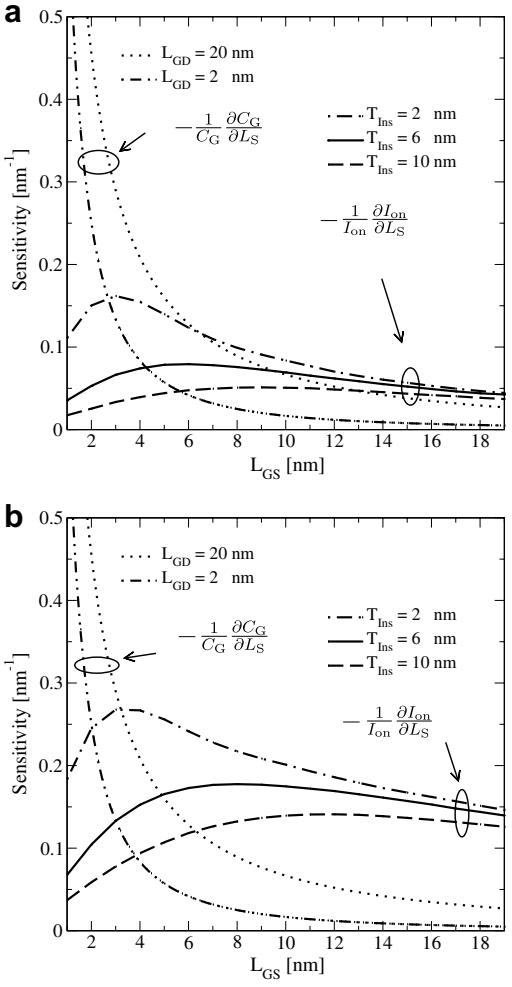

Fig. 6. The sensitivity of the parasitic capacitance and the on-current to L_{GS} for a device with (a) zero barrier height ($\Delta E_e = 0$) and (b) positive barrier height ($\Delta E_e = 0.3$ eV) for electrons. The intersection of the curves gives the optimum L_{GS0} which minimizes τ.

The optimal gate-source spacer length for a device with zero barrier height for electrons is $L_{GS} \approx 6$ nm for $T_{Ins} = 2$ nm and $L_{GD} = 20$ nm. For devices with positive barrier heights the the optimal value of the gate-source spacer length is smaller than that of a device with zero barrier height due to higher sensitivity of the on-current with respect to the gate-source spacer length. Note that the optimal value for L_{GS} depends on L_{GD}. For small values of L_{GD} the gate-drain parasitic capacitance dominates the gate-source parasitic capacitance, therefore any further decrease of the gate-source spacer length does not improve the gate delay time. As shown in Fig. 7, the optimal value of the gate-source spacer length for the given material and geometrical parameters results in optimized device characteristics.

5. Discussion

In general the electron–phonon interaction parameters depend on the diameter and the chirality of the CNT. The calculation of these parameters is presented in [19,20]. The band gap of a semiconducting CNT is inversely proportional to the diameter. A rough estimate is $E_G = 0.8$ eV nm/d_{CNT} nm. CNTs with a diameter $d_{CNT} > 2$ nm have a band gap $E_G < 0.4$ eV, which render them unsuitable as channel for transistors. Since the fabrication of devices with a diameter $d_{CNT} < 1$ nm is very difficult, we limit our study to zigzag CNTs with diameters in the range $d_{CNT} = 1$–2 nm.

Acoustic phonons scattering is treated as an elastic process. Inelastic scattering is induced by OP, RBM, and K-point phonons. Considering the class of CNTs discussed above, the energies of the these phonons are $\hbar\omega_{OP} \approx 200$ meV, $\hbar\omega_{RBM} \approx 30$ meV, and $\hbar\omega_{K-1} \approx 160$ meV, and $\hbar\omega_{K-2} \approx 180$ meV [21,22]. The corresponding coupling coefficients are $D_{inel}^{OP} \approx 40 \times 10^{-3}$ eV^2, $D_{inel}^{RBM} \approx 10^{-3}$ eV^2, and $D_{K-1} \approx 10^{-4}$ eV^2, and $D_{K-2} \approx 50 \times 10^{-3}$ eV^2 [19,22].

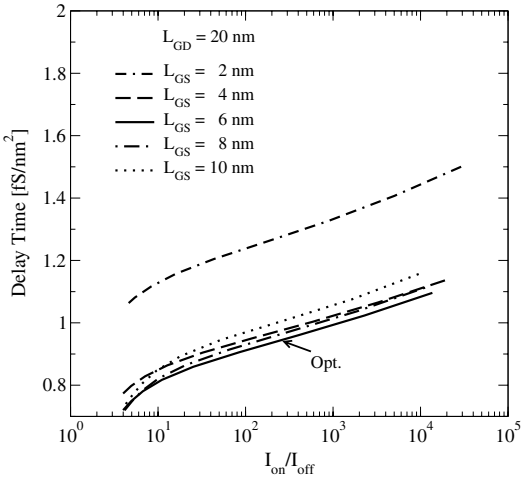

Fig. 7. The effect of L_{GS} on the gate delay time versus the I_{on}/I_{off} ratio for a device with zero barrier height for electrons ($\Delta E_e = 0$). $V_{DD} = 0.8$ V. The optimal L_{GS} for both device types are shown.

As discussed in [22], high energy phonons, such as OP and K-point phonons, reduce the on-current only weakly. Low energy phonons, such as the RBM phonon, can reduce the on-current more effectively. However, due to weak coupling, the RBM mode has a negligible effect at room temperature. The electron–phonon coupling is also weak for acoustic phonons ($D_{\mathrm{el}}^{\mathrm{AP}} < 10^{-3}\ \mathrm{eV}^2$), which implies that elastic back-scattering of carriers is weak. Therefore, the on-current of short CNT based transistors can be close to the ballistic limit [23].

Electron–phonon interaction reduces the on-current, both, directly and indirectly [24,25]. The direct effect is due to back-scattering of carriers, but scattering also redistributes the carrier concentration profile along the device. This redistribution affects the band-edge profile so that it reduces the total current. To reduce the indirect effect one should increase the gate-CNT coupling. If thin high-κ insulators are used then $C_{\mathrm{Ins}} \gg C_{\mathrm{Q}}$ and $C_{\mathrm{GG}} \approx C_{Q}$, implying that the potential on the tube becomes equal to that of the gate (perfect coupling). This regime is called quantum capacitance limit in which the device is potential-controlled rather than charge-controlled [26]. Fig. 8 compares the ratio of the current in the presence of scattering to the current in the ballistic limit for different insulators. For the given material and geometrical parameters a value of $\kappa > 20$ maximizes the performance of the device. But, when using high-κ materials not only the on-current but also the parasitic capacitances increase. Therefore, there is a κ which optimizes the gate delay time. It can be shown that the optimized value is achieved when $\frac{1}{C_{\mathrm{G}}}\frac{\partial C_{\mathrm{G}}}{\partial \kappa}\big|_{\kappa_0} = \frac{1}{I_{\mathrm{on}}}\frac{\partial I_{\mathrm{on}}}{\partial \kappa}\big|_{\kappa_0}$. Considering the expression derived for C_{G} in (10), we have $\frac{1}{C_{\mathrm{G}}}\frac{\partial C_{\mathrm{G}}}{\partial \kappa} = \frac{1}{\kappa}$. Fig. 9 shows the sensitivity of the on-current and parasitic capacitances to κ. Since the curves do not intersect at high values of κ, lower values minimizes τ. Therefore, there is a trade-off between the gate delay time and the on-current. For a specific application this parameter can be optimized.

For optimizing the device performance, it is assumed that the total capacitance is dominated by the parasitic capacitances [18], see Section 4. If the quantum capacitance dominates the total capacitance, by increasing the gate-source spacer length the total capacitance is not decreased, whereas the the on-current decreases. Therefore, the minimum possible value of the gate-source spacer length optimizes the device performance, but a large value of the gate-drain spacer length can be used to suppress the ambipolar conduction and increasing the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio.

Depending on the barrier height for electrons at the metal–CNT interface different optimized values for the spacer lengths can be achieved. Optimized values for the gate-source spacer length L_{GS} are mostly in the range 1–10 nm, while much larger values can be selected for the gate-drain spacer length, such as $L_{\mathrm{GD}} = 20$ nm. However, the gate-drain spacer length should not reduce the gate length too much, to avoid short-channel effects. For the investigated devices a minimum gate length of 20 nm is required.

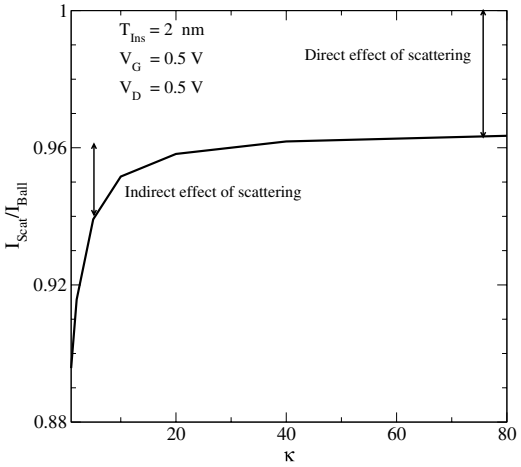

Fig. 8. The ratio of the drain current in the presence of scattering to the ballistic limit for different κ. The fractions due to the direct and the indirect effects of scattering on the on-current are shown. For a high-κ insulator the indirect part reduces.

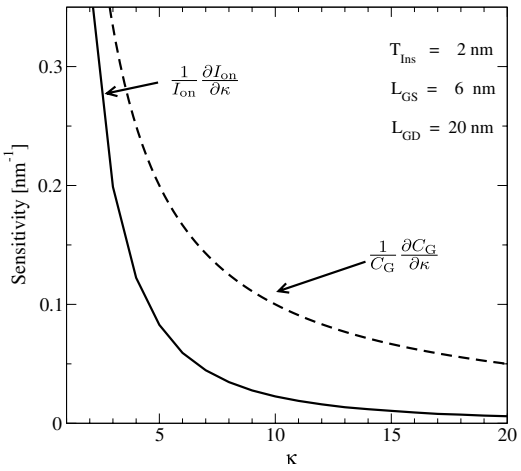

Fig. 9. The sensitivity of the parasitic capacitance and the on-current to κ. Since the curves do not intersect at high values of κ, lower values of κ minimizes τ.

6. Conclusion

We showed that the device characteristics can be optimized by appropriately selecting the geometrical parameters. With increasing the gate-drain spacer, the off-current and the gate-drain parasitic capacitance reduce at the expense of a drain current reduction at low bias voltages. With increasing gate-source spacer length, the drain current and gate-source parasitic capacitance decrease. Since the gate delay time is proportional to the parasitic capacitances and inversely proportional to the on-current, there is a value for the gate-source spacer length which minimizes the gate delay time. The optimal point is where the sensitivity of these quantities are equal. As the barrier height at the metal–CNT reduces, the contribution of thermionic emission to the total current increases and the sensitivity of the on-current with respect to the gate-source spacer length

reduces, which results in larger gate-source spacer lengths for optimized performance. This method can be employed for optimizing the performance of an array of CNTs [18].

Acknowledgments

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