Level Shifts and Gate Interfaces as Vital Ingredients in Modeling of Charge Trapping

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***Abstract*—We present a detailed modeling study of charging and discharging traps in dielectrics used in modern semiconductor devices. Existing descriptions of charge trapping are often restricted to charge injection from the substrate and ignore the presence of the gate contact as a source/sink of charge carriers. This assumption loses its justification when the gate dielectric shrinks into the nanometer range. Furthermore, a novel picture of tunneling into and out of defects has emerged from first principles calculations which questions the conventional concept of fixed trap levels irrespective of their charge state. Consequently, focus is put on the development of a novel rigorous model merging both effects into one general description of charge trapping.**

I. Introduction

Advances in microelectronics have led to aggressive scaling of device geometries, which makes trapping of charge carriers more relevant for reliability issues. Tewksbury's model [1, 2] appears to be well established in this context. However, as modern semiconductor devices feature increasingly smaller gate dielectric thicknesses, charge carrier injection from the gate gains relevance [3]. Therefore Tewksbury's model needs to be extended to charge trapping from the gate contact, which strongly alters the temporal long term charge trapping behavior.

Recently, a series of first principles calculations [4–6] has revealed a new aspect of charge trapping, namely the level shift [7–9]. Since defect levels cannot be regarded independently from their charge state, the energy levels for trapping and detrapping do not necessarily need to coincide. Paying respect to this level shift, a completely different trapping behavior is observed.

II. Modeling

In this section, a brief overview of the models examined throughout this work is provided. The present approach to charge trapping relies on the work of Tewksbury [1]. This description of charge trapping, which will be referred to as the *fixed level model*, assumes a rate equation for the tunneling processes:

$$\begin{aligned}\partial_t f_\mathrm{t}(E_\mathrm{t},x) = &+ n(E_\mathrm{t})\; r_\mathrm{in}(E_\mathrm{t},x)\; (1-f_\mathrm{t}(E_\mathrm{t},x))\\ &- p(E_\mathrm{t})\; r_\mathrm{out}(E_\mathrm{t},x)\; f_\mathrm{t}(E_\mathrm{t},x)\end{aligned} \tag{1}$$

where n or p denote the number of occupied or empty states at the substrate interface and f_t stands for the occupancy of the traps located within the dielectric. Note that all quantities are evaluated at the same trap energy E_t. The first term of the right hand side of equation (1) corresponds to trapping of e^-, while the second term represents e^- detrapping or h^+ trapping, respectively. A derivation of the rates r_in and r_out based on Fermi's golden rule [1] yields a WKB coefficient multiplied with a prefactor ν_0.

$$\begin{aligned}r_\mathrm{in/out} &= \nu_0 \exp\big(-2\int_{x_\mathrm{if}}^{x_\mathrm{t}} kx\,\mathrm{d}x\big)\\ k^2 &= \frac{2m}{\hbar^2}(E_\mathrm{c/v}-E)\,,\end{aligned} \tag{2}$$

where x_t and x_if are the position of the trap or the interface, respectively. $E_\mathrm{c/v}$ stands for the conduction or the valence band edge, respectively. Interface states may also be included in $n(E)$ and $p(E)$ but have to be specified by different prefactors due to their distinct nature compared to band states [1].

We extend this approach (*extended fixed level model*) to account for charge carrier injection from the gate contact by adding the respective trapping and detrapping rates (1), see Fig. 1.

$$\begin{aligned}\partial_t f_\mathrm{t}(E_\mathrm{t},x) = &+ n_\mathrm{s}(E_\mathrm{t})\; r_\mathrm{in}(E_\mathrm{t},x)\; (1-f_\mathrm{t}(E_\mathrm{t},x))\\ &- p_\mathrm{s}(E_\mathrm{t})\; r_\mathrm{out}(E_\mathrm{t},x)\; f_\mathrm{t}(E_\mathrm{t},x)\\ &+ n_\mathrm{g}(E_\mathrm{t})\; r_\mathrm{in}(E_\mathrm{t},x)\; (1-f_\mathrm{t}(E_\mathrm{t},x))\\ &- p_\mathrm{g}(E_\mathrm{t})\; r_\mathrm{out}(E_\mathrm{t},x)\; f_\mathrm{t}(E_\mathrm{t},x)\end{aligned} \tag{3}$$

The subscript s relates to substrate quantities, while g refers to gate quantities.

Models found in literature often assume that the energy level for tunneling into a defect and tunneling out of a defect coincide. However, first principles simulations indicate a trap level shift after a trapping process [4–6, 9]. This shift can be traced back to the fact that defects undergo atomic relaxation after a trapping process accompanied by forming, strengthening, weakening or even breaking of bonds. Additionally, the electrostatics in the defect alter when a charge carrier is introduced into a local defect.

This special feature of traps is incorporated in the *level shift model* by introducing two types of energy levels (see Fig. 2), namely one for the capture of e^- (E_in) and another for the release of e^- (E_out):

$$\begin{aligned}\partial_t f_\mathrm{t}(E_\mathrm{t},x) = &+ n(E_\mathrm{in})\; r_\mathrm{in}(E_\mathrm{in},x)\; (1-f_\mathrm{t}(E_\mathrm{in},x))\\ &- p(E_\mathrm{out})\; r_\mathrm{out}(E_\mathrm{out},x)\; f_\mathrm{t}(E_\mathrm{out},x)\,,\end{aligned} \tag{4}$$

The magnitude of the level shift is then given by

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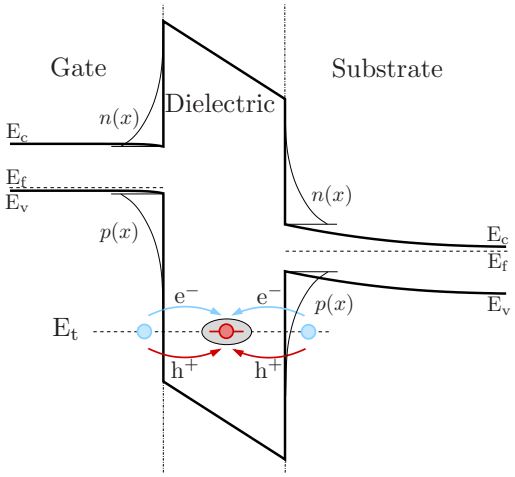

Fig. 1: Extended fixed level model. The figure shows the band diagram of a MOS structure including one single trap level within the dielectric. Dark and grey arrows mark capturing of h^+ or e^-, respectively and represent the rates in equation (1). In the conventional fixed level model, only rates from the substrate (at the right hand side of the dielectric) are considered. In the extended version also rates from the gate are accounted for. Mind that all tunneling rates are evaluated at the same energy level E_t.

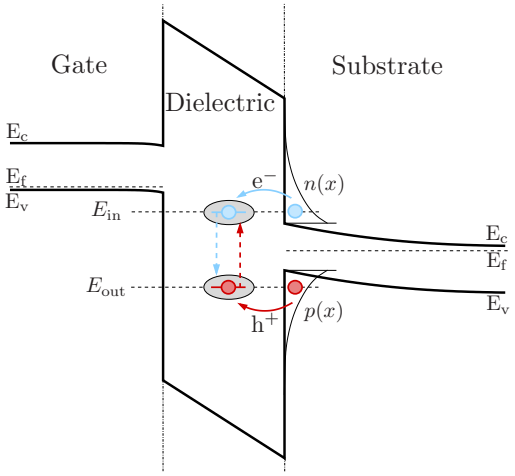

Fig. 2: The same as in Fig. 1 but for the level shift model. As opposed to the fixed level model, two distinct defect levels are considered – one for e^- capture with a corresponding trap level at E_{in} and the other for h^+ capture with a level at E_{out}. When the trap captures a substrate e^- with an energy E_{in}, the e^- capture level vanishes and reappears at E_{out}. The same holds true for h^+ and the corresponding h^+ capture level.

$$\Delta = E_{in} - E_{out}\,, \tag{5}$$

which is released to the surrounding lattice after each trapping process. The threshold voltage shift due to charge trapping can be calculated by evaluating

$$\Delta V_{th} = \frac{q_0}{C_{ox}} \int_0^{t_{ox}} (1 - \frac{x}{t_{ox}}) \rho_t(x)\; dx$$
$$\rho_t(x) = \int_{E_{t,min}}^{E_{t,max}} \rho_t(E_t, x) \Delta f_t(E_t, x)\; dE_t\,, \tag{6}$$

N_t [cm^{-3}]	3×10^{18}
E_t [eV]	-4.8
Δ [eV]	1.6
N_{it} [$cm^{-2}\,eV^{-1}$]	1.6×10^{10}
$\nu_{0,if}$ [$s^{-1}\,cm^2\,eV$]	6.3×10^{-1}
$\nu_{0,band}$ [$s^{-1}\,cm^3\,eV$]	6.3×10^{-12}
m_t	$0.5 \cdot m_e$

Table 1: Values used for the fixed level model with a broad trap distribution. The trap levels are referenced to the conduction band edge of SiO_2. $\nu_{0,if}$ and $\nu_{0,band}$ relate to the prefactor used for trapping from interface within the bandgap or from the bands, respectively. Since the distribution of trap levels is assumed to be uniform, Δ ranges from the topmost to the lowermost trap level and is centered around E_t. m_t and m_e denote the tunneling mass and the electron mass, respectively. N_{it} is the density of interface states.

where C_{ox} denotes the capacitance of the dielectric and t_{ox} the thickness of the dielectric. $\rho_t(E_t, x)$ is the trap density of states in the dielectric which is spatially and energetically distributed. This issue is of special importance regarding amorphous dielectrics since variations in the local defect configuration could cause wide distributions in trap energy levels. The change in the trap occupancy $\Delta f_t(E_t, x)$ in equation (6) is calculated by solving the above differential equations of the model employed. The bandedge energy is delivered by a Poisson solver assuming Fermi-Dirac statistics for the carrier concentrations. Note that for realistic trap densities band bending within the dielectric is normally negligible. Consequently the trap density can be regarded as a scaling factor for the total amount of trapped charges. Each simulation must be preceded by a equilibration phase in order to obtain the equilibrium occupancy of traps.

III. Fixed Level Model and its Extension

First, a comparison of the individual models will be undertaken discussing the main differences in the temporal behavior and dependencies on the gate voltage. The device under investigation is a pMOSFET with $t_{ox} = 3\,nm$ and a p-poly gate. For the following simulations, a broad uniform distribution of trap levels below the silicon valence band edge is assumed (see Table 1). For a proper analysis, the prefactors ν_0 are chosen to match the tunneling time constants given in [1].

The conventional fixed level model is taken as a starting point for discussions in order to recapitulate its basic features. Recall that the e^- capture levels coincide with the respective h^+ capture levels giving rise to a very simple correlation between the trap level occupation and the substrate Fermi level: In an energy range far below the Fermi level, the decay of the h^+ concentration favors e^- injection from the substrate compared to h^+ injection. Statistically speaking, traps at these energy level will be occupied by e^-. As the Fermi level is approaching from below, higher h^+ concentrations promote h^+ trapping and increase the h^+ occupancy of traps. Hence, h^+ trapping is restricted to a small region below the Fermi level. The temporal filling of traps is dominated by the WKB coefficient: The closer the traps are located to the interface, the smaller the respective tunneling time constants become.

Numerical simulations of trapped charges vs. time for the

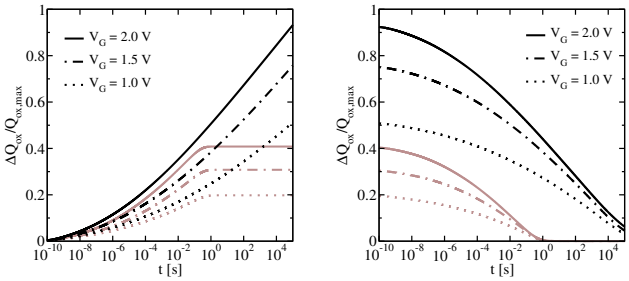

Fig. 3: Time evolution of stored charges during the on-state (left) and the subsequent off-state (right) for the conventional fixed level model (black lines) and extended fixed level model (grey lines). The distribution of trap levels is assumed to be broad. As opposed to the conventional fixed level model one can clearly observe a saturation of trapped charges when accounting for the gate during the on-state. The fact that only traps with small tunneling times are involved in the on-state is reflected in an early erase of trapped charges during the off-state.

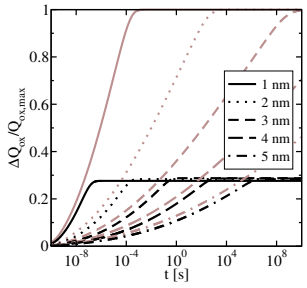

Fig. 4: Charge trapping for various gate thicknesses during the on-state. Black lines mark the extended fixed level model, while the gray lines designate the conventional fixed level model. This figure proves the importance of the gate contact when thin gate dielectrics are considered. For thicker gate dielectrics the impact of the gate becomes relevant at later timepoints.

on-state and for the off-state of the pMOSFET are shown in Fig. 3. Upon application of voltage at the gate, the Fermi level moves below the substrate valence band and h^+ injection into traps around the Fermi level is initiated. h^+ trapping can thus be imagined as a trapped h^+ front which penetrates into the dielectric with increasing time. This gives rise to a nearly linear increase of trapped charges on a logarithmic time scale as demonstrated in Fig. 3. The higher slopes for different gate voltages are linked with larger regions in energy scale which are capable of charge trapping. After the removal of the gate voltage, the h^+ channel built up during the on-state vanishes and suppresses the h^+ injection from the substrate while e^- injection is enhanced. The temporal refilling of traps starts at the interface where traps with the shortest tunneling time constants are located, and continues deeper into the dielectric. Since the same traps participated in the on-state are associated with the same tunneling time constants, detrapping takes place within similar time scales as charge trapping.

For thin dielectrics, the gate contact has to be accounted for as described in Section II, see Fig. 5. For the case when the pMOSFET is in the on-state, h^+ injection from the substrate and e^- injection from the gate determine the trap occupation

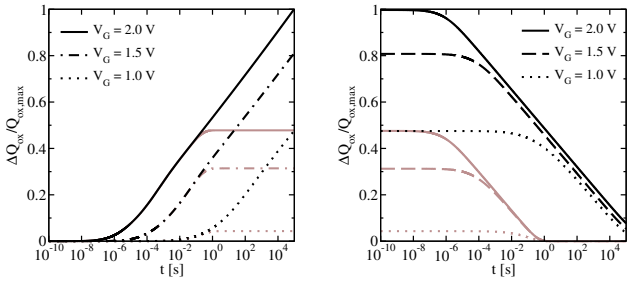

Fig. 5: The same as in Fig. 3 but for a narrow distribution for trap levels: The same setup as for the broad distribution is used, whereas $\Delta_{\mathrm{in/out}}$ is set to $0.2\,\mathrm{eV}$. Note the different onset of charge trapping for different gate biases. This can be traced back to the fact that traps participate in charge trapping which are located closer to the substrate interface for higher gate voltages (see Fig. 6).

in the dielectric. There is a border within the dielectric where the gate e^- capture rate outbalances the substrate h^+ capture rate. This border stops the penetrating tunneling front and causes the early saturation during the on-state (see Fig. 5). The fact that only traps with short tunneling times participate during the on-phase, is also reflected in a fast erase of trapped charges during the off-state. Fig. 4 depicts the amount of trapped charges as a function of the gate thickness. For gate thicknesses smaller than $5\,\mathrm{nm}$, the timepoint of saturation moves to timescales of interest.

Up to this point focus is put on very broad trap distributions only. However, trap levels are often assumed to exhibit only a narrow distribution [4]. Temporal charge trapping for energetically narrow distributed trap levels are plotted in Fig. 5. One can recognize an earlier onset of trapping for higher gate voltages. The behavior can be traced back to different regions of traps involved in charge trapping (see Fig. 6). For higher gate voltages, the traps situated around the Fermi level are moved closer to the interface decreasing the tunneling time constants. These shorter tunneling times correlate with an earlier onset of charge trapping for higher gate voltages.

IV. Level Shift Model

In the following the level shift model is discussed in the context of a special trap distributions. In contrast to the fixed level model, charge trapping is not confined to traps situated close to the Fermi level so that the temporal behavior of charge trapping is strongly affected by the energetical trap distribution.

Fig. 2 shows two opposite processes - namely e^- injection and h^+ injection. Within the level shift model e^- capture (E_{in}) may take place whereas h^+ capture is permitted. The same holds true for the h^+ capture the other way round. These competing processes mainly depend on the carrier concentrations at the respective energy levels and determine the occupation of traps. The distinct nature of e^- capture levels and h^+ capture levels is reflected in their respective prefactors ν_0. Mind that the same value of ν_0 for the substrate and the gate must be chosen since in both cases ν_0 arises from trapping between silicon bulk states and the same sort of traps.

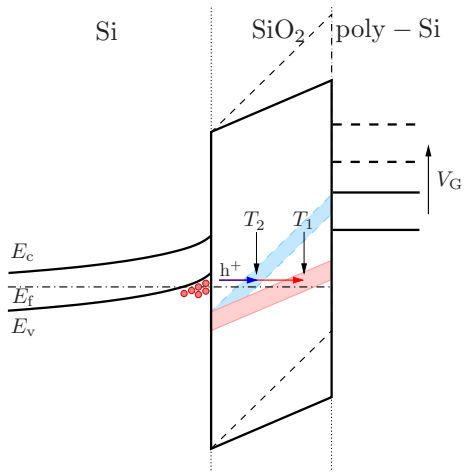

Fig. 6: Schematic of the band diagram for 2 different voltages. The crossing point between the Fermi level and the band of trap levels (grey regions) is linked to the earliest trapping events and the beginning of charge trapping. When the gate bias is increased, the crossing point is shifted closer to the substrate interface ($T_1 \rightarrow T_2$) where traps with smaller tunneling time constants ($\tau_2 < \tau_1$) are situated. This leads to an earlier onset of charge trapping for higher gate voltages.

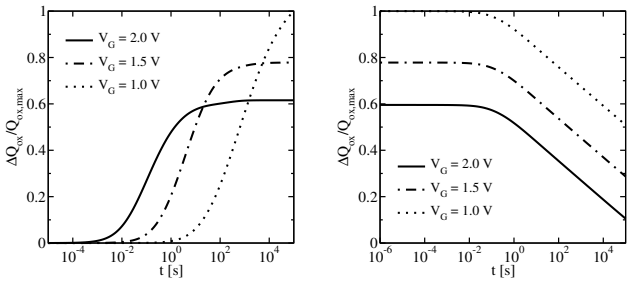

Fig. 7: The same as in Fig. 3 but for the level shift model. The parameter set used for these simulations is listed in Table 2. Mind that charge trapping sets in earlier for higher gate voltages. The same argumentation holds true here as for the fixed level model. As one can see in Fig. 6, a larger region of traps is located above the substrate valence band edge and is therefore excluded from charge trapping. This gives rise to a smaller amount of charge trapping.

Fig. 7 depicts a simulation for the set of parameters listed in Tab. 2. Upon application of a gate voltage, the Fermi level is shifted to the substrate valence band edge. For a certain energetical region of traps, h^+ injection into E_{out} is enhanced and e^- injection into E_{in} is impeded. Both the decay of charge carriers at the interface as well as the dependence of the WKB coefficient determines the temporal filling of traps. So trapping starts close to the interface around the Fermi level and continues deep into the dielectric far below the Fermi level. After the removal of the gate voltage, the initial charge carrier concentrations at the interface are slowly restored. Consequently trap states participating in charge trapping during the on-state capture e^- so that the initial trap occupation before the on-state is reobtained. The refilling of traps proceeds from the energetically deepest traps located near the interface to traps near the Fermi level and deep into the dielectric. Fig. 8 shows

Quantities	Fig. 7	Fig. 8
N_{t} [cm^{-3}]	3×10^{18}	3×10^{18}
E_{in} [eV]	-3.0	-2.6
Δ_{in} [eV]	0.2	0.2
E_{out} [eV]	-4.8	-5.0
Δ_{out} [eV]	0.2	1.4
$\nu_{0,\mathrm{in}}$ [$\mathrm{s}^{-1}\,\mathrm{cm}^3\,\mathrm{eV}$]	6.3×10^{-6}	6.3×10^{4}
$\nu_{0,\mathrm{out}}$ [$\mathrm{s}^{-1}\,\mathrm{cm}^3\,\mathrm{eV}$]	6.3×10^{-16}	6.3×10^{-16}
m_{t}	$0.5 \cdot m_{\mathrm{e}}$	$0.5 \cdot m_{\mathrm{e}}$

Table 2: Values used for the level shift model in Fig. 7 and Fig. 8. The prefactors $\nu_{0,\mathrm{in}}$ and $\nu_{0,\mathrm{out}}$ refer to the trap level at an energy E_{in} or E_{out}.

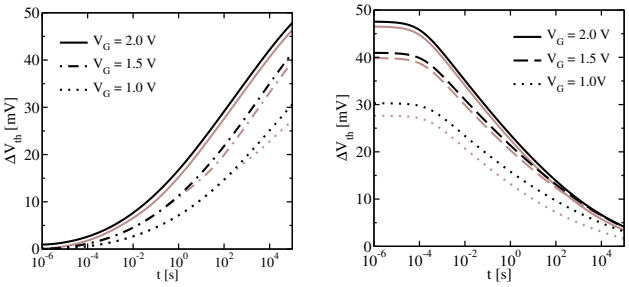

Fig. 8: The same as in Fig. 7 but for a broad distribution of trap levels. The time span of trapping and detrapping covers several decades in the on- as well as in the off-state and a higher gate voltage results in a larger amount of trapped charges. Note that the gate contact only weakly affects the V_{th} transients.

simulations for a different set of parameters (see Table 2). It is noteworthy that charge trapping from the gate contact is of minor importance. This is due to a smaller shift of the gate Fermi level and in consequence in small changes in trapping rates from the gate. h^+ trapping from the substrate below the substrate valence band is partially compensated by e^- trapping from the gate above the substrate conduction band.

V. Conclusion

As thin gate dielectrics are encountered, the impact of the gate contact becomes increasingly important. The presented model, which extends the approach of the conventional fixed level model allows for trapping and detrapping from the gate interface. It has been proven that e^- injection from the gate gives rise to an early saturation in charging transients and smaller amounts of trapped charges during the on-state of the pMOSFET. Additionally, the shift of trap levels motivated by first-principles calculations has been rigorously incorporated into a new model. For certain energetical distributions of traps, it yields V_{th} transients covering several decades in time during both the on-state as well as in the off-state.

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