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On the temperature dependence of NBTI recovery

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ABSTRACT

Poly resistors around the device can be used to perform fast in situ heating on a single device on wafer level. This is a commonly used technique to apply time-saving NBTI stress in the production line [Muth W, Walter W. Bias temperature instability assessment of n- and p-channel MOS transistors using a polysilicon resistive heated scribe lane test structure. Microelectron Reliab 2004;44(8):1251–62; Schluender C, Vollertsen RP, Gustin W, Reisinger H. A reliable and accurate approach to assess NBTI behavior of state-of-the-art pMOSFETs with fast-WLR. In: 37th European solid state device research conference ESSDERC; 2007. p. 131–4; Ting-Kang, Chi-Shiun Wang, Kuan-Cheng Su. Self-heating p-channel metal-oxide-semiconductor field-effect-transistors for reliability monitoring of negative-bias temperature instability. Jpn J Appl Phys 2007;46(12):7639–42]. We demonstrate how such a structure can not only be used as a heating element but also as a fast tool for switching the temperature. The cool down process as well as the heating procedure are rigorously analyzed and found to be very fast (<1 s) and independent of the difference between actual and target temperature. Thus, we are able perform NBTI at a certain stress temperature, which generates a certain degradation level, while the recovery itself can be studied at arbitrary temperatures. By using this technique, our understanding of the recovery physics can be probed in an unprecedented manner. In order to guarantee that our measurements probe the 'classic' NBTI mechanisms, unpolluted by tunneling currents in thin oxides and the strongly process dependent impact of nitridation, we use PMOS transistors with 30 nm SiO_2 gate oxides.

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1. Introduction

A remarkable variety of models concerning NBTI (negative bias temperature instability) degradation and recovery have been published [4–11]. Unfortunately, those models are often inconsistent or even controversial. A reason for that might be the fact that people perform experiments on different device technologies with different gate oxide thicknesses, implantations and metallization stacks. If we consider diffusing hydrogen to play a crucial role in NBTI, as suggested by the RD (reaction–diffusion) model [4,7,9], the device geometry [6], the nature of the gate oxide [6,8,24] as well as the character of interface-near layers are likely to influence the situation significantly. A reliable comparison of phenomena observed is difficult, when such different devices are stressed under various bias and temperature conditions. Consequently, the dynamics of degradation and relaxation have been attributed to many effects like hole trapping/tunneling [12], hydrogen release at the interface [4,7,9], hydrogen diffusion/reaction/cracking within the gate oxide and at the interface [7,9,11,13–15,21], bonding and antibonding hydrogen configurations [16,17], various oxide defects with wide spread energy trap levels [18] and some more.

To summarize the widely reported physical facts, temperature as well as electric field (respectively the interface free hole concentration) play an important role in NBTI degradation and recovery. The question if the total effect is a fusion of multiple components which can differ in their dependencies remains to be seen.

In order to detect fast recovering components a short stress-measurement delay is required. While fast measurements in the microsecond regime have been achieved for devices with thin gate oxides [19], we report for the first time sub-millisecond I_d–V_g measurements on thick gate oxides, which are more complicated to achieve due to the much larger gate voltages differences between stress and recovery. A large voltage switch involves a temporary high charging/discharging current which can exceed the measurement range and is therefore hard to handle. In order to achieve reasonable measurement speed and resolution we have used SMUs (source-measurement units) on highest novel industrial standard. By combining a fast sampling measurement with a conventional spot measurement, we are able to record fast recovering components (<1 ms) as well as long-term effects.

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In this paper our aim is to investigate the temperature dependence of NBTI recovery. The motivation to do this is to clarify, if the observed effects are thermally activated or not. In the case of NBTI thermodynamic models are often linked to mobile hydrogen which can diffuse around and passivate or create dangling bonds at the substrate-oxide interface and inside the bulk of the gate-oxide [15,16,21,24,25].

2. Degradation quenching

A trivial problem encountered in the observation of temperature effects on NBTI recovery is the need to dispose of a set of (i) comparable devices that are brought to (ii) the same degradation level by identical stress, but which then (iii) recover at different temperatures.

The first condition (comparable devices) may be solved by careful sample selection, involving thorough characterization before stress. Our preliminary measurements indicate that a good correlation between the degradation levels observed in equally fabricated devices on the same wafer is to classify them by their virgin CP (charge pumping) current. The 0-h CP current gives information about the initial interface state density of the device.

The second condition (identical degradation level before recovery), however, cannot – and, to our knowledge, has not – be solved by classically available stress and characterization methods, if the third condition (various recovery temperatures) has to be maintained. Classical methods are either based on performing stress and recovery at the same temperature, or strictly separate stress and recovery by a long, scarcely observable and greatly undefined transition period. While the first approach can provide perfect observation of recovery at very good time resolution [19], it obviously always violates condition (ii) if condition (iii) is fulfilled and vice versa.

Therefore, in order not to induce an unknown amount of additional degradation during cooling, the temperature switch has to be fast, well controlled and independent of the difference between actual and target temperature. This demand cannot be fulfilled, when we use a conventional thermo-chuck system for the cool down process. Since the cooling duration of such systems is very long (>30 min) and strongly dependent on the target temperature, the high fraction of unknown additional degradation will always distort the results.

Not to mention contact difficulties related to thermal expansion of probe needles and metal pads when the wafer heats up or cools down. In short, this technique suffers from a lot of unacceptable systematic errors and drawbacks.

Our approach to harmonize all conditions and to get rid of the above described technical difficulties is to use a MOS device which is embedded into a poly resistor (Fig. 1). Such a test structure can bring the device to a defined stress temperature by local Joule heating. When the heating current vanishes, the device cools down quickly towards ambient (i.e., chuck) temperature.

During heating and cooling the saturation drain current can be used as a thermometer to calibrate the $Si–SiO_2$ interface temperature by using a procedure similar to the one suggested in [3]. The method is very accurate due to the perfect quadratic relationship between saturation drain current and interface temperature. The substrate-gate oxide interface is mentioned here intentionally because most studies suggest this interface to be the location of concern for NBTI.

As can be seen in Fig. 2, the cooling duration of the device is basically very short and virtually completed after one second independently of the difference between stress and recovery temperature. If the stress temperature is 125 °C, the time to cool down to 80 °C(±1 °C) (ΔT = 45 K) is approximately 0.3 s which is about three times faster than the time to cool down to −40 °C(±1 °C) (ΔT = 165 K). However, after one second all devices are less than 1 K away from their target temperatures. In this specific experiment a reliable resolution <1 K could not be achieved do to the noisy data of the sampling measurement.

In order to prevent any recovery during cooling, the stress bias remains applied to the gate until the device has reached its target temperature. During this additional second, stress continues in an undefined way, but since this additional stress time is very small compared to the main stress period, and since the cool down time is nearly independent of ambient temperature and thus identical for all samples, we believe that the transition time from stress to recovery can safely be neglected.

Consequently, our technique guarantees that the degradation level is still the same for all devices in the moment the recovery phase starts. This moment is the point of time, when the gate bias switches from stress level to threshold voltage.

By "quenching" the degradation level to an arbitrary temperature in the way described above, we are capable of investigating the role of temperature during NBTI recovery unambiguously, and shall present results in the next paragraphs.

3. Temperature dependent recovery

During the stress period the heater generates a defined interface temperature and a certain bias is applied at the gate (NBTI). Source and Drain are at zero volts. After 1000 s stress, the heating current is taken away. The device immediately cools down and approaches ambient temperature. This temperature is usually defined by the underlying thermo-chuck. Consequently, if we want study recovery at −40 °C the chuck has to be at that temperature already before stress. Of course, the required power supply for the polyheater in order to reach the much higher stress temperature

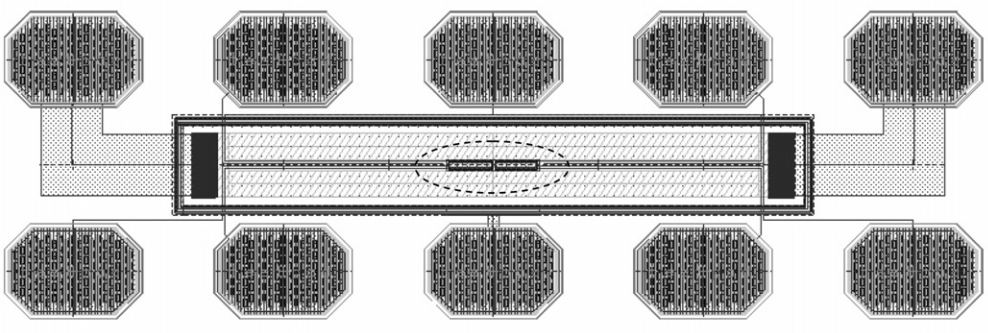

Fig. 1. Device embedded into polyheater structure. The transistor is pointed out by the circle.

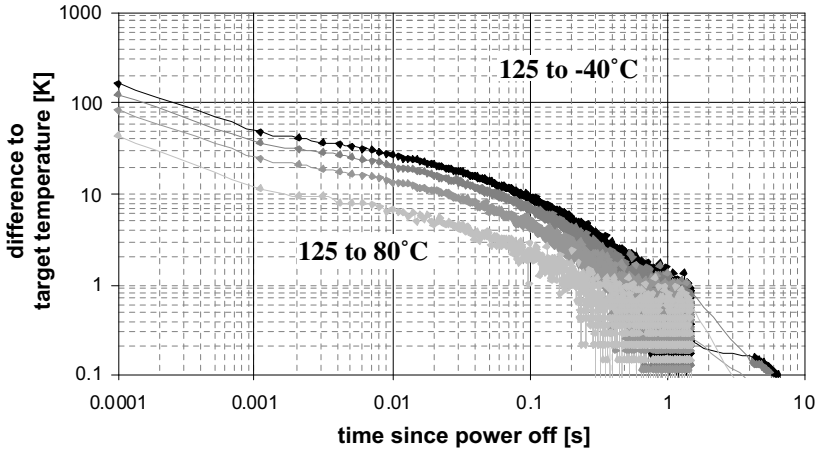

Fig. 2. Temperature characteristics of the polyheater during cooling from stress temperature (125 °C) to different recovery target temperatures (−40/0/40/80 °C).

(125 °C) is the greater the lower the base temperature of the chuck.

One second after the heater has been turned off the gate bias switches to threshold voltage which terminates the stress abruptly and the relaxation of the drain current is recorded. As already mentioned before, one second is required to guarantee that the device has definitely reached its target temperature when the recovery measurement starts. As the gate bias changes to threshold voltage (−1.1 V) the drain bias rises simultaneously to its readout value, which is −2.5 V, in order to measure the saturation drain current. The transition from stress to readout bias conditions requires about 200 μs and is limited by the speed of the source unit. The first measured current at recovery temperature and bias conditions can be recorded about 300 μs after the stress voltage has been removed and about one second after the heater has been turned off. The time dependent development of the saturation drain current can then be converted into a stress/recovery induced threshold voltage shift. As a reference we use the virgin saturation drain current recorded before stress at the respective target temperature [20].

The result of such a temperature quenched recovery measurement is illustrated in Fig. 3. The DUTs are PMOS transistors with a 30 nm SiO_2 gate-oxide. The channel length is 4 μm and its width is 40 μm. The stress temperature, supplied by the polyheater, was 125 °C. The recovery temperatures were 125/80/40/0/−40 °C. Stress and recovery duration was respectively 1000 s.

As can be seen in Fig. 3, the recovery curves look quite similarly except for a temperature dependent offset which is already present at the first measurement point at 300 μs.

Obviously there is no significant long term temperature dependence visible, although the temperature was varied by more than 160 K. At a first glance all the recovery curves seem to have nearly the same slope which would indicate a completely temperature independent recovery phase.

In Fig. 4 the drift per decade is evaluated more precisely for the first hundred milliseconds (diamonds) and for the last two decades (triangles) of the recovery branch. On closer inspection there is a temperature dependence visible in the first 100 ms right after stress. We observe an increasing slope of the recovery curve with increasing temperature. While at −40 °C the amount of recovery is 1 mV per decade, it is about three times higher for temperatures above 80 °C.

A few seconds later all curves are nearly parallel. In Fig. 4 we can see that after 10 seconds the decrease of threshold voltage shift has leveled off to about 2 mV per decade independently of the recovery temperature. This holds for at least two to three decades of time.

The offset at 300 μs can be explained qualitatively by the following arguments. Since a fast temperature dependent component has been identified, it is likely that the actual offset at the real beginning of the recovery is smaller than the one observed at 300 μs. A small offset can be explained by the temperature

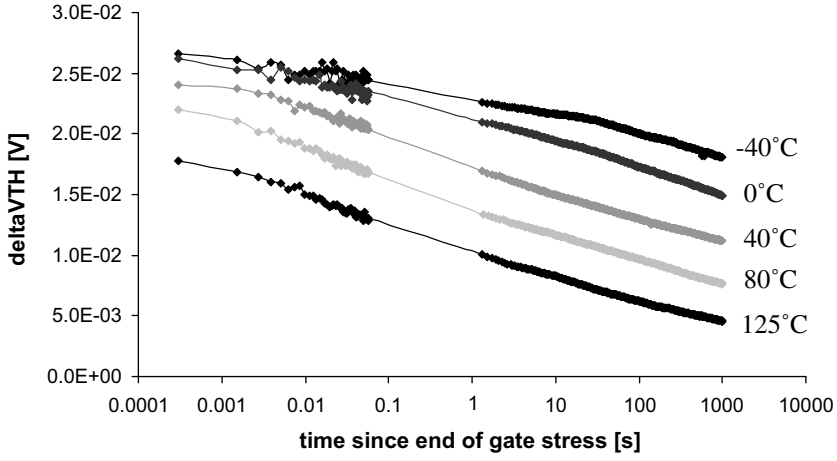

Fig. 3. Recovery of threshold voltage stress conditions: VGS = −16.5 V, VDS=0.0 V, T = 125 °C; recovery conditions: VGR = −1.1 V, VDR = −2.5 V, T = −40/0/40/80/125 °C.

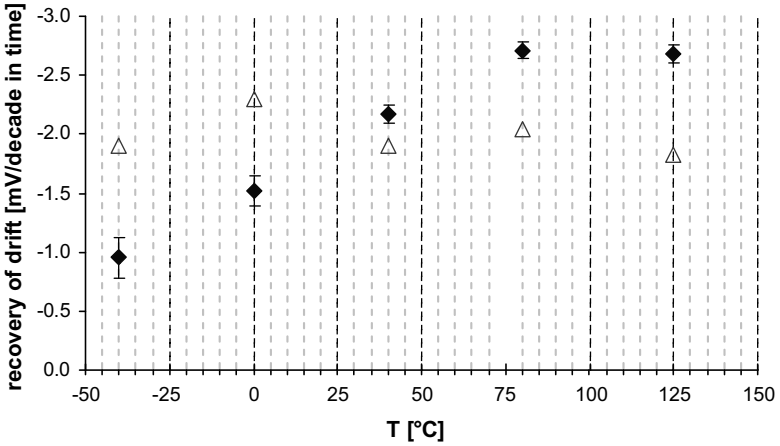

Fig. 4. Temperature dependent recovery ♦ between 1 ms and 100 ms post stress Δ between 10 s and 1000 s post stress.

dependent position of the Fermi-level at threshold voltage. While at low temperature the Fermi-level is closer to the valance band edge, it moves further towards midgap the higher the temperature. If we assume the creation of interface states within the silicon band gap under NBTI, their charge state (occupation probability) is governed by the position of the Fermi-level. This means, at lower temperatures more of them are positively charged which arises in a greater threshold voltage shift. The temperature dependent variation of the Fermi-level apparently causes a systematic error which is, however, believed to be too little to explain the full offset at 300 μs.

All in all the result is definitely quite surprising in particular if we consider that degradation during stress has usually high temperature dependence. It suggests that degradation and recovery are different mechanisms with different dependencies.

A crucial point is that temperature independence challenges models based on hydrogen dominated recovery. In dispersive diffusion models hydrogen is believed to be stored in traps within the oxide, at the interface or somewhere else close to the oxide. In order to passivate stress induced damage, the H or H_2 molecule has to be relieved from there which means to overcome a thermodynamic barrier. At lower temperatures the probability of release as well as the diffusion velocity of hydrogen should be much lower. If such a mechanism would be the controlling process, one would expect a clear freeze of recovery at −40 °C. However, we still observe strong recovery at low temperatures.

The same argument also holds for an imaginable switching of hydrogen from a bonding to an antibonding Si–H configuration, as proposed by [17]. Since the transfer from bonding to antibonding is a thermodynamic process, it should be highly temperature accelerated.

To put it in a nutshell, the above described experiment suggests that it is a weakly temperature dependent component that governs the recovery branch at least for relaxation times greater than some seconds. This could be for example a tunneling component originating from substrate carriers which might get captured by positively charged oxide defects, as suggested by [5,11,15]. The role of interface states in the recovery process will be discussed in the next paragraph by means of CP (charge pumping).

4. On the role of interface states

According to a wide spread belief, hydrogen passivated interface states (Si–H bonds) can be depassivated during stress. The cracking of bonds is believed to be accelerated by temperature and electric field. When hydrogen diffuses away, a silicon dangling bond is left behind. As a consequence, the total density of interface states increases. In the case of a PMOS transistor most interface states, which are assumed to be amphoteric or donor-like, are positively charged at threshold voltage, which results in a positive shift of the transfer curve.

The RD model assumes the interface states to be the only contribution to device parameter shift. In this model both the bond cracking during stress as well as the repassivation of dangling bonds during recovery are diffusion limited. Alternative theories [25,26] deal with variable energy barriers and quantum wells for hydrogen release and recurrence at the interface in order to explain long term recovery and permanent components. Such models are rather reaction than diffusion limited. In essence, all approaches which are based on relaxation or atomic motion are strongly coupled to thermodynamic equations.

To check the temperature dependence of interface states recovery, we have measured CP currents before stress and after recovery at the appropriate temperatures.

The maximum CP current is proportional to the density of interface states averaged by a certain temperature dependent energy interval within the silicon bandgap [27,28].

$$I^{\mathrm{vir}}_{\mathrm{CP\,max}}(T) = q \cdot f \cdot A \cdot \overline{D^{\mathrm{vir}}_{\mathrm{it}}}(\Delta E(T)) \cdot \Delta E(T) \tag{1}$$

$$I^{\mathrm{str+rec}}_{\mathrm{CP\,max}}(T) = q \cdot f \cdot A \cdot \overline{D^{\mathrm{str+rec}}_{\mathrm{it}}}(\Delta E(T)) \cdot \Delta E(T) \tag{2}$$

Here q is the elementary charge, f the measurement frequency, A the device area and $D_{\mathrm{it}}(\Delta E)$ the density of states averaged by the active energy interval $\Delta E(T)$ within the silicon bandgap.

The CP current consists of the following contributions.

$$I^{\mathrm{str+rec}}_{\mathrm{CP\,max}}(T_{\mathrm{r}}) = I^{\mathrm{vir}}_{\mathrm{CP\,max}}(T_{\mathrm{r}}) + \Delta I^{\mathrm{str}}_{\mathrm{CP\,max}}(T_{\mathrm{r}}) - \Delta I^{\mathrm{rec}}_{\mathrm{CP\,max}}(T_{\mathrm{r}})$$

$$\Delta I_{\mathrm{CP\,max}}(T_{\mathrm{r}}) = q \cdot f \cdot A \cdot \overline{\Delta D^{\mathrm{total}}_{\mathrm{it}}}(\Delta E(T_{\mathrm{r}})) \cdot \Delta E(T_{\mathrm{r}}) \tag{3}$$

$$\overline{\Delta D^{\mathrm{total}}_{\mathrm{it}}}(\Delta E(T_{\mathrm{r}})) = \overline{\Delta D^{\mathrm{str}}_{\mathrm{it}}}(\Delta E(T_{\mathrm{r}})) - \overline{\Delta D^{\mathrm{rec}}_{\mathrm{it}}}(\Delta E(T_{\mathrm{r}})) \tag{4}$$

Here T_{r} corresponds to the appropriate recovery temperatures. The total change in D_{it} can be attributed to an increase during stress and a subsequent decrease during recovery. Since the CP current right after stress was not measured, in order not to influence the degradation level, the value of $\Delta I_{\mathrm{CP\,max}}$ (stressed) and ΔD_{it} (stressed) is basically unknown. However, this is not considered a serious limitation since the devices have been stressed under the same bias and temperature conditions anyway. This means, the increase of D_{it} due to stress should be identically for all devices. What remains actually temperature dependent is the decrease of the CP current and D_{it} due to recovery.

If we consider the pure change of the CP current due to stress and recovery in Fig. 5 (triangles), the remaining interface damage seems to increase with decreasing temperature. At a first glance this result would confirm a temperature dependent recovery theory as reported in [23].

If we, however, keep in mind that CP currents, measured at different temperatures, record a different part of the silicon bandgap [27,28], the absolute increase $\Delta I_{CP\,max}(T_r)$ has to be corrected by a temperature dependent weighting factor in order to obtain a meaningful comparison.

The visible part of the silicon band gap in a CP measurement at temperature T is defined by:

$$\Delta E(T) = 2kT \cdot \ln\left(\frac{\Delta V_G}{\overline{v_t}(T) \cdot \bar{\sigma} \cdot n_i(T) \cdot \sqrt{t_r \cdot t_f} \cdot (V_{TH} - V_{FB})}\right) \tag{5}$$

In Eq. (5) k is the Boltzmann constant, T the temperature, v_t the average thermal drift velocity for electrons and holes, σ the medium capture cross section, n_i the intrinsic carrier density, t_r/t_f the rising/falling times of the gate pulse, ΔV_G the pulse amplitude and $(V_{TH} - V_{FB})$ the difference between threshold and flatband voltage of the device. For typical device and measurement parameters ($\sigma = 1E-15\ cm^2$, $\Delta V_G/t_r = \Delta V_G/t_f = 8\ V/\mu s$) the energy interval is calculated as a decreasing function of T in Fig. 6, and this implies that both I_{CP} and ΔI_{CP} must anyway be decreasing functions of T. In addition, $D_{it}(E)$ is variable within the silicon bandgap [29]. Consequently, we must also consider that the medium density of states, which is averaged by this energy interval, will change if ΔE increases or decreases.

Hence, it is the product of the medium density of states and the active energy interval that differs for every temperature. This product is the total number of interface states per unit area which contribute to the CP signal at a certain temperature.

$$\overline{D_{it}}(\Delta E(T_r)) \cdot \Delta E(T_r) = N_{it}(T_r) \tag{6}$$

Thus, if we want to compare CP currents recorded at various temperatures, we have to evaluate a weighting factor first of all that normalizes all currents to a certain reference temperature T_0 which we set equal to the stress temperature T_s:

$$\begin{aligned} N_{it}^{vir}(T_r) &= w(T_r, T_s) \cdot N_{it}^{vir}(T_s) \\ w(T_r, T_s) &= \frac{N_{it}^{vir}(T_r)}{N_{it}^{vir}(T_s)} = \frac{I_{CP\,max}^{vir}(T_r)}{I_{CP\,max}^{vir}(T_s)} \end{aligned} \tag{7}$$

Experimentally, the factor is straight-forward to obtain by measuring the CP currents on a virgin device at first at stress temperature T_s and afterwards at the appropriate recovery temperatures T_{ri}. Such an experiment has been carried out and the results are illustrated in Fig. 7. Note, that the weighting coefficient in the inlay of Fig. 7 varies by a factor of almost four over the whole temperature range, more than would have been expected from the pure energy-interval consideration in Fig. 6.

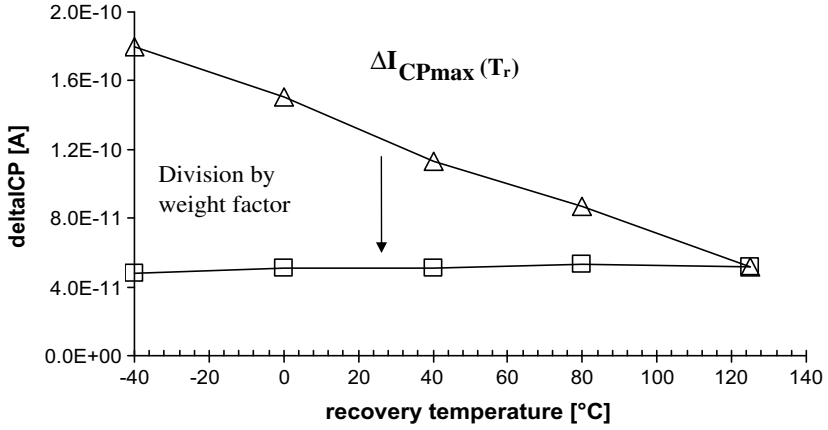

Fig. 5. Increase of CP current after stress and recovery while the triangles reflect the pure difference of $\Delta I_{CP\,max}(T_r)$, the squares show the difference corrected by the temperature weight factor.

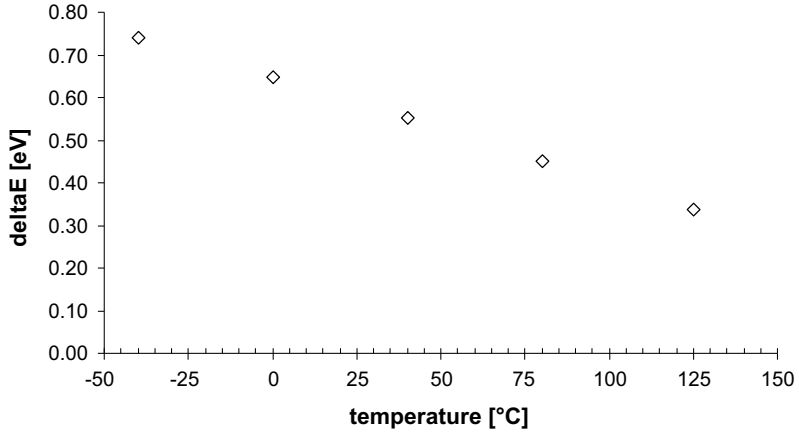

Fig. 6. Active energy interval for CP, calculated for the appropriate recovery temperatures.

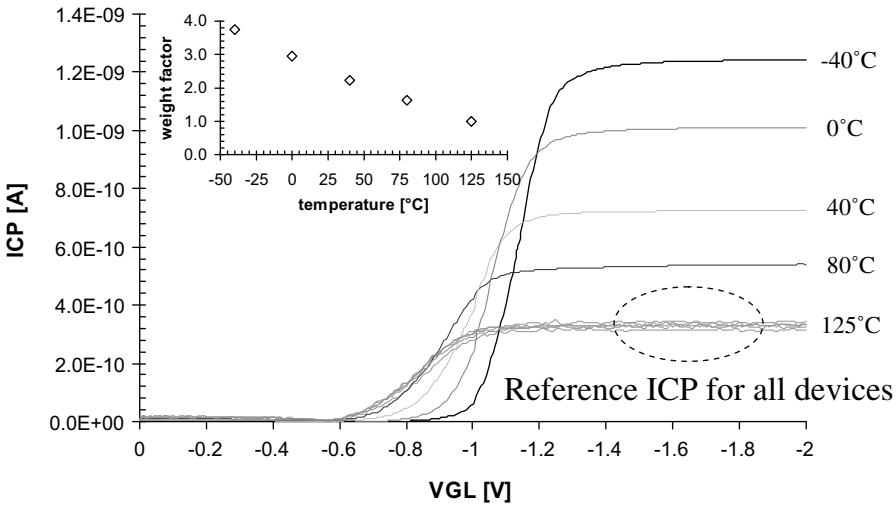

Fig. 7. Virgin CP currents measured at different recovery temperatures and at stress temperature. The illustration in the left corner shows the evaluated weight factors $w(T_{ri}, T_s)$.

Having identified all weighting factors, the systematic error in Fig. 5 can be eliminated by normalizing all $\Delta I_{CP\,max}$ signals to stress temperature.

$$\Delta I^{norm}_{CP\,max}(T_{ri}) = \frac{\Delta I_{CP\,max}(T_{ri})}{w(T_{ri}, T_s)} \tag{8}$$

The results are shown as squares in Fig. 5.

The assumption made, by dividing the actual CP current at recovery temperature by the weight factor, is that the shape of the $D_{it}(E)$ curve remains conserved which implicates that energy intervals with a higher D_{it} are weighted heavier than areas with a lower D_{it}. This a rational assumption if we consider that the probability to create a trap with the energy E may be proportional to the virgin density of states at the same energy.

Again we do not see a significantly temperature accelerated recovery of interface states. The factor ΔD_{it} (recovery) in Eq. (4) is either the same for all temperatures or just zero which would eliminate interface states recovery at all like reported in [22].

On the other hand, the absolute increase of the total CP current after stress and recovery indicates a significant number of interface states has been generated during stress (ΔD_{it} (total) > 0). The total number of states (N_{it}) after stress and recovery is still about 16% higher than before stress. We therefore again observe a discrepancy between stress and recovery with respect to the creation and relaxation of interface states.

The results, which we have shown in this paragraph, demonstrate explicitly that on our device interface states do not play the major role in long term threshold voltage recovery.

5. Conclusion

In this paper we have introduced a new method to quench nBTI degradation on wafer level to an arbitrary temperature, which enables us to observe the recovery of identically stressed devices at different temperatures. A case study on the recovery at five different temperatures ranging from −40 °C to 125 °C has demonstrated a fast temperature dependent component which influences the recovery curve within the first seconds post stress. After this period of time the temperature does not seem to influence the slope of the recovery branch anymore which suggests a non-thermodynamic process to be dominant.

By performing CP experiments before stress and after recovery the role of interface states has been elaborated. We have pointed out the difficulty of comparing CP currents measured at different temperatures and presented a method how to compare the results anyway in a rational manner. The results show that although interface states are generated during stress, they do not recover significantly when the stress bias is taken away. Furthermore, their recovery cannot be accelerated or decelerated when the temperature varies between −40 °C and 125 °C. Our observations therefore challenge thermodynamic and interface controlled recovery theories like the RD model.

Acknowledgements

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