

The Effect of Microstructure on the Electromigration Lifetime Distribution

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Abstract- In this work we analyze the influence of the statistical distribution of copper grain sizes on the electromigration time to failure distribution based on numerical simulations. We have applied a continuum multi-physics electromigration model which incorporates the effects of grain boundaries for stress build-up. It is shown that the lognormal distribution of grain sizes causes a lognormal distribution for the times to failure. Moreover, the increase of the standard deviation of the grain size distribution results in an increase of the electromigration lifetimes standard deviation.

I. INTRODUCTION

According to the International Technology Roadmap for Semiconductors (ITRS) 2008 Update [1], the copper dual-damascene technology process will continue to be applied for the fabrication of on-chip interconnects for the next technological nodes. The metal wiring pitch in microprocessors units will be scaled down to 64 nm for the 32 nm node, and 44 nm for the 22 nm node. At the same time, the expected operating current densities can reach 2.11 MA/cm² and 2.80 MA/cm², respectively.

The continuous shrinking of the dimensions of on-chip interconnects and the introduction of advanced backend-of-line (BEoL) manufacturing process steps increases the complexity of physical phenomena behind the electromigration failure. The total wiring length amounts to kilometers arranged in several levels of metallization, with millions of interlevel connections. The tendency of modern technologies to increase the interconnect length and, at the same time, to reduce the cross section, makes the interconnect structures more and more susceptible to electromigration. Currently, integrated circuits are often designed using simple and conservative design rules to ensure that the resulting circuits meet reliability goals. However, this precaution leads to reduced performance for a given circuit and metallization technology.

Experiments have shown that electromigration times to failure present a lognormal distribution. Although the origin of such a distribution is not entirely clear, the copper grain sizes seem to follow lognormal distributions in typical dual-damascene process technology [2]. Therefore, this has been considered as the major cause for the lognormal distribution of electromigration times to failure. The understanding of the electromigration lifetime distribution is crucial for the extrapolation of the times to failure obtained empirically from accelerated tests to real operating conditions, as performed by a modified form of the Black equation [2].

Also, it has been shown that the microstructure plays a key role regarding the failure mechanisms in copper dual-damascene interconnects [3]. It affects electromigration in different ways. They are natural locations of atomic flux divergence, they act as fast diffusivity paths for vacancy diffusion [4], and grain boundaries act as sites of annihilation and production of vacancies [5].

The main challenge in electromigration modeling is the diversity of physical phenomena which have to be taken into account for an adequate description of the problem. Electromigration transport is also accompanied by material transport driven by the gradients of material concentration, mechanical stress, and temperature. Furthermore, taking into account the effects of interfaces and grain boundaries as fast diffusivity paths imposes new challenges for electromigration modeling.

In this work we investigate the origin of the statistical distribution of electromigration times to failure as a function of the distribution of copper grain sizes. The effect of lognormal grain size distributions on the distribution of electromigration lifetimes of fully three-dimensional copper dual damascene interconnect structures is studied based on numerical simulations. We have applied a continuum multi-physics electromigration model which incorporates the effects of grain boundaries for stress build-up. Moreover, we have developed a tool to include the microstructure into the simulations based on a given statistical distribution of grains sizes.

II. ELECTROMIGRATION MODEL

Several driving forces are responsible for the vacancy transport in a conductor line under electromigration. The combination of these driving forces leads to the total vacancy flux given by

$$\vec{J}_v = -D_v \left(\nabla C_v + \frac{|Z^* e|}{k_B T} C_v \nabla \varphi + \frac{f \Omega}{k_B T} C_v \nabla \sigma \right), \quad (1)$$

where D_v is the vacancy diffusion coefficient of the dominant transport path, C_v is the vacancy concentration, $Z^* e$ is the effective charge, f is the vacancy relaxation ratio, Ω is the atomic volume, σ is the hydrostatic stress, k_B is Boltzmann's constant, and T is the temperature.

Vacancies accumulate or vanish in sites of flux divergence, and this dynamics is described by the continuity equation

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G(C_v), \quad (2)$$

where $G(C_v)$ is the source function which models vacancy generation and annihilation processes [6]. The source term plays a major role for the mechanical stress buildup and is taken into account only at interfaces and grain boundaries. It comprises three processes, namely, the exchange of point defects between adjacent grains, exchange of point defects between grains and grain boundaries, and the formation/annihilation of point defects at grain boundaries.

In our model grain boundaries are treated as separate regions which can trap or release vacancies [7], as shown in Fig. 1. We denote the vacancy concentration from both sides of the grain boundary as C_v^1 and C_v^2 , respectively, and the concentration of immobile vacancies which are trapped inside the grain boundary as C_v^{im} .

The trapping rate of vacancies at the grain boundary, which corresponds to the generation/recombination rate, is controlled by the atomic fluxes J_v^1 and J_v^2 , yielding [7]

$$\frac{\partial C_v^{im}}{\partial t} = G = \frac{1}{\tau} \left[C_v^{eq} - C_v^{im} \left(1 + \frac{2\omega_R}{\omega_T(C_v^1 + C_v^2)} \right) \right], \quad (3)$$

where ω_T is the trapping rate of vacancies from both neighboring grains, ω_R is the release rate, and C_v^{eq} is the equilibrium vacancy concentration inside the grain boundary, given by

$$C_v^{eq} = C_v^0 \exp\left(\frac{\sigma_{nn} \Omega}{k_B T}\right), \quad (4)$$

where C_v^0 is the equilibrium vacancy concentration in the absence of stress and σ_{nn} is the stress component normal to the grain boundary. In (3) τ represents the vacancy relaxation time, which characterizes the efficiency of the grain boundary as vacancy sink/source [7]

$$\frac{1}{\tau} = \frac{\omega_T(C_v^1 + C_v^2)}{\delta}. \quad (5)$$

Sarychev et al. [8] introduced the contribution of vacancy migration and generation/annihilation processes for stress build-up in a three-dimensional model of stress evolution during electromigration. Considering the grain boundary model we have proposed that the strain growth from both sides of the grain boundary is proportional to the growth rate of immobile vacancies

$$\frac{\partial \varepsilon_{kk}}{\partial t} = \Omega \left[(1-f) \nabla \cdot \vec{J}_v + f \frac{\partial C_v^{im}}{\partial t} \right], \quad (6)$$

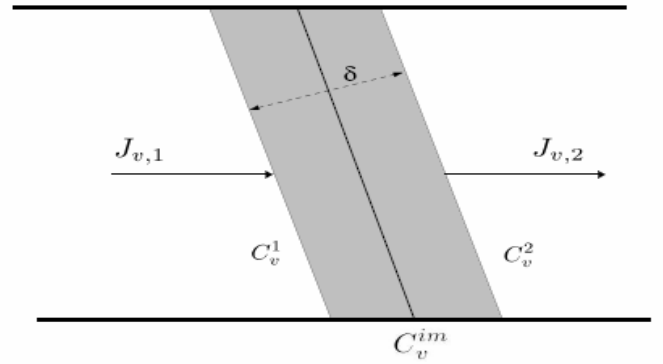


Fig. 1. Grain boundary model.

where ε_{kk} is the trace of the strain vector.

Equation (6) shows that vacancies trapped at the grain boundaries are responsible for build-up of tensile stress. When the grain boundaries are able to capture large amounts of vacancies, a high tensile stress develops.

The system of equations formed by (1) – (6) is solved until a stress threshold (σ_{th}) for void nucleation is reached at an intersection of grain boundaries with the capping layer. These intersections are considered sites of weak adhesion and, consequently, most susceptible to void nucleation.

Gleixner et al. [9] showed that the stress threshold is given by

$$\sigma_{th} = \frac{2\gamma_s \sin \theta_c}{R_p}, \quad (7)$$

where R_p is the radius of the adhesion-free patch, θ_c is the contact angle between the void and the surface, and γ_s is the surface energy.

III. SIMULATION APPROACH

Equations (1) – (6) are solved using the finite element method (FEM). Grain boundaries, and generally, all interfaces of the problem geometry have to be supplied with an appropriately fine FEM mesh. This is necessary in order to provide sufficient resolution for the local dynamics described by the proposed model.

In order to include the grain distribution into the numerical simulations, a microstructure generator tool has been developed. Given a specific interconnect structure and providing the tool with a median grain size and corresponding standard deviation, it generates a lognormal distribution of grain sizes. Then, following this distribution, the interconnect line is cut along its length by the planes that form the grain boundaries. Furthermore, the angles between the grain boundaries' planes and the line surface follow a normal distribution with median value of 90 °C. The corresponding standard deviation can also be specified.

In Fig. 2 we present the schema of the simulation procedure. Three standard deviations for the distribution of grain sizes are considered, namely 0.1, 0.3 and 0.6. For each of them 20 dual-damascene interconnect structures were created with the microstructure generator.

As the interconnect line is assumed to present a bamboo-like structure, the median grain size is equal to the line width, 0.10 μm . The barrier, capping and interlayer dielectric layers are Ta, SiN, and SiO_2 , respectively. The corresponding interconnect structure is shown in Fig. 3.

The applied current density is 1.5 MA/cm^2 , and the temperature is 300 $^\circ\text{C}$. We have used a stress threshold value as failure criterion, which means that the electromigration time-to-failure represents the time for a void nucleation to occur. Thus, the time-to-failure is determined by the time for the stress to reach a given threshold value at some intersection between a grain boundary and the SiN layer. Such a failure criterion is equivalent to a very small resistance increase criterion, which is commonly used in experiments.

IV. RESULTS AND DISCUSSION

Fig. 4 shows the hydrostatic tensile stress development for the structures with grain size standard deviation of 0.3. The stress peak value follows the peak of trapped vacancy concentration and is located at the intersection of grain boundaries with the capping layer, as shown by Fig. 5.

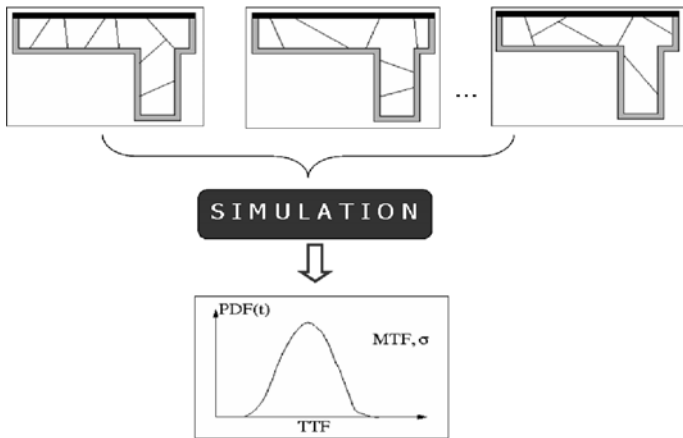


Fig. 2. Schematic simulation procedure.

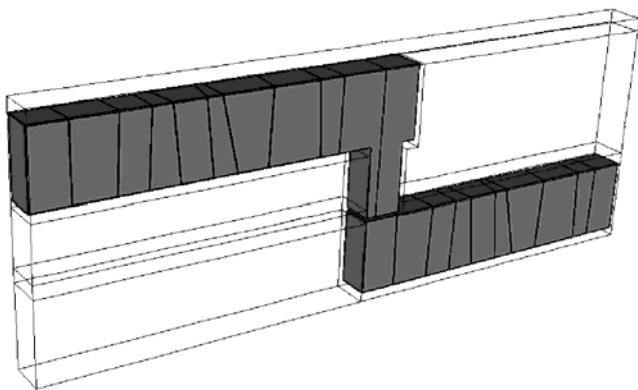


Fig. 3. Simulated dual-damascene interconnect structure.

Collecting the times-to-failure from Fig. 4 and calculating the cumulative failure percentages resulted in lognormal

distributions of electromigration lifetimes, as shown in Fig. 6. The obtained standard deviations of electromigration lifetimes are 0.0065, 0.0080, and 0.0085 for the grain size distributions with standard deviations of 0.1, 0.3, and 0.6, respectively, with the standard deviation (σ) for a lognormal distribution given by

$$\sigma = \sqrt{\frac{1}{N-1} \sum_{i=1}^N (\ln TTF_i - \ln MTF)^2}, \quad (8)$$

where TTF_i is the time to failure of the i -th test structure, N is the number of test structures, and MTF is the mean time to failure of the lognormal distribution

$$\ln MTF = \frac{1}{N} \sum_{i=1}^N \ln TTF_i. \quad (9)$$

The standard deviations for the electromigration lifetimes are rather small compared to those frequently observed in experiments [2]. Several factors can explain this behavior. First, for convenience, we have used a small value of stress threshold as failure criterion to determine the interconnect lifetime. As can be seen from Fig. 4, the variation of the lifetimes can be more pronounced for higher stress thresholds. Second, the simulation parameters and material properties are independent of the grain distribution. This means that mechanical properties and diffusivities, for example, are equal and constant for all grains in an interconnect line, for all simulated structures. This is clearly not the case in real experiments, as it is well known that material properties vary not only from sample to sample but also according to the grain distribution along the line. Therefore, the small standard deviations obtained from our simulations, compared to those experimentally observed, should be indeed expected.

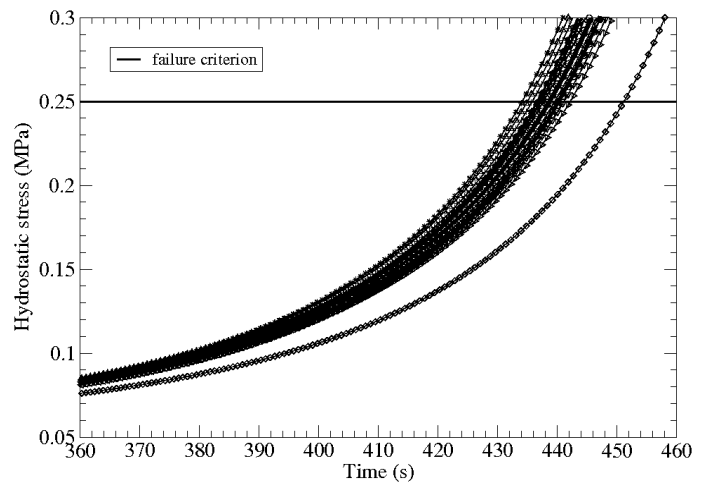


Fig. 4. Peak of hydrostatic stress development for the set with grain size standard deviation of 0.3.

V. CONCLUSION

We analyzed the electromigration failure development in typical copper dual-damascene interconnect structures based on numerical simulations. A continuum electromigration model which describes mechanical stress build-up in connection with the microstructure effect was applied. The simulation results indicate that the lognormal distribution of the copper grain sizes is the primary cause for the lognormal distributions of the electromigration lifetimes. Moreover, an increase of the standard deviation of the grain size distribution leads to an increase of the electromigration time-to-failure distribution. We observed that the peak of tensile stress is located at the intersection of grain boundaries with the capping layer, following the peak of trapped vacancy concentration. This shows that the microstructure has a decisive impact on the determination of void nucleation sites.

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REFERENCES

- [1] International Technology Roadmap for Semiconductors, 2008.
- [2] M. Hauschildt, M. Gall, S. Thrasher, P. Justison, R. Hernandez, et al., "Statistical Analysis of Electromigration Lifetimes and Void Evolution," *J. Appl. Phys.*, vol. 101, pp. 043523-1 – 043523-9, 2007.
- [3] L. Arnaud, T. Berger, and G. Reimbold, "Evidence of Grain Boundary versus Interface Diffusion in Electromigration Experiments in Copper Damascene Interconnects," *J. Appl. Phys.*, vol. 93, pp. 192 – 204, 2003.
- [4] M.R. Sorensen, Y. Mishin, and A.F. Voter, "Diffusion Mechanisms in Cu Grain Boundaries," *Phys. Rev. B*, vol. 62, pp. 3658 – 3673, 2000.
- [5] R.W. Balluffi, "Grain Boundary Diffusion Mechanisms in Metals," *Metall. Trans. A*, vol. 13A, pp. 2069 – 2095, 1982.
- [6] R. Rosenberg and M. Ohring, "Void Formation and Growth during Electromigration in Thin Films," *J. Appl. Phys.*, vol. 42, pp. 5671 – 5679, 1971.
- [7] H. Ceric, R.L. de Orio, J. Cervenka, and S. Selberherr, "A Comprehensive TCAD Approach for Assessing Electromigration Reliability of Modern Interconnects," *IEEE Trans. Mat. Dev. Rel.*, vol. 9, pp. 9 – 19, 2009.
- [8] M.E. Sarychev, Y.V. Zhitnikov, L. Borucki, C.L. Liu, and T.M. Makhviladze, "General Model for Mechanical Stress Evolution During Electromigration," *J. Appl. Phys.*, vol. 86, pp. 3068 – 3075, 1999.
- [9] R.J. Gleixner, B.M. Clemens, and W.D. Nix, "Void Nucleation in Passivated Interconnect Lines: Effects of Site Geometries, Interfaces, and Interface Flaws," *J. Mater. Res.*, vol. 12, pp. 2081 – 2090, 1997.

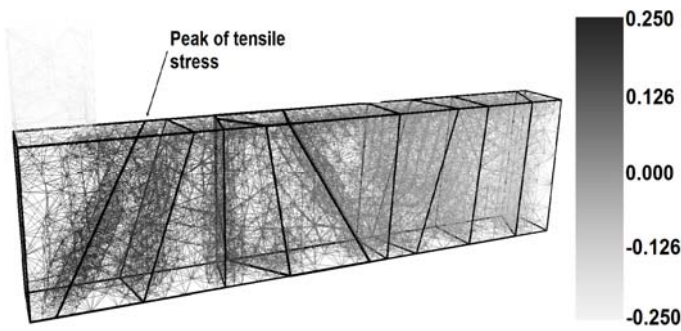


Fig. 5. Hydrostatic stress distribution in a simulated interconnect (in MPa). The peak value is located at grain boundaries, where vacancies are trapped.

Nevertheless, our results show that the microstructure can still affect the electromigration lifetimes by providing sites of flux divergence and grain boundaries as fast diffusivity paths, so that the lifetimes clearly follow lognormal distributions, as presented in Fig. 6. Moreover, as the standard deviation of the distribution of grains sizes increases, we observed an increase of the standard deviation of the electromigration lifetime distribution, as shown in Fig. 7. These results strongly imply that the lognormal grain size distribution is the primary cause for the lognormal distribution of the electromigration lifetimes.

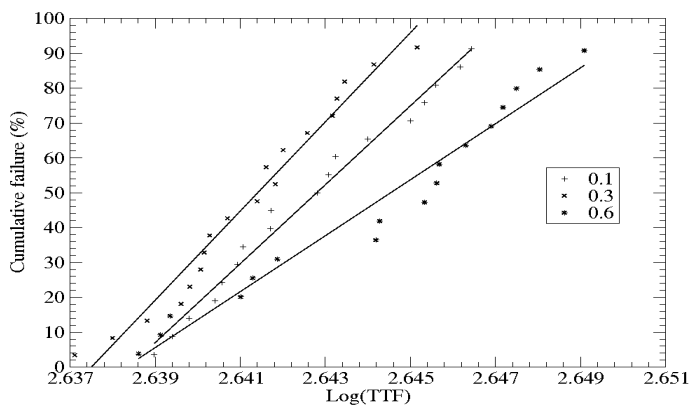


Fig. 6. Electromigration lifetime distributions for different standard deviations for the grain size distribution.

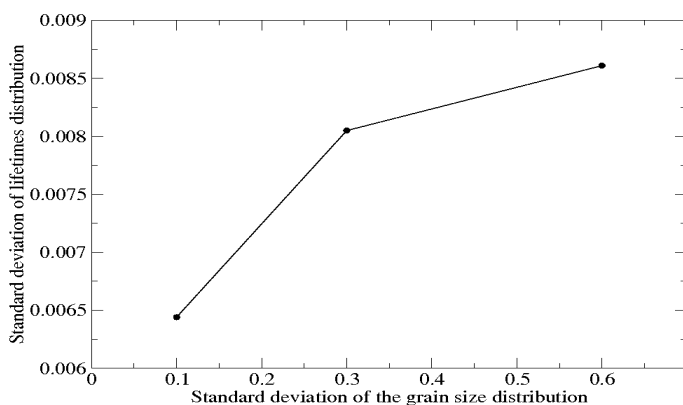


Fig. 7. Electromigration lifetime standard deviation for different standard deviations of grain size.