Electromigration Failure Development in Modern Dual-Damascene Interconnects

Roberto Lacerda de Orio, Hajdin Ceric, Johann Cervenka, and Siegfried Selberherr
Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, A-1040 Wien, Austria
Email: {orio|ceric|cervenka|selberherr}@iue.tuwien.ac.at

***Abstract*— The electromigration failure development in typical copper dual-damascene interconnect structures is analyzed based on numerical simulations. The origin of the lognormal distribution of electromigration times to failure is investigated. Also, electromigration-induced void formation and evolution in advanced 0.18 μm dual-damascene lines are simulated and the results are compared with experiments. It is shown that the lognormal distribution of the grain sizes leads to lognormal distributions of the electromigration lifetimes. Moreover, the void nucleation sites and main features of void development are highly dependent on the microstructure of the interconnect lines.**

I. Introduction

According to the International Technology Roadmap for Semiconductors (ITRS) 2008 Update [1] the copper dual-damascene technology process will continue to be applied for the fabrication of on-chip interconnects for the next technological nodes. The metal wiring pitch in microprocessors will shrink down to 64 nm for the 32 nm node, and 44 nm for the 22 nm node. At the same time, the expected operating current densities can reach 2.11 MA/cm^2 and 2.80 MA/cm^2, respectively.

The continuous shrinking of the dimensions of on-chip interconnects and the introduction of advanced backend-of-line (BEoL) manufacturing process steps increases the complexity of physical phenomena behind electromigration failure. The total wiring length amounts to kilometers arranged in several levels of metalizations with millions of interlevel connections. The tendency of modern technologies to increase the interconnect length and, at the same time, reduce the cross section, makes the interconnect structures more and more susceptible to electromigration. Currently, integrated circuits are often designed using simple and conservative design rules to ensure that the resulting circuits meet reliability goals. However, this precaution leads to reduced performance for a given circuit and metalization technology.

Experiments have shown that electromigration times to failure follow a lognormal distribution [2]. Although the origin of such a distribution is not entirely clear, it has been argued that the diffusion process in connection with the effect of microstructure on electromigration provides the basis for the lognormal distribution [3]. In copper dual-damascene interconnects the main diffusivity path is along the copper/capping layer interface. This interfacial diffusion is affected by the orientation of the grains. As the copper grain sizes seem to follow lognormal distributions in typical dual-damascene process technology [3] and due to the influence of microstructure on the electromigration process, the lognormal distribution has been used as the underlying statistics for electromigration lifetimes. However, it has been discussed whether this choice is the most appropriate [4]. The understanding of the electromigration lifetime distribution is crucial for the extrapolation of the times to failure obtained empirically from accelerated tests to real operating conditions, as performed by a modified form of the Black equation [2].

Also, the microstructure plays a key role regarding the failure mechanisms in copper dual-damascene interconnects [5] and affects electromigration in different ways. They are natural locations of atomic flux divergence, they act as fast diffusivity paths for vacancy diffusion [6], and grain boundaries act as sites of annihilation and production of vacancies [7].

The main challenge in electromigration modeling and simulation is the diversity of physical phenomena which have to be taken into account for an adequate description of the problem. Electromigration transport is also accompanied by material transport driven by the gradients of material concentration, mechanical stress, and temperature. Furthermore, taking into account the effects of interfaces and grain boundaries as fast diffusivity paths imposes new challenges for electromigration modeling.

In this work we analyze the electromigration failure development in typical copper dual-damascene interconnect structures based on numerical simulations. We investigate the origin of the statistical distribution of electromigration times to failure as a function of the distribution of copper grain sizes. Moreover, electromigration-induced void formation and evolution in advanced 0.18 μm dual-damascene lines are simulated and the results are compared with experiments.

II. Electromigration Model

Several driving forces are responsible for the vacancy transport in a conductor line under electromigration. The combination of these driving forces leads to the total vacancy flux given by

$$\vec{J}_v = -D_v\left(\nabla C_v + \frac{|Z^*e|}{k_BT}C_v\nabla\varphi + \frac{f\Omega}{k_BT}C_v\nabla\sigma\right), \qquad (1)$$

where D_v is the vacancy diffusion coefficient of the dominant transport path, C_v is the vacancy concentration, Z^*e is the effective charge, f is the vacancy relaxation ratio, Ω is the atomic volume, σ is the hydrostatic stress, k_B is Boltzmann's constant, and T is the temperature.

Vacancies accumulate or vanish in sites of flux divergence, and this dynamics is described by the continuity equation

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G(C_v), \tag{2}$$

where $G(C_v)$ is the source function which models vacancy generation and annihilation processes [8]. The source term $G(C_v)$ plays a major role for the mechanical stress buildup and is taken into account only at interfaces and grain boundaries. It comprises three processes, namely, the exchange of point defects between adjacent grains, the exchange of point defects between grains and grain boundaries, and the formation/annihilation of point defects at grain boundaries.

In our model the grain boundary is treated as a separate region which can trap or release vacancies [9], as shown in Fig. 1. We denote the vacancy concentration from both sides of the grain boundary as C_v^1 and C_v^2, respectively, and the concentration of immobile vacancies which are trapped inside the grain boundary as C_v^{im}.

The trapping rate of vacancies at the grain boundary, which corresponds to the generation/recombination rate, is controlled by the atomic fluxes J_v^1 and J_v^2, yielding [9]

$$\frac{\partial C_v^{im}}{\partial t} = G = \frac{1}{\tau}\Big[C_v^{eq} - C_v^{im}\Big(1 + \frac{2\,\omega_R}{\omega_T(C_v^1 + C_v^2)}\Big)\Big], \tag{3}$$

where ω_T is the trapping rate of vacancies from the neighboring grains, ω_R is the release rate, and C_v^{eq} is the equilibrium vacancy concentration inside the grain boundary, given by

$$C_v^{eq} = C_v^0 \exp\Big(\frac{\sigma_{nn}\Omega}{k_B\,T}\Big), \tag{4}$$

where C_v^0 is the equilibrium vacancy concentration in the absence of stress and σ_{nn} is the stress component normal to the grain boundary. Eq. (3) shows that grain boundaries act as source/sinks of vacancies provided that the concentration of trapped vacancies deviates from the equilibrium one. τ represents the vacancy relaxation time and it characterizes the efficiency of the grain boundary as vacancy sink/source [9]

$$\frac{1}{\tau} = \frac{\omega_T(C_v^1 + C_v^2)}{\delta}. \tag{5}$$

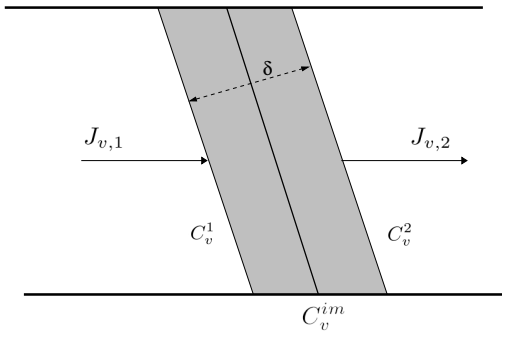

Fig. 1. Grain boundary model.

Sarychev *et al.* [10] introduced the contribution of vacancy migration and generation/annihilation processes for stress build-up in a three-dimensional model of stress evolution during electromigration. Considering the grain boundary model we have proposed that the strain growth from both sides of the grain boundary is proportional to the growth rate of immobile vacancies

$$\frac{\partial \varepsilon_{kk}}{\partial t} = \Omega\Big[(1-f)\nabla \cdot \vec{J}_v + f\frac{\partial C_v^{im}}{\partial t}\Big], \tag{6}$$

where ε_{kk} is the trace of the strain vector.

Equation (6) shows that vacancies trapped at the grain boundaries are responsible for build-up of tensile stress. When the grain boundaries are able to capture large amounts of vacancies, a high tensile stress develops.

Flinn [11] showed that void nucleation due to vacancy condensation is not expected to occur. He suggests that flaws at the metal/capping layer interface may provide a mechanism with a low energy barrier for void formation. Based on this work Clemens *et al.* [12] and Gleixner *et al.* [13] show that the stress threshold required for void nucleation at some weak adhesion point is given by

$$\sigma_{th} = \frac{2\gamma_s \sin\theta_c}{R_p}, \tag{7}$$

where R_p is the radius of the adhesion-free patch, θ_c is the contact angle between the void and the surface, and γ_s is the surface energy. If we assume the adhesion free patch with a radius of 10 nm (about 20 atoms) and $\theta_c = \pi/2$, we obtain $\sigma_{th} \sim 344$ MPa [9].

As a void is nucleated in the interconnect line, a new phase of failure development starts, the void evolution phase. An evolving void surface is shaped by two dynamic forces, namely the chemical potential gradient and the electron wind. Including both contributions, the total surface vacancy flux is [14]

$$\vec{J}_s = J_s\vec{t} = -D_s\Big[|eZ^*|\vec{E}_s + \Omega\nabla_s\Big(\frac{\sigma:\varepsilon}{2} - \gamma_s\kappa\Big)\Big], \tag{8}$$

where $\vec{t}$ is the unit vector tangential to the void surface, $\vec{E}_S = E_s\vec{t}$ is the local component of the electric field tangential to the void surface, ∇_s is the surface gradient operator, $1/2\,(\sigma:\varepsilon)$ is the strain energy density of the material adjacent to the void surface, and κ is the curvature of the void surface. D_s is given by an Arrhenius law

$$D_s = \frac{D_0\,\delta_s}{k_B\,T\Omega}\exp\Big(-\frac{Q_s}{k_B\,T}\Big), \tag{9}$$

where δ_s is the thickness of the diffusion layer, Q_s is the activation energy for the surface diffusion, and D_0 is the pre-exponential coefficient for mass diffusion.

III. Numerical Approach

Equations (1–7) are solved using the finite element method (FEM) until the stress threshold for void nucleation is reached at some weak adhesion point. We consider the intersection of grain boundaries with the copper/capping layer interface as natural places of weak adhesion [15]. As grain boundaries and interfaces act as fast diffusivity paths, the diffusion coefficient in (1) has to be adapted for these regions. We have used $D_v^{gb} = 10^4 D_v^{bulk}$ for grain boundaries and $D_v^{Cu-cap} = 10^5 D_v^{bulk}$ for the copper/capping layer interface [16]. It should be pointed out that all model parameters are equal for all grains and all simulated structures. Grain boundaries, and generally, all interfaces of the problem geometry have to be supplied with an appropriately fine FEM mesh. This is necessary in order to provide sufficient resolution for the local dynamics described by the proposed model.

The void evolution equations are solved using the Level Set Method [17]. The evolving surface of the void is implicitly represented by a level set function ϕ, which is governed by the Hamilton-Jacobi equation

$$\frac{\partial \phi}{\partial t} + v_n \|\nabla \phi\| = 0, \tag{10}$$

where $v_n = \nabla_s \cdot \vec{J}_s$ is the speed function which describes the evolution of the level set and, consequently, the void development.

In order to include the grain distribution in our numerical simulations, a microstructure generator tool has been developed. Given a specific interconnect structure and providing the tool with a median grain size and corresponding standard deviation, it generates a lognormal distribution of grain sizes. Then, following this distribution, the interconnect line is cut along its length by the planes that form the grain boundaries. Furthermore, the angles between the grain boundaries' planes and the line surface follow a normal distribution with median value of 90°.

IV. Results and Discussion

A. Electromigration Lifetimes Distribution

In order to evaluate the impact of the microstructure statistics on the electromigration lifetimes, three standard deviations for the distribution of grain sizes are considered, namely 0.1, 0.3 and 0.6. For each of them 20 dual-damascene interconnect structures were created using the microstructure generator. In Fig. 2 we present the schema of the simulation procedure. As the interconnect line is assumed to present a bamboo-like structure, the median grain size is equal to the line width, 0.10 μm. In these simulations, the barrier, capping and interlayer dielectric layers are Ta, SiN, and SiO_2, respectively. The applied current density is 1.5 MA/cm^2, and the temperature is 300 °C.

Fig. 3 shows the hydrostatic stress development for the structures with grain size standard deviation of 0.3. Collecting the times to failure from Fig. 3 and calculating the cumulative

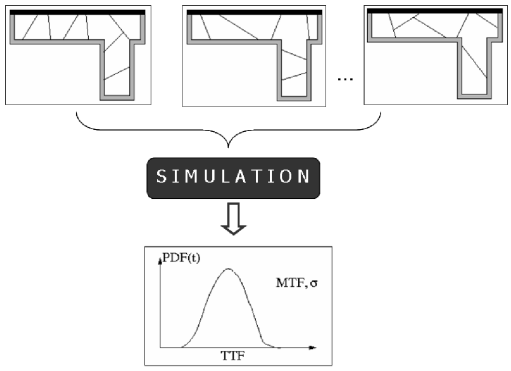

Fig. 2. Schematic simulation procedure.

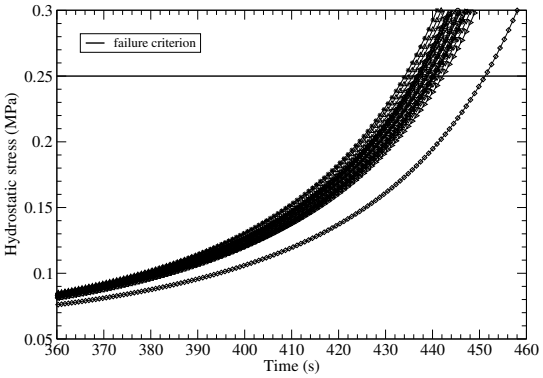

Fig. 3. Peak of hydrostatic stress development for the set with grain size standard deviation of 0.3.

failure percentages results in the distributions of electromigration lifetimes shown in Fig. 4. The lifetimes are fitted by lognormal distributions. The obtained standard deviations are 0.0065, 0.0080, and 0.0085 for the grain size distributions with standard deviations of 0.1, 0.3, and 0.6, respectively.

The standard deviations for the electromigration lifetimes are rather small compared to those frequently observed in experiments [2]. Several factors can explain this behavior. First, for convenience, we have used a small value of stress threshold as failure criterion to determine the interconnect lifetime. As can be seen from Fig. 3, the variation of the lifetimes can be more pronounced for higher stress thresholds. Second, the simulation parameters and material properties are independent of the grain distribution. This means that mechanical properties and diffusivities are equal and constant for all grains in an interconnect line, for all simulated structures. This is clearly not the case in real experiments, as it is well known that material properties vary not only from line to line but also according to the grain orientation. It is expected that atomic diffusion along the copper/capping layer interface changes from grain to grain, inducing a flux divergence at the corresponding grain boundary. Moreover, the diffusivities are different from line to line as the grain distribution varies. Therefore, given the simplifications we have made, the small standard deviations we have obtained should be expected.

Nevertheless, our results show that the grain distribution still affects the electromigration lifetime distribution. When the grain size distribution exhibits a smaller standard deviation the corresponding interconnect lines have a more uniform distribution of the grains. As a consequence, the stress build-up has smaller variations yielding a smaller standard deviation of the electromigration lifetimes. On the other hand, increasing the grain size standard deviation, the lines exhibit significant differences in the grain structures. This leads to increased variations for the stress development. Thus, a bigger standard deviation of electromigration lifetimes is expected. This behavior is presented in Fig. 5. It shows that the increase of the standard deviation of the distribution of grains sizes increases the standard deviation of the electromigration lifetime distribution.

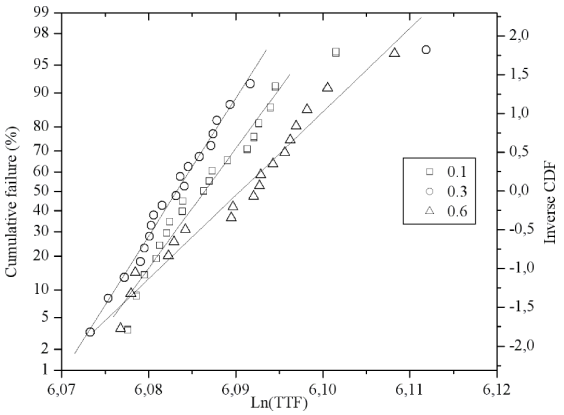

Fig. 4. Electromigration lifetime distributions.

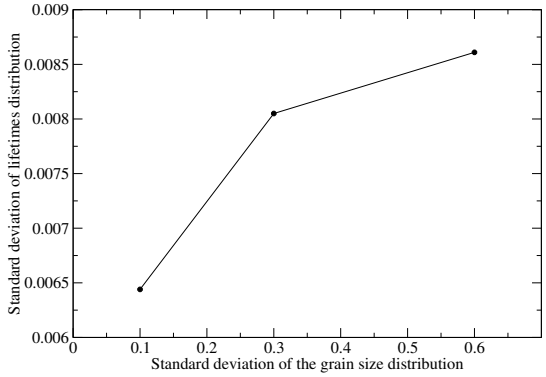

Fig. 5. Electromigration lifetime standard deviation for different standard deviations of grain size.

B. Void Nucleation and Evolution

In this analysis all parameters for simulation are set according to experiments published in [18]. The line width is 0.18 μm, the applied current density is 1.5 MA/cm^2, and the temperature is 300 °C. Barrier and capping layers are Ta/TaN and SiCN, respectively. SiOC is used as passivation layer.

Fig. 6 shows the hydrostatic stress distribution along the interconnect line. Peaks of electromigration-induced stress

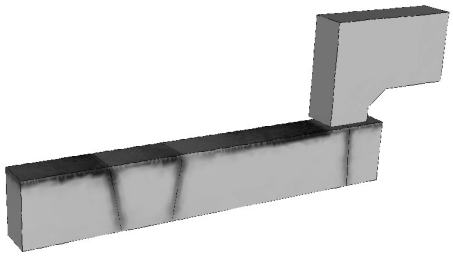

Fig. 6. Peak hydrostatic tensile stress distribution (dark areas) caused by electromigration.

develop at triple-points formed by the grain boundaries and the copper/capping layer interface. Once the stress reaches the threshold σ_{th}, a small spherical void is set at the corresponding triple point location, as shown in Fig. 7, and the Hamilton-Jacobi equation (10) is solved.

After the void is nucleated, it moves in the direction of the electric current flow. As the void encounters the second grain boundary, it receives an additional flux of vacancies. Therefore, the void develops further, goes through a shape change process, and grows through the line. As the void grows the local cross section for electric current flow decreases, which leads to a significant increase of the interconnect resistance. The void development process is shown in Fig. 8 and Fig. 9.

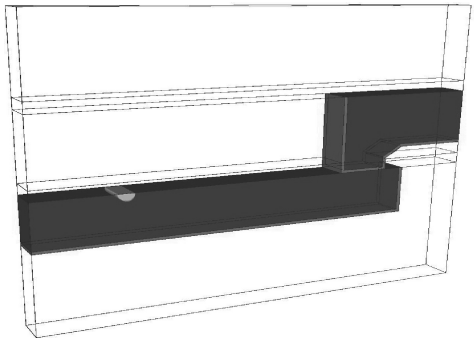

Fig. 7. Initial void placed at the nucleation site.

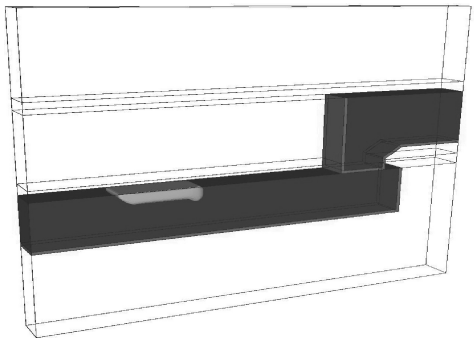

Fig. 8. The void moves and encounters the second grain boundary.

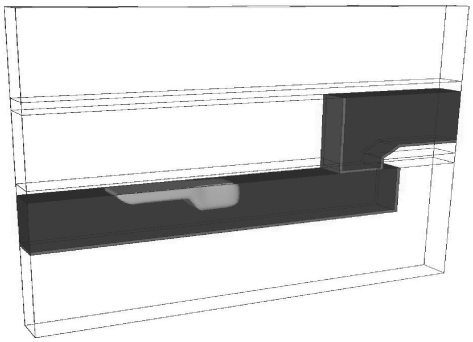

Fig. 9. Void shape changes as it drifts toward the via.

The results of simulations and experiments demonstrate a decisive impact of the microstructure on the failure development [18]. The void first nucleates at a triple point, then grows and changes its shape, leading to the interconnect failure. A detailed view of the fatal void is shown in Fig. 10. For comparison, a FIB cross section of an interconnect after an electromigration test is shown in Fig. 11. The experimental result clearly documents that the applied models, together with the assumed microstructure, satisfactorily reproduce the observed void dynamics.

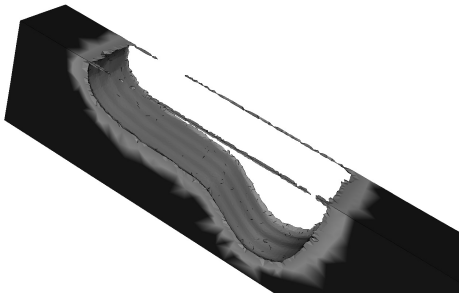

Fig. 10. Detail of the final void shape.

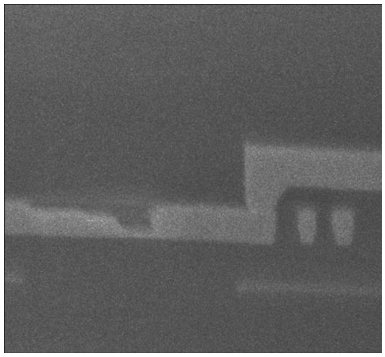

Fig. 11. FIB cross section of interconnect after an electromigration test [18] (courtesy of Dr. Lucille Arnaud).

V. Conclusion

We analyzed the electromigration failure development in typical copper dual-damascene interconnect structures based on numerical simulations. A detailed study of vacancy dynamics and stress build-up in connection with the microstructure is presented. Our results indicate that the lognormal distribution of the copper grain sizes is a primary cause for the lognormal distributions of the electromigration lifetimes. Moreover, a close investigation of the effect of microstructure on void nucleation and evolution has shown that the network of grain boundaries has a decisive impact on the determination of void nucleation sites and of void development.

Acknowledgment

This work has been supported by the European Community with the project PULLNANO (contract no 026828) and the Austrian Science Fund with the project P18825-N14.

References

[1] *International Technology Roadmap for Semiconductors*, 2008.

[2] M. Hauschildt, M. Gall, S. Thrasher, P. Justison, R. Hernandez, H. Kawasaki, and P. S. Ho, "Statistical Analysis of Electromigration Lifetimes and Void Evolution," *J. Appl. Phys.*, vol. 101, p. 043523, 2007.

[3] M. Hauschildt, "Statistical Analysis of Electromigration Lifetimes and Void Evolution in Cu Interconnects," Dissertation, The University of Texas at Austin, 2005.

[4] J. Lloyd and J. Kitchin, "The Electromigration Failure Distribution: The Fine-Line Case," *J. Appl. Phys.*, vol. 69, no. 4, pp. 2117–2127, 1991.

[5] L. Arnaud, T. Berger, and G. Reimbold, "Evidence of Grain-Boundary Versus Interface Diffusion in Electromigration Experiments in Copper Damascene Interconnects," *J. Appl. Phys.*, vol. 93, no. 1, pp. 192–204, 2003.

[6] M. R. Sorensen, Y. Mishin, and A. F. Voter, "Diffusion Mechanisms in Cu Grain Boundaries," *Phys. Rev. B*, vol. 62, no. 6, pp. 3658–3673, 2000.

[7] R. W. Balluffi, "Grain Boundary Diffusion Mechanisms in Metals," *Metall. Trans. A*, vol. 13, pp. 2069–2095, 1982.

[8] R. Rosenberg and M. Ohring, "Void Formation and Growth During Electromigration in Thin Films," *J. Appl. Phys.*, vol. 42, no. 13, pp. 5671–5679, 1971.

[9] H. Ceric, R. L. de Orio, J. Cervenka, and S. Selberherr, "A Comprehensive TCAD Approach for Assessing Electromigration Reliability of Modern Interconnects," *IEEE Trans. Mat. Dev. Rel.*, vol. 9, no. 1, pp. 9–19, 2009.

[10] M. E. Sarychev, Y. V. Zhitnikov, L. Borucki, C. L. Liu, and T. M. Makhviladze, "General Model for Mechanical Stress Evolution During Electromigration," *J. Appl. Phys.*, vol. 86, no. 6, pp. 3068–3075, 1999.

[11] P. A. Flinn, "Mechanical Stress in VLSI Interconnections: Origins, Effects, Measurement, and Modeling," *MRS Bulletin*, pp. 70–73, 1995.

[12] B. M. Clemens, R. J. Gleixner, and W. D. Nix, "Void Nucleation On a CFontaminated Patch," *J. Mater. Res.*, vol. 12, pp. 2038–2042, 1997.

[13] R. J. Gleixner, B. M. Clemens, and W. D. Nix, "Void Nucleation in Passivated Interconnect Lines: Effects of Site Geometries, Interfaces, and Interface Flaws," *J. Mater. Res.*, vol. 12, pp. 2081–2090, 1997.

[14] D. N. Bhate, A. Kumar, and A. F. Bower, "Diffuse Interface Model for Electromigration and Stress Voiding," *J. Appl. Phys.*, vol. 87, no. 4, pp. 1712–1721, 2000.

[15] A. V. Vairagar, S. G. Mhaisalkar, A. Krishnamoorthy, K. N. Tu, A. M. Gusak, M. A. Meyer, and E. Zschech, "In Situ Observation of Electromigration-Induced Void Migration in Dual-Damascene Cu Interconnect Structures," *Appl. Phys. Lett.*, vol. 85, no. 13, pp. 2502–2504, 2004.

[16] V. Sukharev, E. Zschech, and W. D. Nix, "A Model for Electromigration-Induced Degradation Mechanisms in Dual-Inlaid Copper Interconnects: Effect of Microstructure," *J. Appl. Phys.*, vol. 102, no. 053505, 2007.

[17] J. A. Sethian, *Level Set Methods and Fast Marching Methods: Evolving Interfaces in Computational Geometry, Fluid Mechanics, Computer Vision and Materials Science*. Cambridge University Press, 1999.

[18] L. Doyen, E. Petitprez, P. Waltz, X. Federspiel, L. Arnaud, and Y. Wouters, "Extensive Analysis of Resistance Evolution due to Electromigration-Induced Degradation," *J. Appl. Phys.*, vol. 104, p. 123521, 2008.