

Analysis of Electromigration in Dual-Damascene Interconnect Structures

R. L. de Orío^a, S. Carniello^b, H. Ceric^a, and S. Selberherr^a

^a Institute for Microelectronics, TU Wien, Gußhausstr. 27–29, A-1040 Vienna, Austria

^b austriamicrosystems AG, Schloss Premstätten, A-8141 Unterpremstätten, Austria

We have analyzed the stress build-up and vacancy dynamics due to material transport caused by electromigration in dual-damascene interconnect structures. Our model incorporates all relevant driving forces for material transport with a complete integration of mechanical stress in connection with microstructural aspects. First, it is shown that the addition of redundant vias can be effective in increasing the interconnect lifetime, although the spacing between the vias can have a significant impact on such an approach. Then, we discuss the importance of grain boundaries in providing triple point intersections, where the combination of high vacancy concentration and high stress is likely to cause void nucleation.

Introduction

Electromigration is one of the main reliability issues in modern integrated circuits, which can trigger system failure at some undefined future time. The phenomenon is particularly likely to afflict the thin, tightly spaced interconnect lines of deep-submicron designs.

Blech (1, 2) was one of the first to explain the origin of the electromigration phenomena. In his experiments he discovered a critical product of interconnect line length and current density, below which no electromigration failure is observed. Kirchheim (3) proposed a physically based model in which the generation of stress in the grain boundaries during electromigration is caused by annihilation and generation of vacancies. Korhonen (4) proposed another physics based analytical model for mechanical stress evolution during electromigration in a confined metal line described by a one-dimensional equation.

Since electromigration has been recognized as an important risk for interconnect reliability, engineers have been thinking about strategies for reducing or completely eliminating its effect. Independent of interconnect technology, there are basically two possibilities how to contest electromigration. The first one is choosing the appropriate materials or combination of these materials to produce preferable properties. Such efforts led from originally aluminum interconnects to aluminum-copper alloys, and later to pure copper interconnects. This material design for reliability also encompasses the choice of materials which surround the interconnect metal. The second strategy to control electromigration behavior is the introduction of special geometrical features. The basic idea is to avoid material dwindling due to material transport in specific interconnect structures. The most widely applied examples of such strategies are material reservoirs (5) and redundant vias (6-8).

There exists a remarkable amount of experimental experience gained in designing electromigration resistant interconnect geometries (7), however, the complete understanding, why such geometrical features really enhance interconnect reliability, is still lacking or available only for simple situations. Using two or more via contacts between interconnect levels has shown to be a very promising geometrical strategy for preventing stress migration (6-8) and electromigration (7).

The effect of redundant vias has been more extensively studied for stress migration than for electromigration. The experiments have shown that stress migration failure is also determined by vacancy transport and mechanical stress build-up, however, the only driving force for material transport is the gradient of stress. The group of Yoshida *et al.* (8) was the first to closely investigate the effect of redundant vias on stress migration. In their work, no stress migration failure was detected, when two neighboring vias were used. This is because the nucleation of a void underneath the first via relaxes the stress also under the second one, suppressing the driving force for new void formation. Yoshida *et al.* (8) based their explanation on the concept of “active volume”, which is the intersection between the interconnect volume, the diffusion volume, and the stress gradient region, first introduced by Ogawa *et al.* (9).

The main challenge in electromigration modeling and simulation is the diversity of the relevant physical phenomena. Electromigration induced material transport is also accompanied by material transport driven by the gradients of material concentration, mechanical stress, and temperature distribution. A comprehensive, physics based analysis of electromigration for modern copper interconnect lines serves as the basis for deriving sophisticated design rules, which will ensure higher steadfastness of interconnects against electromigration.

In this work we present the results of our investigations on the physics of the redundant via approach, as well as the grain boundaries effects regarding the electromigration phenomenon. As a basis for our analysis a comprehensive, multiphysics model of electromigration and accompanying effects is used (10). Relying on previous works, our model reveals an improvement in two major points. First, there is a complete integration of the mechanical stress phenomena in connection with microstructural aspects in the classical multi-driving force model and, secondly, the developed finite element based scheme enables an efficient numerical solution of the three-dimensional formulation of the problem.

Electromigration Modeling

The transport of vacancies due to the gradient of vacancy concentration, electric field, gradient of temperature, and gradient of mechanical stress, respectively, is (11)

$$\vec{J}_v = -D_v \left(\nabla C_v + \frac{Z^* e}{k_B T} C_v \nabla \phi - \frac{Q^*}{k_B T^2} C_v \nabla T + \frac{f \Omega}{3 k_B T} C_v \nabla \text{tr}(\bar{\sigma}) \right), \quad [1]$$

where D_v is the vacancy diffusion coefficient, C_v is the vacancy concentration, $Z^* e$ is the effective charge, Q^* is the heat of transport, f is the vacancy relaxation ratio, Ω is the

atomic volume, $\bar{\sigma}$ is the stress tensor, k_B is Boltzmann's constant, and T is the temperature.

In sites of flux divergence, vacancies will accumulate or vanish, and this vacancy dynamics is described by the continuity equation (11)

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G(C_v), \quad [2]$$

where $G(C_v)$ is the source function which models vacancy generation and annihilation processes (12).

Sarychev *et al.* (11) introduced the contribution of the local vacancy dynamics to stress build-up in a three-dimensional model of stress evolution during electromigration, which is given in terms of strain by (13)

$$\frac{\partial \varepsilon_{kk}}{\partial t} = \Omega \left[(1-f) \nabla \cdot \vec{J}_v + fG(C_v) \right], \quad [3]$$

where ε_{kk} is the trace of the strain vector.

Void Nucleation Condition

From the early days of electromigration modeling, the void nucleation condition has been set based on the following two criteria:

- void nucleation after reaching a vacancy (atomic) concentration threshold (10, 14);
- void nucleation after reaching a tensile stress threshold (15, 16).

However, a careful investigation based on the classical nucleation theory has shown that these nucleation conditions, from a thermodynamic point of view, cannot be justified.

From the classical nucleation theory, in a strained single-phase material, a droplet of a second phase embryo is produced by spontaneous fluctuations, when the barrier energy ΔF^* , given by (17)

$$\Delta F^* = \frac{48\pi\gamma_m^3}{(tr(\bar{\sigma}))^2}, \quad [4]$$

for spherical embryos, is overcome. Here, γ_m is the surface free energy, and $\bar{\sigma}$ is the applied stress field. If we assume a rather high hydrostatic pressure of 1 GPa (18) and take 1.72 J/m² as the surface free energy of copper (19), we obtain an energy barrier of 133 eV. Then, the number of critical embryos per unit volume can be calculated by (17)

$$Z^* = \frac{1}{\Omega n^*} \left(\frac{\Delta F^*}{3\pi k_B T} \right)^{1/2} e^{-\frac{\Delta F^*}{k_B T}}, \quad [5]$$

where n^* is the number of vacancies in a critical embryo.

Critical embryos are spontaneously formed by the condensation of vacancies in stressed copper. However, the condensation process is reversible and, in most cases, the embryos completely dissolve in the surrounding lattice. The situation changes, when the critical embryo starts to accept additional free vacancies and the irreversible transition to an initial void is imminent (17). Then, the nucleation rate is calculated as

$$I = \nu e^{-\frac{U_D}{k_B T}} Z^* n_s^*, \quad [6]$$

where ν is the frequency of vibration of the atoms, U_D is the activation energy of the jump process, and n_s^* is the number of vacancies in the matrix at the surface of the critical embryo.

For copper, the nucleation rate in the metal bulk is $I \sim 10^{-1396} \text{ m}^{-3} \text{ s}^{-1}$. The nucleation rate dependence on temperature/stress is presented in Fig. 1. Similar values can be obtained for nucleation at the interconnect sidewall, grain boundaries, and sidewall/grain boundary intersection. This means that a void nucleation by means of vacancy condensation for both, accelerated test conditions and realistic use conditions, is not possible.

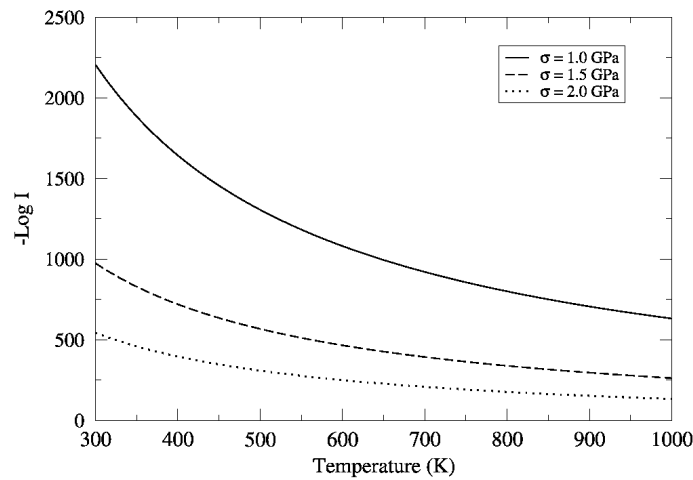


Figure 1. Nucleation rate dependence on hydrostatic stress and temperature. Even a very high temperature can not significantly increase the nucleation rate.

An analysis carried out in (20) set a new framework for the understanding of void nucleation. The author considers a circular patch on the interface between copper and the capping layer with virtually no adhesion. Such an entity can actually be the product of a surface defect or contamination (21). As the stress in the line increases, the free metal

surface is driven to accommodate a half-spherical void embryo. The stress threshold given by Clemens *et al.* (22), and Glaixner *et al.* (18) is

$$\sigma_{th} = \frac{2\gamma_m \sin \theta_c}{R_p}, \quad [7]$$

where R_p is the radius of the adhesion-free patch and θ_c is the equilibrium contact angle between the void and the sidewall.

For stresses $\sigma < \sigma_{th}$ an energy barrier exists between the embryo and a stable-growing void. If the stress is above the threshold value ($\sigma > \sigma_{th}$) the free energy monotonically decreases with the void volume and the energy barrier vanishes. If we now assume the adhesion free patch with a radius of 10 nm, approximately 20 atoms, and $\theta_c = \pi/2$, we obtain $\sigma_{th} \sim 344$ MPa. Such a stress level can already be reached by thermal stress (23) in modern interconnects.

Simulation Procedure

The model presented by the set of equations [1]–[3] is numerically solved by the finite element method implemented in an in-house code for three-dimensional structures. The solving algorithm is depicted in Fig. 2. Each model is handled according to a unique priority list, starting with the electro-thermal problem, which is the coupled system of the Laplace and the Fourier equation. Then, the material transport equations [1], [2] are solved and, finally, the corresponding stress is determined via Eq. [3]. As Fig. 2 shows, the calculated attributes are transferred from the model of higher priority to the model of lower priority.

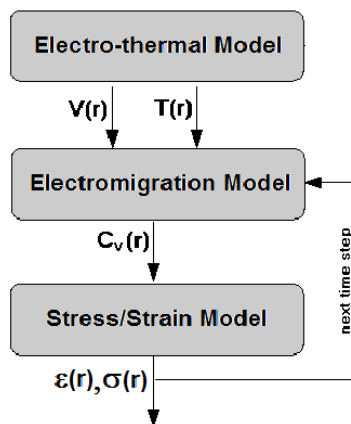


Figure 2. The complete solving procedure. The electromigration and the mechanical problem are solved each time step.

Results and Discussion

Fig. 3 and Fig. 4 show the hydrostatic stress distribution for the single via structure and the redundant via structure, respectively. The electron flow is from the upper to the lower metal line (downward flow), and therefore vacancies accumulate right under the via region at the lower line. As the vacancy has a smaller volume than the metal atom, the accumulation of vacancies in this region leads to the production of local tensile stresses. We have observed that the stress developed under the left via for the structure with the redundant via is higher than that for the single via. The addition of the second via reduces the interconnect resistance and increases the electrical current. Consequently, the driving force for material transport along the line is increased, and more vacancies concentrate under the left via of the redundant via structure, producing a higher stress.

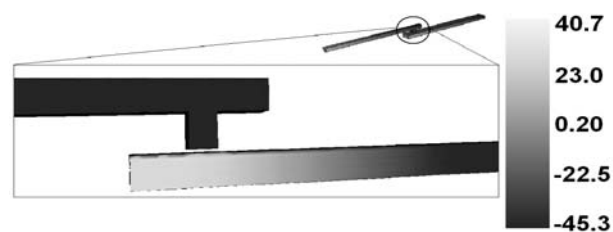


Figure 3. Detail of the hydrostatic stress in a single via interconnect structure.

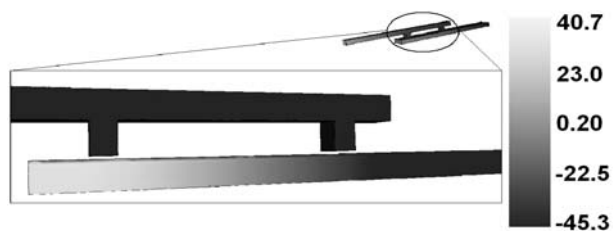


Figure 4. Detail of the hydrostatic stress in a redundant via interconnect structure.

The stress build-up for structures with different distances between the redundant vias is shown in Fig 5. The comparison between the redundant and single via structure clearly indicates that the addition of a redundant via leads to higher stresses. The stress increases as the distance between the vias becomes larger. These results suggest that a void nucleates sooner for the redundant via structures, but the associated stress relaxation hinders a void nucleation under the second via, and an increase in the interconnect mean time to failure is observed (7, 8).

In Fig. 6 the stress values under the vias are compared as a function of the distance between them. It is remarkable that the stress decrease under the right via is much more pronounced than the stress increase under the left via. As for small distances the stress magnitudes under both of the vias are very similar, a void could nucleate in either the left or the right via. However, increasing the distance the right via stress is significantly reduced and it can be expected that a void nucleates only under the left via.

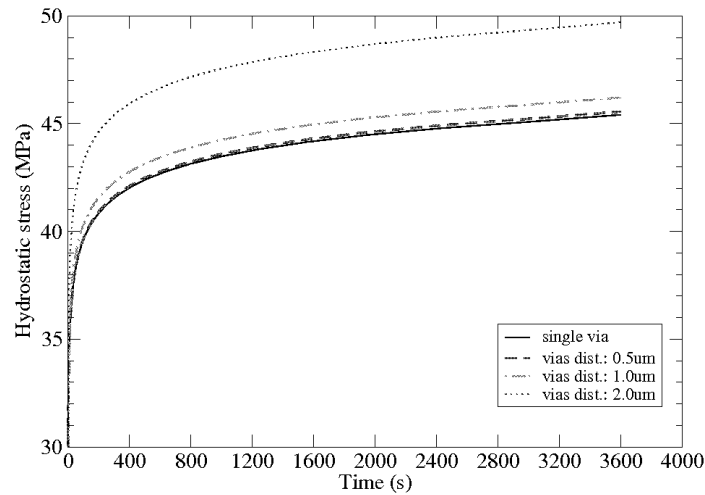


Figure 5. Maximum hydrostatic stress under the left via developed with time for different distances between the vias.

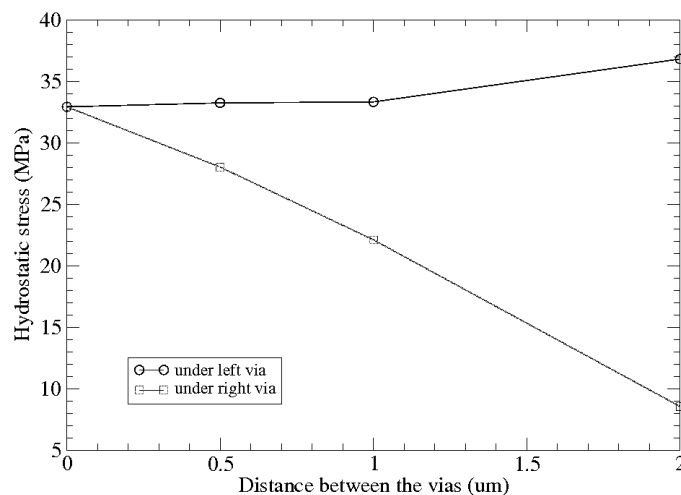


Figure 6. Hydrostatic stress under the vias as a function of the vias distance. The stress for the single via case is given at zero distance between the vias.

When a void nucleates under the right via, its subsequent growth can span the lower line thickness leading to the interruption of electrical current flow in the line, and the interconnect fails even with the redundant via. As increasing the distance between the vias allows the void to nucleate only under the left via, even if it spans the whole line thickness, the failure is not observed, because the right via still serves as a path for current conduction (7).

Changing the direction of the electrical current, the electron flow will be from the lower to the upper metal line (upward flow), the corresponding maximum stress build-up and vacancy concentration in the upper metal line are given in Fig. 7 and Fig. 8, respectively. First, we can observe that the developed stresses are higher than those

produced for the downward electron flow, due to the higher current density in the upper line. Second, the addition of a redundant via results in a stress decrease. This behavior is the opposite to that observed for the downward flux. Fig. 9 and Fig. 10 show the vacancy distribution in the single via structure and in the redundant via structure in the case of upward flux. We can see that the vacancy concentration in the single via structure is higher.

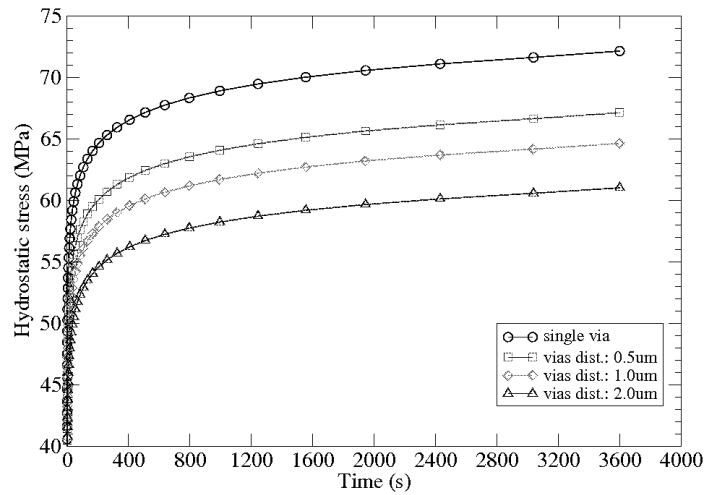


Figure 7. Hydrostatic stress build-up in the upper interconnect line for different distances between the vias.

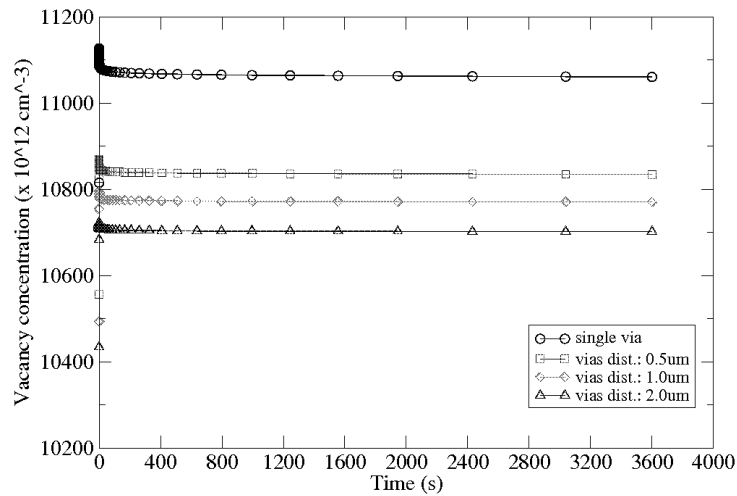


Figure 8. Maximum vacancy concentration in the upper metal line developed with time for different distances between the vias.

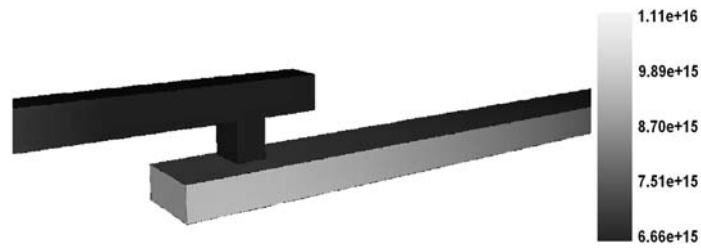


Figure 9. Vacancy distribution for the single via structure (units in cm^{-3}).

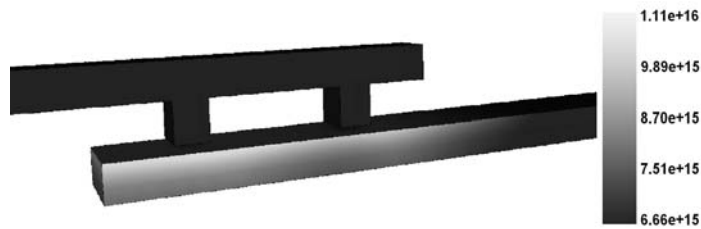


Figure 10. Vacancy distribution for the structure with redundant vias (units in cm^{-3}).

These figures suggest that the vias share the distribution of vacancies in the redundant via structure, which reduces the maximum vacancy concentration, as shown in Fig. 8, therefore reducing the stress. Such a behavior is similar to that observed by Huang *et al.* (6) in a study of stress migration, in the sense that the addition of a redundant via provides another destination for the migrating vacancies. Since in our studies of electromigration transport the maximum stress is always located in the right via region, even if a void nucleates and grows until it spans this via, the left via is not affected. Therefore the interconnect failure does not occur.

We have applied the model presented in this work to an interconnect layout which has been extensively used for accelerated electromigration tests (24). This layout, as shown in Fig. 11, is typical for dual-damascene $0.18\ \mu\text{m}$ technologies. The copper microstructure has been set according to results of EBSD (Electron Backscatter Diffraction) measurements (25).

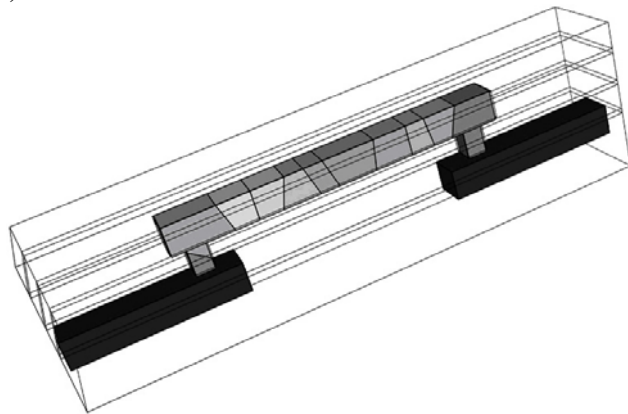


Figure 11. Three-dimensional interconnect structure with polycrystalline copper metalization.

The distribution of peak vacancy concentration and peak tensile stress for the initial time steps are presented in Fig. 12 and Fig. 13, respectively. We can see that the tensile stress tensor component σ_{yy} , which is orthogonal to the capping layer interface, reaches its peak value at the bottom of the via structure. However, high values can also be observed at the capping layer interface in the vicinity of triple point intersections with grain boundaries.

Under accelerated test conditions, as used in this example, high stresses at the triple points develop in the first hours of testing. As observed in experiments (24) carried out under operating conditions similar to our simulations, we have the first void nucleation in less than 2 hours. As previously discussed, a void can nucleate in places of local interface defects, where high tensile stress develops. According to our results, the coincidence of high vacancy concentration and high tensile stress values at triple points, such as the intersections between grain boundaries and capping layer, indicates that these regions are prone to void nucleation, as they are natural places of weak adhesion. In fact, reference (25) presents an EBSD map of a cross section of a copper dual-damascene test structure that clearly shows the presence of voids at such triple points.

The works (24, 25) show that voids initially nucleate at the interface between the copper and the capping layer far away from the cathode. Then, these voids migrate in the direction opposite to the electron flow, toward the cathode end of the line, where they agglomerate and coalesce to form a void which spans the line, causing the failure. Our results indicate that the scenario of weak triple points in combination with a stress threshold supports such a mechanism of multiple void nucleations. As Fig. 13 shows, peak tensile stress develops simultaneously at different intersections of grain boundaries and capping layer.

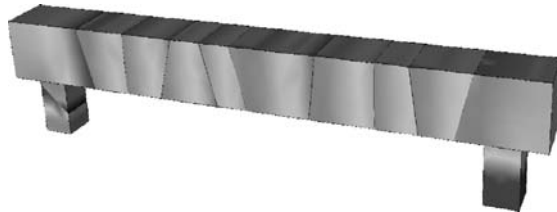


Figure 12. Vacancy distribution. Right is the cathode end of the interconnect.

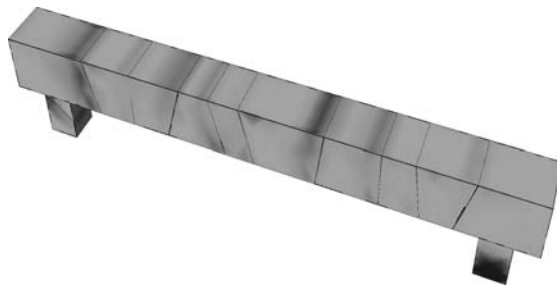


Figure 13. Peak tensile stress distribution for the σ_{yy} tensor component.

Conclusion

We presented an electromigration model which takes into account all relevant driving forces for material transport combined with microstructural aspects developed into a three-dimensional simulation tool.

We investigated the electromigration behavior in structures with redundant vias and with multi-grain metal lines.

It was shown that the application of a redundant via geometry can be effective in enhancing the interconnect reliability against electromigration failure. However, important differences have been observed depending on the direction of electron flow. For the upward flow, we have observed that the redundant via shares the vacancy distribution, reducing the vacancy concentration in the right via and, consequently, the stress. Moreover, if a void spans one of the vias, the other one still provides a path for current conduction, and the failure does not happen. Hence, the addition of redundant vias is a promising approach in order to increase the interconnect lifetime. On the other hand, in the case of downward electron flow, the results indicate that the spacing between the vias can affect the effectiveness of such an approach considerably. If the vias are too close to each other, it is possible that a void nucleates and grows until it spans the whole lower line, interrupting the current flow. Therefore, a proper design of redundant via structures is required to assure a gain on interconnect lifetime.

In the case of multi-grain lines, high vacancy concentration and high tensile stress develop at triple points, mainly at intersections between the grain boundaries and the capping layer. Based on the void nucleation analysis we have presented, such sites can be considered the most probable ones for void nucleation.

Acknowledgments

Support by the Austrian Science Fund with the project P18825-N14 is gratefully acknowledged.

References

1. I. A. Blech and C. Herring, *J. Appl. Phys.*, **29**, 131 (1976).
2. I. A. Blech and K. L. Tai, *Appl. Phys. Lett.*, **30**, 387 (1977).
3. R. Kirchheim, *Acta Metall. Mater.*, **40**, 309 (1992).
4. M. A. Korhonen, P. Borgesen, K. N. Tu, and C. Y. Li, *J. Appl. Phys.*, **73**, 3790 (1993).
5. E. T. Ogawa, K. D. Lee, V. A. Blaschke, and P. S. Ho, *IEEE Trans. on Reliability*, **51**, 403 (2002).
6. T. C. Huang, C. H. Yao, W. K. Wan, C. C. Hsia, and M. S. Liang, *Proc. Intl. Interconnect Technology Conf.*, p. 207 (2003).
7. A. von Glasow, *Zuverlässigkeitsaspekte von Kupfermetallisierungen in Integrierten Schaltungen*, Dissertation, Technische Universität München (2005).

8. K. Yoshida, T. Fujimaki, T. Miyamoto, T. Honma, H. Kaneko, H. Nakazawa, and M. Morita, *Digest. Intl. Electron Devices Meeting*, p. 753 (2002).
9. E. T. Ogawa, J. W. McPherson, J. A. Rosal, K. J. Dickerson, T. C. Chiu, L. Y. Tsung, M. K. Jain, T. D. Bonifield, J. C. Ondrusek, and W. R. McKee, *Proc. Intl. Reliability Physics Symp.*, p. 312 (2002).
10. V. Sukharev, R. Choudhury, and C. W. Park, *Integrated Reliability Workshop Final Report*, p. 80 (2003).
11. M. E. Sarychev, Y. V. Zhitnikov, L. Borucki, C. L. Liu, and T. M. Makhviladze, *J. Appl. Phys.*, **86**, 3068 (1999).
12. R. Rosenberg and M. Ohring, *J. Appl. Phys.*, **42**, 5671 (1971).
13. H. Ceric, R. Heinzl, C. Hollauer, T. Grasser, and S. Selberherr, *Stress-Induced Phenomena in Metallization*, AIP, p. 262 (2006).
14. O. Kraft and E. Arzt, *Acta Mater.*, **46**, 3733 (1998).
15. C. L. Gan, C. V. Thompson, K. L. Pey, W. K. Choi, H. L. Tay, B. Yu, and M. K. Radhakrishnan, *Appl. Phys. Lett.*, **79**, 4592 (2001).
16. J. T. Trattles, A. G. O'Neill, and B. C. Mecrow, *J. Appl. Phys.*, **75**, 7799 (1994).
17. J. W. Christian, *The Theory of Transformations in Metal and Alloys, PART I*, Pergamon (2002).
18. R. J. Gleixner, B. M. Clemens, and W. D. Nix, *J. Mater. Res.*, **12**, 2081 (1997).
19. D. A. Porter and K. E. Easterling, *Phase Transformations in Metals and Alloys*, Stanley Thornes Publishers Ltd (2000).
20. P. A. Flinn, *MRS Bulletin*, **20**, 70 (1995).
21. E. Zschech, H.-J. Engelmann, M. Meyer, V. Kahlert, A. V. Vairagar, S. G. Mhaisalkar, A. Krishnamoorthy, M. Yan, K. N. Tu, and V. Sukharev, *Zeitschrift fur Metallkunde*, **96**, 966 (2005).
22. B. M. Clemens, W. D. Nix, and R. J. Gleixner, *J. Mater. Res.*, **12**, 2038 (1997).
23. Z. Jing, M. O. Bloomfield, L. Jian-Qiang, R. J. Gutmann, and T. S. Cale, *IEEE Trans. Sem. Man.*, **19**, 437 (2006).
24. A. V. Vairagar, S. G. Mhaisalkar, A. Krishnamoorthy, and K. N. Tu, *J. Appl. Phys.*, **85**, 2502 (2004).
25. E. Zschech and V. Sukharev, *Microelectron. Eng.*, **82**, 629 (2005).
26. J. Lloyd and K. P. Rodbell, in *Handbook of Semiconductor Interconnection Technology*, G. C. Schwartz and K. V. Srikrishnan, Editors, p. 471 (2006).