The Effect of Copper Grain Size Statistics on the Electromigration Lifetime Distribution

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***Abstract*—We investigate the influence of the statistical distribution of copper grain sizes on the electromigration time-to-failure distribution. We have applied a continuum multi-physics electromigration model which incorporates the effects of grain boundaries for stress build-up. The peak of tensile stress develops at the intersection of copper grain boundaries with the capping layer. It is shown that the electromigration lifetimes follow lognormal distributions. Moreover, the increase of the standard deviation of the grain size distribution results in an increase of the electromigration lifetimes standard deviation. The results strongly imply that the lognormal distribution of the grain sizes is a primary cause for the lognormal distribution of electromigration lifetimes.**

I. Introduction

The continuous shrinking of the dimensions of on-chip interconnects and the introduction of advanced backend-of-line (BEoL) manufacturing process steps increases the complexity of physical phenomena behind electromigration failure. The total wiring length amounts to kilometers arranged in several levels of metallization with millions of interlevel connections. The tendency of modern technologies to increase the interconnect length and, at the same time, to reduce the cross section, makes the interconnect structures more and more susceptible to electromigration. Currently, integrated circuits are often designed using simple and conservative design rules to ensure that the resulting circuits meet reliability goals. However, this precaution leads to reduced performance for a given circuit and metallization technology.

Electromigration data have been described by lognormal distributions [1]. Although the origin of the lognormal distribution of electromigration lifetimes is not entirely clear, it has been argued that the diffusion process in connection with the effect of microstructure on electromigration provides the basis for the lognormal distribution [2]. In copper dual-damascene interconnects the main diffusivity path is along the copper/capping layer interface. This interfacial diffusion is affected by the orientation of the grains. As the copper grain sizes seem to follow lognormal distributions in typical dual-damascene process technology [2] and due to the influence of microstructure on the electromigration process, the lognormal distribution has been used as the underlying statistics for electromigration lifetimes. However, it has been discussed whether this choice is the most appropriate [3], [4]. The understanding of the electromigration lifetime distribution is crucial for the extrapolation of the times to failure obtained empirically from accelerated tests to real operating conditions, as performed by a modified form of the Black equation [1].

Also, it has been shown that the microstructure plays a key role regarding the failure mechanisms in copper dual-damascene interconnects [5]. It affects electromigration in different ways. Grain boundaries are natural locations of atomic flux divergence, they act as fast diffusivity paths for vacancy diffusion [6], and they act as sites of annihilation and production of vacancies [7].

The main challenge in electromigration modeling is the diversity of physical phenomena which have to be taken into account for an adequate description of the problem. Electromigration transport is also accompanied by material transport driven by the gradients of material concentration, mechanical stress, and temperature. Furthermore, taking into account the effects of interfaces and grain boundaries as fast diffusivity paths imposes new challenges for electromigration modeling.

In this work we investigate the origin of the statistical distribution of electromigration times to failure as a function of the distribution of copper grain sizes. The effect of lognormal grain size distributions on the distribution of electromigration lifetimes of fully three-dimensional copper dual damascene interconnect structures is studied based on numerical simulations. We have applied a continuum multi-physics electromigration model which incorporates the effects of grain boundaries for stress build-up. Moreover, we have developed a tool to include the microstructure into the simulations based on a given statistical distribution of grains sizes.

II. Electromigration Modeling

Several driving forces are responsible for the vacancy transport in a conductor line under electromigration. The combination of these driving forces leads to the total vacancy flux given by

$$\vec{J}_v = -D_v\left(\nabla C_v + \frac{|Z^*e|}{k_BT}C_v\nabla\varphi + \frac{f\Omega}{k_BT}C_v\nabla\sigma\right), \qquad (1)$$

where D_v is the vacancy diffusion coefficient of the dominant transport path, C_v is the vacancy concentration, Z^*e is the effective charge, f is the vacancy relaxation ratio, Ω is the atomic volume, σ is the hydrostatic stress, k_B is Boltzmann's constant, and T is the temperature.

Vacancies accumulate or vanish in sites of flux divergence, and this dynamics is described by the continuity equation

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$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G(C_v), \tag{2}$$

where $G(C_v)$ is the source function which models vacancy generation and annihilation processes [8]. The source term plays a major role for the mechanical stress buildup and is taken into account only at interfaces and grain boundaries. It comprises three processes, namely, the exchange of point defects between adjacent grains, the exchange of point defects between grains and grain boundaries, and the formation/annihilation of point defects at grain boundaries.

In our model grain boundaries are treated as separate regions which can trap or release vacancies [9], as shown in Fig. 1. We denote the vacancy concentration from both sides of the grain boundary as C_v^1 and C_v^2, respectively, and the concentration of immobile vacancies which are trapped inside the grain boundary as C_v^{im}.

The trapping rate of vacancies at the grain boundary, which corresponds to the generation/recombination rate, is controlled by the atomic fluxes J_v^1 and J_v^2, yielding [9]

$$\frac{\partial C_v^{im}}{\partial t} = G = \frac{1}{\tau}\Big[C_v^{eq} - C_v^{im}\Big(1 + \frac{2\,\omega_R}{\omega_T(C_v^1 + C_v^2)}\Big)\Big], \tag{3}$$

where ω_T is the trapping rate of vacancies from both neighboring grains, ω_R is the release rate, and C_v^{eq} is the equilibrium vacancy concentration inside the grain boundary, given by

$$C_v^{eq} = C_v^0 \exp\Big(\frac{\sigma_{nn}\Omega}{k_B\,T}\Big), \tag{4}$$

where C_v^0 is the equilibrium vacancy concentration in the absence of stress and σ_{nn} is the stress component normal to the grain boundary. In (3) τ represents the vacancy relaxation time which characterizes the efficiency of the grain boundary as vacancy sink/source [9]

$$\frac{1}{\tau} = \frac{\omega_T(C_v^1 + C_v^2)}{\delta}. \tag{5}$$

Sarychev *et al.* [10] introduced the contribution of vacancy migration and generation/annihilation processes for stress build-up in a three-dimensional model of stress evolution during electromigration. Considering the grain boundary model we have proposed that the strain growth from both sides of the grain boundary is proportional to the growth rate of immobile vacancies

$$\frac{\partial \varepsilon_{kk}}{\partial t} = \Omega\Big[(1-f)\nabla \cdot \vec{J}_v + f\frac{\partial C_v^{im}}{\partial t}\Big], \tag{6}$$

where ϵ_{kk} is the trace of the strain vector.

Equation (6) shows that vacancies trapped at the grain boundaries are responsible for build-up of tensile stress. When the grain boundaries are able to capture large amounts of vacancies, a high tensile stress develops.

The system of equations formed by (1)–(6) is solved until a stress threshold (σ_{th}) for void nucleation is reached at an intersection of grain boundaries with the capping layer. These intersections are considered sites of weak adhesion and, consequently, most susceptible to void nucleation [11].

Gleixner *et al.* [12] showed that the stress threshold is given by

$$\sigma_{th} = \frac{2\gamma_s \sin\theta_c}{R_p}, \tag{7}$$

where R_p is the radius of the adhesion-free patch, θ_c is the contact angle between the void and the surface, and γ_s is the surface energy.

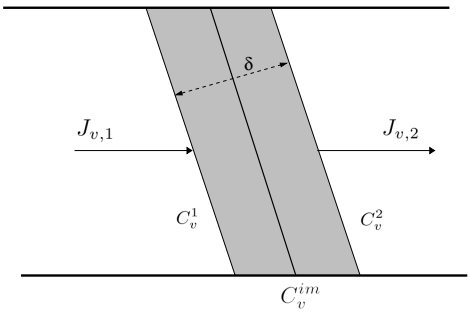

Fig. 1. Grain boundary model.

III. Simulation Approach

Equations (1)–(6) are solved using the finite element method (FEM) until the stress threshold for void nucleation is reached at some weak adhesion point. We consider the intersection of grain boundaries with the copper/capping layer interface as natural places of weak adhesion [11]. As grain boundaries and interfaces act as fast diffusivity paths, the diffusion coefficient in (1) has to be adapted for these regions. We have used $D_v^{gb} = 10^4 D_v^{bulk}$ for grain boundaries and $D_v^{Cu-cap} = 10^5 D_v^{bulk}$ for the copper/capping layer interface [13]. It should be pointed out that all model parameters are equal for all grains and all simulated structures. Grain boundaries, and generally, material interfaces of the geometry have to be supplied with an appropriately fine FEM mesh. This is necessary in order to provide sufficient resolution for the local dynamics described by the proposed model.

In order to include the grain distribution into the numerical simulations, a microstructure generator tool has been developed. Given a specific interconnect structure and providing the tool with a median grain size and corresponding standard deviation, it generates a lognormal distribution of grain sizes. Then, following this distribution, the interconnect line is cut along its length by the planes that form the grain boundaries. Furthermore, the angles between the grain boundaries planes and the line surface follow a normal distribution with median value of 90 °C. The corresponding standard deviation can also be specified.

In Fig. 2 we present the schema of the simulation procedure. Three standard deviations for the distribution of grain sizes are considered, namely 0.1, 0.3 and 0.6. For each of them 20 dual-damascene interconnect structures were created with the microstructure generator. As the interconnect line is assumed

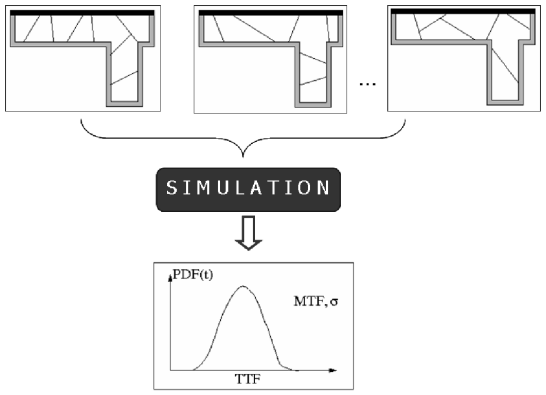

Fig. 2. Schematic simulation procedure.

to present a bamboo-like structure, the median grain size is equal to the line width, 0.10 μm. The barrier, capping and interlayer dielectric layers are Ta, SiN, and SiO_2, respectively. The corresponding interconnect structure is shown in Fig. 3.

The applied current density is 1.5 MA/cm^2, and the temperature is 300 °C. We have used a stress threshold value as failure criterion, which means that the electromigration time to failure represents the time for a void nucleation to occur. Thus, the time to failure is determined by the time for the stress to reach a given threshold value at some intersection between a grain boundary and the SiN layer.

IV. Results and Discussion

Fig. 5 shows the hydrostatic tensile stress development for the structures with grain size standard deviation of 0.3. The stress peak value follows the peak of trapped vacancy concentration and is located at the intersection of grain boundaries with the capping layer, as shown by Fig. 4.

Collecting the times to failure from Fig. 5 and calculating the cumulative failure percentages resulted in the distributions of electromigration lifetimes shown in Fig. 6. The lifetimes are fitted by lognormal distributions. The obtained standard deviations are 0.0065, 0.0080, and 0.0085 for the grain size distributions with standard deviations of 0.1, 0.3, and 0.6, respectively. The standard deviation for a lognormal distribution is given by

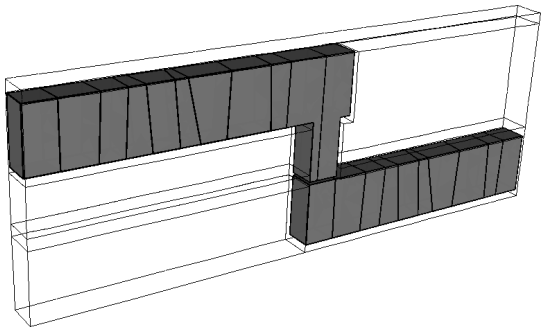

Fig. 3. Dual-damscene interconnect structure.

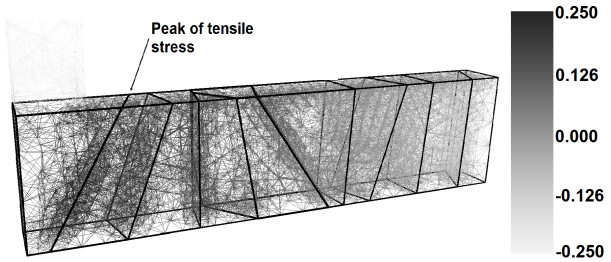

Fig. 4. Hydrostatic stress distribution in a simulated interconnect (in MPa). The peak value is located at grain boundaries, where vacancies are trapped.

$$\sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(ln\ TTF_i - ln\ MTF)^2}. \quad (8)$$

where TTF_i is the time to failure of the i-th test structure, N is the number of test structures, and MTF is the mean time to failure of the lognormal distribution

$$ln\ MTF = \frac{1}{N}\sum_{i=1}^{N} ln\ TTF_i, \quad (9)$$

The standard deviations for the electromigration lifetimes are very small compared to those frequently observed in experiments [1]. Several factors can explain this behavior. First, for convenience, we have used a small value of stress threshold as failure criterion to determine the interconnect lifetime. As can be seen from Fig. 5, the variation of the lifetimes can be more pronounced for higher stress thresholds. Second, the simulation parameters and material properties are independent of the grain distribution. This means that mechanical properties and diffusivities, for example, are equal and constant for all grains in an interconnect line, for all simulated structures. This is clearly not the case in real experiments, as it is well known that material properties vary according to the grain orientation. It is expected that atomic diffusion along the copper/capping layer interface changes from grain to grain, inducing a flux

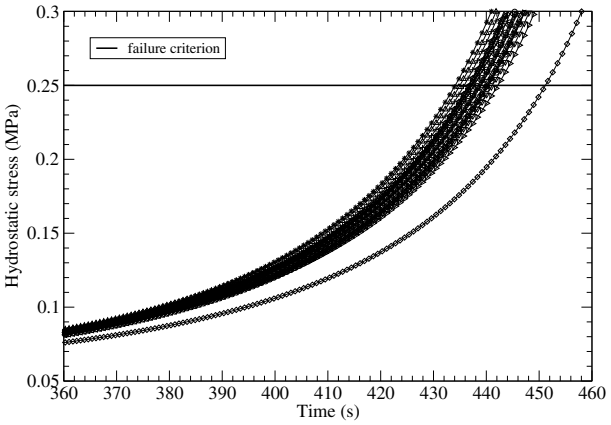

Fig. 5. Peak of hydrostatic stress development for the set with grain size standard deviation of 0.3.

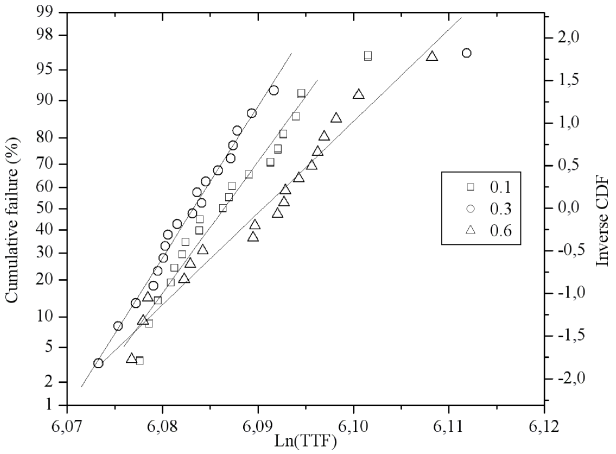

Fig. 6. Electromigration lifetime distributions.

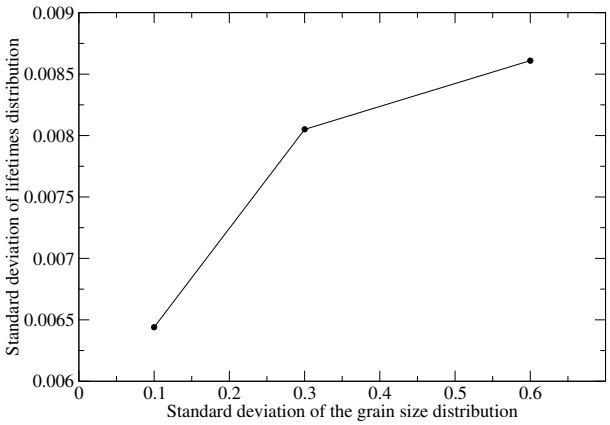

Fig. 7. Electromigration lifetime standard deviation for different standard deviations of grain size.

divergence at the corresponding grain boundary. Moreover, the diffusivities are different from line to line as the grain distribution varies. Therefore, given the simplifications we have made, the small standard deviations obtained from our simulations should be expected.

Nevertheless, our results show that the grain distribution still affects the electromigration lifetime distribution.When the grain size distribution exhibits a smaller standard deviation the corresponding interconnect lines have a more uniform distribution of the grains. As a consequence, the stress build-up has smaller variations yielding a smaller standard deviation of the electromigration lifetimes. On the other hand, increasing the grain size standard deviation, the lines exhibit significant differences in the grain structures. This leads to increased variations for the stress development. Thus, a bigger standard deviation of electromigration lifetimes is expected. This behavior is presented in Fig. 7. It shows that the increase of the standard deviation of the distribution of grains sizes increases the standard deviation of the electromigration lifetime distribution.

V. Conclusion

We analyzed the electromigration failure development in typical copper dual-damascene interconnect structures based on numerical simulations. A continuum electromigration model which describes mechanical stress build-up in connection with the microstructure effect was applied. We observed that the peak of tensile stress is located at the intersection of grain boundaries with the capping layer, following the peak of trapped vacancy concentration. This shows that the microstructure has a decisive impact on the determination of void nucleation sites. The simulation results indicate that the lognormal distribution of the copper grain sizes is a primary cause for the lognormal distributions of the electromigration lifetimes. Moreover, an increase of the standard deviation of the grain size distribution leads to an increase of the electromigration time-to-failure distribution.

Acknowledgment

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