

# Applicability of Charge Pumping on Germanium MOSFETs

K. Martens, B. Kaczer, T. Grassler, B. De Jaeger, M. Meuris, H. E. Maes, and G. Groeseneken

**Abstract**—In this letter, the charge-pumping (CP) technique is validated for germanium MOSFETs. Effects of the smaller Ge bandgap on CP are discussed through both experiments and simulations. The standard CP setup with  $\sim 100$ -ns transition times at room temperature tuned for Si/SiO<sub>2</sub> MOS evaluates the Ge interface-trap density only near midgap, and the total density is thus strongly underestimated. We show two CP methods which can be used to correctly reflect the actual complete interface-trap density by probing closer to the band edges. The use of low-temperature measurements to probe traps near the band edges with CP is discussed. CP measurements are demonstrated with transition times down to 6-ns at 300-K without making use of RF structures. Using these fast measurements, it is possible to obtain an interface state density closer to the band edges for Ge MOSFETs at 300-K.

**Index Terms**—Charge pumping (CP), electrical characterization, Ge MOSFET, interface state density extraction.

## I. INTRODUCTION

ALTERNATIVE channel materials show promise for enhancing CMOS performance beyond silicon capabilities [1]–[4]. A crucial issue is the correct measurement of the electrical interface properties of semiconductor–dielectric interfaces. Previously, it was shown that, for non-Si/SiO<sub>2</sub> MOS, several issues arise which jeopardize the accuracy of the conductance method [5]. These issues are resolved by introducing the full-conductance method [5]. Charge pumping (CP), one of the most reliable techniques for analyzing the electrical properties of a MOSFET interface, is evaluated for germanium in this letter. When CP is used on Ge as it is used on Si/SiO<sub>2</sub> (300-K, 100-ns transition times), the method can underestimate the total interface-trap density because interface traps near the band edges are not measured. The effects of smaller bandgap and higher interface-trap densities are elaborated for the germanium case. We provide two approaches to measure interface-trap density in proximity to the band edges.

## II. DEVICES AND MEASUREMENT SETUP

The devices considered are Si-passivated Ge pMOSFETs [6] with TaN gates fabricated on n-type Ge-on-Si substrates (a 2- $\mu$ m-thick epitaxially grown and fully relaxed Ge layer on a

Manuscript received August 13, 2008. Current version published November 21, 2008. This work was supported by the Flemish Institute for Science and Technology (IWT). The review of this letter was arranged by Editor C. Bulucea.

K. Martens, H. E. Maes, and G. Groeseneken are with the IMEC vzw, The Interuniversity Microelectronics Center, 3001 Heverlee, Belgium, and also with the ESAT Laboratories, Catholic University of Leuven, 3000 Leuven, Belgium (e-mail: koen.martens@imec.be).

B. Kaczer, T. Grassler, B. De Jaeger, and M. Meuris are with the IMEC vzw, The Interuniversity Microelectronics Center, 3001 Heverlee, Belgium.

Digital Object Identifier 10.1109/LED.2008.2007582

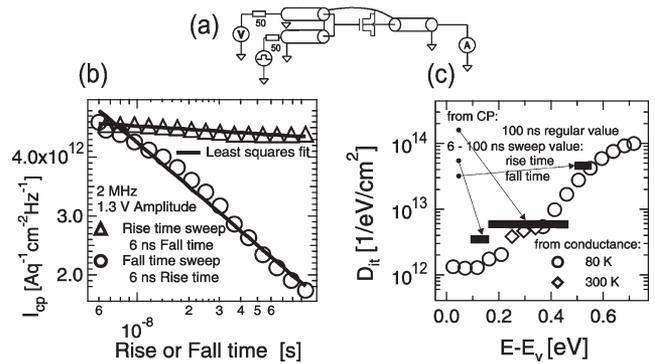


Fig. 1. (a) High-frequency setup used for CP with transition times down to 6 ns. (b) CP current as a function of rise and fall times down to 6 ns. The extracted characteristics using a least squares linear fit are shown in (c) as compared with an extraction using the full-conductance method.

p-type Si substrate) with a doping level of  $\sim 3 \times 10^{16}$ -cm<sup>-3</sup> defined by implantation. After appropriate surface cleaning, an  $\sim 0.8$ -nm Si layer is grown in an ASM Epsilon epitaxial reactor to passivate the Ge surface followed by an ozone oxidation forming 0.4-nm of silicon oxide. Then, a 4-nm HfO<sub>2</sub> layer is deposited using atomic layer deposition. The EOT of these MOSFETs is 1.4-nm as determined by split *CV*.

These devices show performance benefits as compared to Si MOSFETs [6] and an interface-trap distribution [ $D_{it}(E)$ ] deviating significantly from Si/SiO<sub>2</sub> MOS [5]. This makes the devices interesting and relevant to study how, and if, CP can be applied on Ge MOSFETs to extract  $D_{it}(E)$ .

A standard CP setup was used for 100-ns transition-time measurements. CP measurements with rise and fall times down to 6 ns without making use of RF structures were carried out by making use of a system with  $\sim 1$ -GHz bandwidth similar to the setup used for fast *Q-V* measurements [7] [see Fig. 1(a)]. The oscilloscope and pulse generator are 50- $\Omega$  terminated, and cables with 1-GHz bandwidth are used. The shields of the probes are connected in the probing area, which is kept within an area with a 2.5-cm radius. The bulk terminal is linked to the parameter-analyzer terminal while the source and drain terminals are grounded to the shield.

## III. THEORY

The CP current ( $I_{CP}$ ) is proportional to the amount of interface traps located in between the electron and hole emission levels ( $E_{e,e}$  and  $E_{e,h}$ , respectively) [8]

$$I_{CP} = qAf \int_{E_{e,h}}^{E_{e,e}} D_{it}(E) dE$$

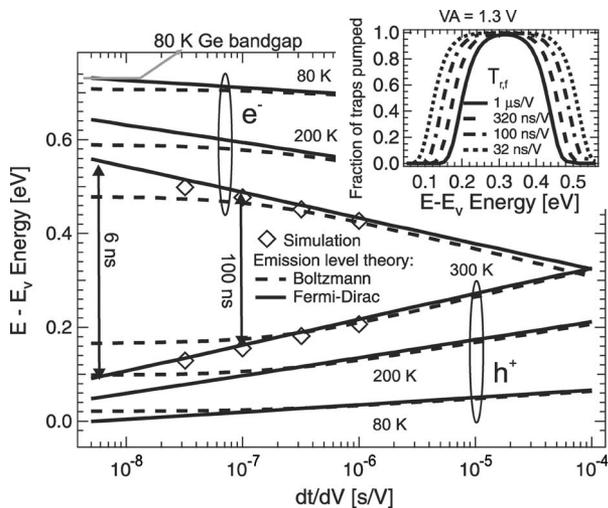


Fig. 2. Electron and hole emission levels calculated with Boltzmann [8] and Fermi-Dirac statistics as a function of pulse edge slew rate at different temperatures for germanium. (Inset) Simulation of the fraction of traps giving rise to CP current taking into account all emission and capture processes at 300-K. Equivalent emission levels from the simulation are compared with those from emission-level theory, showing the validity of the emission-level theory for germanium MOSFETs.

where  $q$  is the elementary charge,  $A$  is the device area,  $f$  is the CP frequency, and  $E$  is the energy. The emission levels for germanium are shown in Fig. 2 for a capture cross section of  $5 \times 10^{-17}\text{-cm}^{-2}$ .

The validity of the emission-level CP theory [8] was checked for germanium MOSFETs. Previously, it was shown that the conductance method is jeopardized by germanium's small bandgap as compared to silicon [5], [9]. We investigated whether germanium's small bandgap also jeopardizes CP measurements. In the emission-level approximation [8], it is assumed that, at any time during the application of a gate-voltage pulse, only one type of communication with one band is dominant (either emission or capture). Simulations which take into account all four mechanisms at any time during a CP cycle are done to verify whether this approximation still holds for germanium. The capture and emission-rate equation is integrated over time while transition times are varied, and a simulated curve showing the fraction of traps contributing to  $I_{cp}$  across the bandgap is shown in the Fig. 2 inset. A constant  $D_{it}$  of  $1 \times 10^{12}\text{-cm}^{-2} \cdot \text{eV}^{-1}$ , a capture cross section of  $5 \times 10^{-17}\text{-cm}^{-2}$  and an amplitude (VA) of 1.3-V is used at 300-K.

Equivalent emission levels are defined to give rise to the same measured integrated interface-trap density (per square centimeter) as the profiles shown in the Fig. 2 inset. It is clear that the equivalent emission levels from simulation and from the emission-level theory are in good agreement (Fig. 2), showing that the emission-level approximation holds for CP on MOSFETs with small bandgap materials like germanium.

At 300-K, only a small portion of the Ge bandgap is scanned, and the total interface state density is, hence, strongly underestimated.

The interface-trap distribution can be characterized across a wider portion of the bandgap for germanium MOSFETs by measuring at lower temperature. This is possible because the electron and hole emission levels move closer to the band

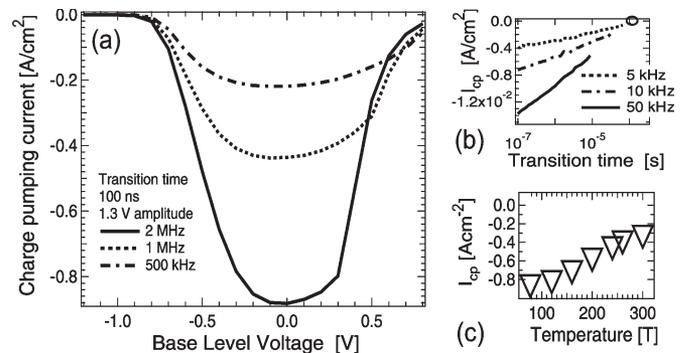


Fig. 3. (a) Ge MOSFET CP characteristics at 300-K show the typical hat shape and frequency scaling. (b) 300-K transition time sweep showing the point at which the CP current becomes zero. This corresponds to the time at which the hole and electron emission levels coincide. (c) CP current versus temperature increases in magnitude with decreasing temperature.

edges (Fig. 2). A monotonous increase in  $I_{cp}$  is expected when lowering the temperature [10].

An alternative method to characterize the interface-trap distribution across a wider portion of the bandgap is to measure with shorter transition times. According to emission-level theory based on Boltzmann statistics [8], lowering the transition times below 100-ns at 300-K will not make much difference because of the saturation of the emission levels near flatband and threshold voltage (see Fig. 2). Using Fermi-Dirac statistics, appropriate for ultrathin dielectrics, one sees that it is possible to scan further into the gap using CP with shorter transition times at 300-K (Fig. 2).

## IV. CHARACTERISTICS

### A. Room-Temperature Characteristics

Shown in Fig. 3(a) are 300-K base-level-sweep CP characteristics of Si-passivated germanium MOSFETs. A typical CP hat is observed (negative currents for pMOS) which shows proper frequency scaling. Sufficiently high frequencies (500-kHz–2-MHz) were chosen to avoid the influence of traps in the high- $\kappa$  oxide [11] in order to study the interface traps at the Ge–oxide interface only.

The magnitude of the CP signal shows an integrated interface-trap density of  $2 \times 10^{12}\text{-cm}^{-2}$  at a transition time of 100-ns while the total interface-trap density was previously determined to be  $\sim 1 - 2 \times 10^{13}\text{-cm}^{-2}$  using full-conductance measurements [5]. The experiment is, hence, in agreement with emission-level theory, since only the interface traps near midgap are measured with a regular CP measurement.

Transition-time-sweep measurements [see Fig. 3(b)] show that CP current becomes zero for a specific transition time. This specific transition time corresponds to the transition time at which the hole and electron emission levels coincide (see Fig. 2) and confirm the capture cross-sectional value of  $\sim 5 \times 10^{-17}\text{-cm}^2$  assumed in our simulations.

### B. Low-Temperature Characteristics

Measurements below 300-K are done to characterize the interface-trap distribution across a wider portion of the bandgap

for germanium MOSFETs [see Fig. 3(c)]. A 100-ns transition time and 1.3-V amplitude are used. The current is found to increase continuously in magnitude with decreasing temperature. At 80-K, an integrated interface-trap density of  $6 \times 10^{12}\text{-cm}^{-2}$  is extracted, showing that interface traps located closer to the band edges are measured at low temperature. Low-temperature measurements yield a more accurate and complete extraction of interface-trap density than possible at 300-K.

### C. Room-Temperature Characteristics With Ultrashort Transition Times

Another approach enabling characterization of the interface-trap density across a wider portion of the bandgap is reduction of CP transition times (see Fig. 2). For this purpose, a high-frequency setup [see Fig. 1(a)] is used with an  $\sim 1\text{-GHz}$  bandwidth, enabling transition times down to 6-ns.

Experiments show that, indeed, trap densities closer to the band edges can be extracted using CP (see Fig. 1) at 300-K. A clear increase in  $I_{cp}$  is evident when decreasing the fall time.

Extractions of interface-trap density were done from the CP transition time sweeps. A line is fitted to the CP current as a function of energy, which is related to the logarithm of the transition time [Fig. 1(b)]. The linear fit guarantees a robust extraction. The extracted interface-trap density from the rise and fall time sweeps corresponding to the valence and conduction band sides is shown in Fig. 1(b). The extractions [Fig. 1(c)] from CP measurements clearly confirm the asymmetric nature of the interface-trap density as previously found using the full-conductance method, which is the method resolving the issues of the conductance method [4]. Moreover, the correspondence with the full-conductance method results proves that using short transition times down to 6-ns indeed allows probing the interface traps closer to the band edges at 300-K.

## V. CONCLUSION

CP characteristics of germanium MOSFETs are investigated, and the validity of emission-level theory is confirmed for Ge MOSFETs. From theory and experiment, it is clear that 300-K CP with transition times down to 100-ns, as used for Si/SiO<sub>2</sub>, can only quantify the amount of interface traps in a fraction of the bandgap near midgap for Ge. This explains why Si/SiO<sub>2</sub> CP practices can lead to an underestimation of the actual total trap density in Ge.

To increase the measured fraction of the bandgap, low-temperature measurements can be used. By using transition times down to 6 ns, the interface-trap density is extracted closer to the band edges on germanium MOSFETs at 300-K. This

enables a convenient 300-K evaluation of interface-trap density across a large part of the bandgap for process- and reliability-evaluation purposes. The obtained results are found to be in agreement with full-conductance method results.

## ACKNOWLEDGMENT

The authors would like to thank R. Degraeve and M. Heyns for useful discussions and to AMSIMEC for measurement support. This letter is part of the IMEC core partner program, funded by Elpida, Hynix, Infineon, Qimonda, Intel, Matsushita, Micron, NXP, Samsung, ST, TI, and TSMC.

## REFERENCES

- [1] K. Saraswat, C. O. Chui, K. Donghyun, T. Krishnamohan, and A. Pette, "High mobility materials and novel device structures for high performance nanoscale MOSFETs," in *IEDM Tech. Dig.*, 2006, pp. 659–662.
- [2] C. O. Chui, F. Ito, and K. C. Saraswat, "Nanoscale germanium MOS dielectrics—Part I: Germanium oxynitrides," *IEEE Electron Device Lett.*, vol. 53, no. 7, pp. 1501–1507, Jul. 2006.
- [3] T. Maeda, M. Nishizawa, and Y. Morita, "Role of germanium nitride interfacial layers in HfO<sub>2</sub>/germanium nitride/germanium metal-insulator-semiconductor structures," *Appl. Phys. Lett.*, vol. 90, no. 7, pp. 072 911-1–072 911-3, Feb. 2007.
- [4] G. Mavrou, S. Galata, P. Tsipas, A. Sotiropoulos, Y. Panayiotatos, A. Dimoulas, E. K. Evangelou, J. W. Seo, and C. Dieker, "Electrical properties of La<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub>/La<sub>2</sub>O<sub>3</sub> gate dielectrics for germanium metal-oxide-semiconductor devices," *J. Appl. Phys.*, vol. 103, no. 1, pp. 014 506-1–014 506-9, Jan. 2008.
- [5] K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547–556, Feb. 2008.
- [6] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L.-Å. Ragnarsson, D. P. Brunco, F. E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M. M. Heyns, "High performance Ge pMOS devices using a Si-compatible process flow," in *IEDM Tech. Dig.*, San Francisco, CA, 2006, pp. 1–4.
- [7] K. Martens, M. Rosmeulen, B. Kaczer, G. Groeseneken, and H. E. Maes, "Electrical characterization of leaky charge-trapping high- $\kappa$  MOS devices using pulsed Q-V," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 436–439, May 2007.
- [8] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, no. 1, pp. 42–53, Jan. 1984.
- [9] P. Batude, X. Garros, L. Clavelier, C. Le Royer, J. M. Hartmann, V. Loup, P. Besson, L. Vandroux, Y. Campidelli, S. Deleonibus, and F. Boulanger, "Insights on fundamental mechanisms impacting Ge metal oxide semiconductor capacitors with high- $k$ /metal gate stacks," *J. Appl. Phys.*, vol. 102, no. 3, p. 034 514, Aug. 2007.
- [10] G. Van den Bosch, G. Groeseneken, P. Heremans, and H. E. Maes, "Spectroscopic charge pumping: A new procedure for measuring interface trap distributions on MOS transistors," *IEEE Trans. Electron Devices*, vol. 38, no. 8, pp. 1820–1831, Aug. 1991.
- [11] H. Dawei, C. D. Young, G. A. Brown, P. Y. Hung, A. Diebold, E. M. Vogel, J. B. Bernstein, and G. Bersuker, "Spatial distributions of trapping centers in HfO<sub>2</sub>/SiO<sub>2</sub> gate stack," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1338–1344, Jun. 2007.