Energetic distribution of oxide traps created under negative bias temperature stress and their relation to hydrogen

Thomas Aichinger,[1,a)] Michael Nelhiebel,[2,b)] Stefan Decker,[3,c)] and Tibor Grasser[4,d)]
[1]*Kompetenzzentrum für Automobil- und Industrieelektronik (KAI), Villach 9500 Austria*
[2]*Infineon Technologies Austria, Villach 9500 Austria*
[3]*Infineon Technologies AG, Munich 81739 Germany*
[4]*Christian Doppler Laboratory for TCAD, Institute for Microelectronics TU Vienna, Vienna 1040 Austria*

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By applying an incremental sweep technique to silicon devices subjected to negative bias temperature stress, we identify two significant peaks of recoverable oxide defects located energetically within the silicon band gap. The first peak is near midgap and is almost fully developed after ten seconds of stress while the second peak is found in the upper half of the silicon band gap and develops gradually as a function of stress time. We obtain very similar density-of-state profiles for two samples having vastly different hydrogen concentrations within the gate oxide indicating that the precursor for oxide trap creation is independent of hydrogen. © *2010 American Institute of Physics*. [doi:10.1063/1.3374452]

After subjecting p-doped metal oxide semiconductor (PMOS) devices to negative bias temperature stress (NBTS),[1] it has been reported that some of the defects causing a negative V_{TH} shift rapidly recover at the moment the gate bias is switched from the stress level to the much lower threshold voltage of the device.[2,3] This recovery phenomenon is either attributed to the back-diffusion of hydrogen and the subsequent repassivation of previously created interface states[4,5] or the neutralization and annealing of positively charged switching oxide traps (E' centers) via elastic/inelastic carrier exchange with the silicon substrate.[6,7] While the first explanation suggests a strong correlation between the recovery rate and the amount of hydrogen released from the interface during stress, the second model predicts recovery characteristics mainly dependent on the concentration and the energy of the free substrate carriers at the interface. Provided the trap precursor includes no hydrogen (i.e., oxygen vacancy[8]) the second explanation particularly suggests a hydrogen independent recovery mechanism.

By applying a recently suggested incremental sweep technique[9] to devices having different initial hydrogen concentrations within their gate oxides, we obtain similar recovery characteristics (density-of-state profiles). By contrast, vastly different permanent V_{TH} offsets remain after repeated gate bias switches between inversion and accumulation. Thus, our results indicate that the total V_{TH} shift observed after NBTS consists of a recoverable component which is independent of hydrogen and whose recovery rate can be controlled by the Fermi level (gate bias). On the other hand, there is a superimposed permanent component which is highly dependent on the hydrogen concentration within the gate oxide and correlates well with the increase in the charge pumping (CP) current.

We use PMOS devices with 30 nm SiO_2 gate oxides. During Back End of Line processing, we have incorporated titanium layers of different thicknesses below the metallization in order to control the hydrogen diffusion from upper hydrogen-rich plasma enhanced chemical vapor deposited silicon nitride layers toward the gate oxide during fabrication. Titanium is known to be an effective barrier against hydrogen diffusion.[10] We analyze two selected split wafers which provide vastly (about an order of magnitude) different hydrogen concentrations within the gate oxide. This is demonstrated in Fig. 1 by the considerably different virgin CP characteristics (recorded in the constant base level mode). Wafer I is supposed to have a well passivated interface (thin Ti liner → much hydrogen → low CP signal) while wafer II seems to have a weakly passivated interface (thick Ti liner → few hydrogen → high CP signal). Following Ref. 11, the average density of interface states was calculated from the maximum CP signal. It yields $D_{it} \sim 2 \times 10^9$ eV^{-1} cm^{-2} for wafer I and $D_{it} \sim 7 \times 10^{10}$ eV^{-1} cm^{-2} for wafer II. The correlation between the virgin CP current and the hydrogen incorporation within the gate oxide is supported by "time of flight secondary ion mass spectroscopy" measurements not

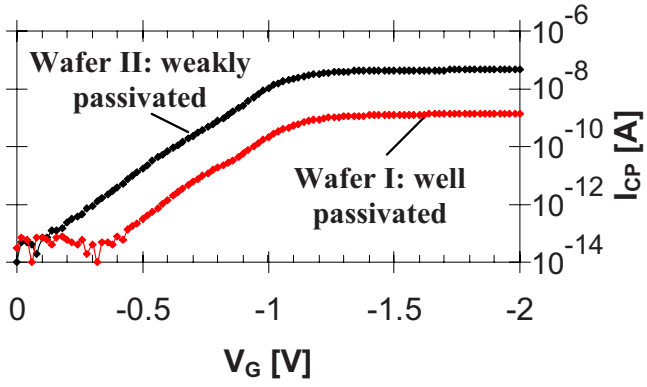

FIG. 1. (Color online) The virgin CP currents of the two selected split wafers (wafer I—well passivated interface; wafer II—weakly passivated interface). The CP currents were recorded in the constant base level mode (variable amplitude) at a temperature of −60 °C and at a frequency of 1 MHz using a trapezoidal gate pulse shape with constant rising/falling slopes of 32 V/μs.

a)Electronic mail: thomas.aichinger@k-ai.at. Tel.: +43 4242 34 890. FAX: +43 4242 34890 99.
b)Electronic mail: michael.nelhiebel@infineon.com. Tel.: +43 5 1777 2723.
c)Electronic mail: stefan.decker@infineon.com. Tel.: +49 89 234 46298.
d)Electronic mail: grasser@iue.tuwien.ac.at. Tel.: +43 1 58801 36023.

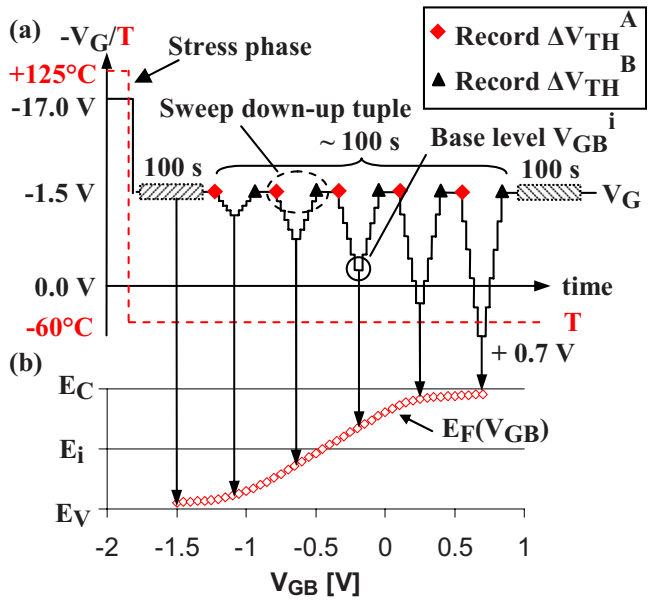

FIG. 2. (Color online) A schematic illustration of the incremental sweep technique (a). The V_{TH} shift is measured for 100 s at a constant gate bias of V_G=−1.5 V directly post stress and directly after the incremental sweep procedure. In-between, we record V_{TH} shift tuples right before (diamonds) and right after (triangles) each double-staircase ramp. The Fermi level positions corresponding to the base potentials (V_{GB}^i) of the double-ramps are illustrated in (b). The energy levels $E_F(V_{GB}^i)$ were simulated numerically using Medici and a process simulation of the device.

illustrated in Fig. 1, see supplementary material (Ref. 12 or 13).

We perform four subsequent stress-recovery runs on every device with increasing stress times (10/100/1000/10000 s). During stress, we use *in situ* poly heaters[14] to heat the device from −60 °C (chuck temperature) to +125 °C (stress temperature). During recovery, we characterize the device at −60 °C as it is beneficial for defect profiling since trap neutralization via tunneling is assumed to be due to an inelastic multiphonon process and is hence temperature accelerated.[15]

The incremental sweep technique, applied during recovery, is schematically depicted in Fig. 2(a). At the end of each stress run, we turn off the poly heater which terminates stress abruptly [cf. degradation quenching in Ref. 14]. Afterwards, we switch the gate bias from stress level to −1.5 V (deep inversion) and remain there for 100 s. This constant bias phase is introduced in order to monitor the fast initial recovery phase associated with the large gate voltage drop from stress level −17.0 V to −1.5 V. Furthermore, it guarantees that time dependent recovery is negligible during the subsequent incremental sweep procedure which takes another 100 s. The measured recovery rates during the first 100 s constant gate bias phase are illustrated in Fig. 3. Both samples show similar recovery rates of ~1.8 mV/decade which slightly increase with stress time.

After the initial recovery phase, we initiate the incremental sweep by performing double-staircase ramps where the potential of the base level is elevated stepwise from −1.5 V (deep inversion) toward +0.7 V (accumulation). Before and after each double-ramp, we record V_{TH} shift tuples at −1.5 V. As described in detail in Ref. 9, the technique allows energetic profiling of recoverable oxide defects by referencing the successive decrease in the ΔV_{TH} shift (measured at

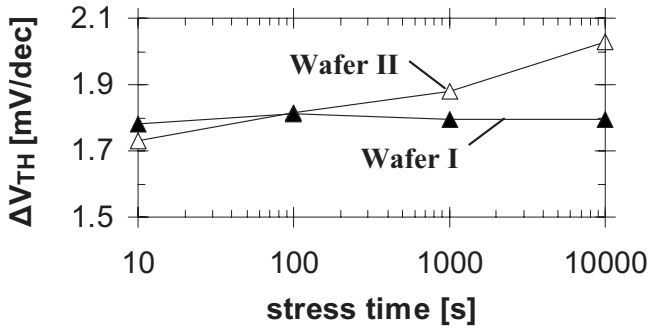

FIG. 3. The recovery rates of the two selected split wafers recorded within the 100 s constant gate bias phase (−1.5 V) directly post stress at −60 °C. Both samples show similar time dependent recovery rates of approximately 1.8 ± 0.2 mV/decade.

−1.5 V) to the corresponding Fermi level position between ramp down and ramp up, cf. Fig. 2(b). We remark that the actual energetic position of the trap states within the gate oxide may deviate from these extracted effective energies due to the multiphonon nature of the charge exchange mechanism causing neutralization during recovery.

By assuming the spatial location of the recoverable oxide traps close to the gate oxide-substrate interface, we can calculate the effective density of state profile as follows:

$$D_{OX}^{rec}\left(\frac{E_F^i + E_F^{i-1}}{2}\right) = \frac{C_{OX}}{q} \cdot \frac{\Delta V_{TH}^A(E_F^i) - \Delta V_{TH}^B(E_F^i)}{E_F^i - E_F^{i-1}}. \quad (1)$$

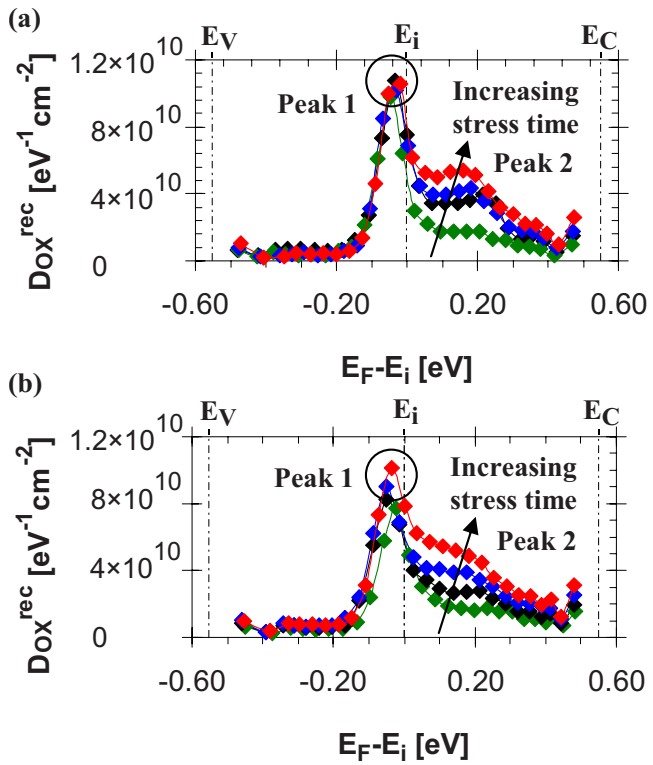

FIG. 4. (Color online) The recoverable effective density of state (D_{OX}^{rec}) profiles of wafer I (a) and wafer II (b) extracted from the V_{TH} shift tuples measured during the incremental sweep procedure. Both samples show two peaks; the first is located close to midgap and almost fully developed after ten seconds of stress; the second is located in the upper half of the silicon band gap and develops gradually as a function of stress time.

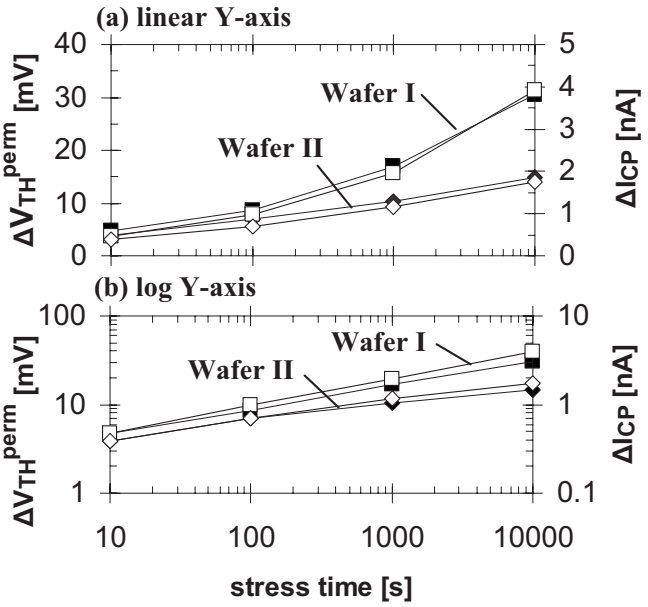

FIG. 5. The permanent V_{TH} shift (full symbols) and the increase in CP current (open symbols) of wafer I (squares) and wafer II (diamonds) as a function of stress time (a). Wafer I shows a considerable higher permanent V_{TH} shift and interface degradation than wafer II. The increase in CP current correlates with the permanent V_{TH} shift by a multiplicative factor. The permanent components of both split wafers show a power-law like increase with stress time (b), wafer II having a smaller power-law exponent than wafer I.

In Eq. (1) C_{OX} is the oxide capacitance, q the elementary charge and E_F^i is the Fermi level position at the base level V_{GB}^i.

The effective density of state profiles of both split wafers are illustrated in Fig. 4. Both samples show very similar recoverable DOS profiles indicating that the trap precursor is actually independent of hydrogen. In particular, we observe two significant peaks; the first one is located near the midgap and is almost fully developed after ten seconds of stress; the second one is located in the upper half of the silicon band gap and develops gradually with further increasing stress times.

The permanent V_{TH} shift (ΔV_{TH}^{perm}; measured for 100 s directly after the sweep procedure at -1.5 V) and the increase in CP current (ΔI_{CP}; measured directly after ΔV_{TH}^{perm} by gate pulsing) are illustrated in Figs. 5(a) and 5(b) as a function of the stress time. ΔV_{TH}^{perm} and ΔI_{CP} correlate by a multiplicative factor and they are considerably larger for wafer I (well passivated interface) than for wafer II (weakly passivated interface) indicating that both components are directly linked to each other and to hydrogen.

In this paper we have analyzed the density of state profiles of recoverable oxide traps by making use of the recently published incremental sweep technique. In particular, we found two peaks located energetically in the middle and in the upper half of the silicon band gap. By comparing two PMOS devices taken from selected split wafers which provide vastly different hydrogen budgets within the gate oxide, we found that recovery is independent of hydrogen while the increase in the CP current and the permanent V_{TH} shift is strongly connected to hydrogen.

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