

Temperature dependence of the emission and capture times of SiON individual traps after positive bias temperature stress

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A new method to analyze the statistical properties of individual defects on pMOSFETs has been recently introduced to get insight into the recovery component after negative bias temperature stress (NBTS) [1]. This method is based on the quantized threshold voltage V_{TH} transients observed on nano-scaled MOSFET devices following stress and provides the characteristic emission and capture times of individual traps [2]. In this work, we apply the methodology to a single SiON nMOSFET (EOT=1.6nm) after positive bias temperature stress (PBTS). A strong temperature dependence is observed for both emission and capture times. The obtained activation energies are in the order of 0.6eV and they are close to the values obtained for negatively stressed SiON pMOSFET [1]. This fact is incompatible with the direct e-tunneling theory which is extensively used in the operation model of charge trap memories [3], PBTI [4], and TSCIS [5].

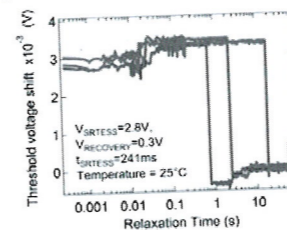


Fig.1 V_{TH} transients of a single device stressed at 25°C and 2.8V for 241ms. The V_{TH} transients show a discrete behavior due to the electron emission from an individual trap.

Fig. 1 shows three typical V_{TH} transients after stressing a single $70 \times 90 \text{ nm}^2$ nMOSFET device at 25°C and 2.8V for 241ms. The procedure to obtain these curves is based on fast V_{TH} -evaluation methods developed on BTI [6]. In Fig. 1, a V_{TH} shift of 3mV is observed for the three traces at the start of the relaxation period that drops abruptly to 0V at relaxation times about 1s. The discrete V_{TH} drop observed in Fig. 1 is due to the electron emission from an individual trap. The large step height is understood by means of the random dopant fluctuations in the nMOSFET channel [7] that generate different conduction paths between drain and source. These paths can be modified by the charge and discharge of traps, thus modifying the drain current. The change of drain current can be in turn transformed into a V_{TH} shift taken as a reference the I_D - V_G curve of the fresh device.

Fig. 2 shows a histogram of the emission times $t_{emission}$ obtained when the experiment was repeated 20 times on the same device. The histogram shows a $A t_{emission} / \tau_{emission} \exp\{-t_{emission} / \tau_{emission}\}$ distribution with $\tau_{emission}$ equal to 10 ± 1 s at 25°C, and number of events A equal to 20. The Arrhenius plot of the emission time shown in Fig. 2b demonstrates a strong temperature dependence of this

parameter. Note that the extracted activation energy is 0.68eV.

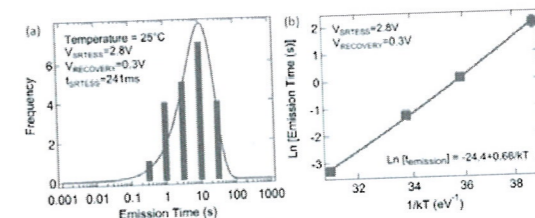


Fig.2. (a) Histogram of the emission times extracted from 20 V_{TH} transients of a single device stressed at 25°C and 2.8V for 241ms. (b) The Arrhenius plot of the emission time $\tau_{emission}$ shows a strong temperature dependence of this parameter.

The procedure was repeated on the same device with decreasing stress time $t_{stress} = \{241, 189, 136, 28, 14\}$ ms. As shown in Fig. 3a, the probability of charging the trap decreases with decreasing stress time and is described by $P_C = 1 - \exp(-t_{stress} / \tau_{capture})$. The obtained capture time $\tau_{capture}$ for this characteristic trap was 37 ± 14 ms at 25°C and decreased to 6 ± 1 ms when the temperature was increased to 50°C. As shown in Fig. 3b, the extracted thermal activation energy for the capture time of this trap was 0.62eV.

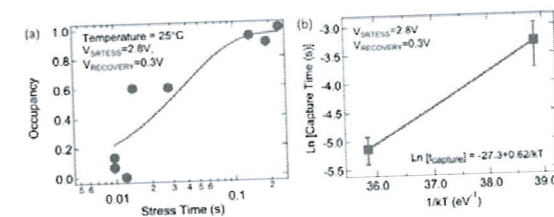


Fig.3 (a) Trap occupancy P_C as a function of the stress time t_{stress} for a single device stressed at 25°C and 2.8V. (b) Arrhenius plot of capture time $\tau_{capture}$

In summary, we have successfully applied a recently developed methodology for the study of individual traps in a positively stressed nano-scaled SiON nMOSFET. From this study, we conclude that the emission and capture times of individual traps are thermally activated, in agreement with the findings presented on SiON pMOSFET after negative bias temperature stress. Therefore, analogous traps are responsible of the relaxation curves in pMOSFETs and nMOSFETs under NBTS and PBTS, respectively. This result disagrees with the direct tunneling theory ubiquitously used in different trap characterization techniques and simulations.

[1] T. Grasser IEDM 2009, [2] M.J. Kirton APL 1989, [3] E. Vianello IEDM 2009, [4] G. Reimbold WoDiM 2006, [5] R. Degraeve IEDM 2008, [6] B. Kaczer IRPS 2008, [7] A. Ghetti TED 2009.