A Monte Carlo Simulation of Reproducible Hysteresis in RRAM

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Abstract — **A generalization of the stochastic model of the resistive switching mechanism in bipolar metal-oxide-based resistive random access memory (RRAM) is presented. The distribution of electron occupation probabilities obtained is checked with respect to results of previously published work. A hysteresis cycle of a RRAM simulated with our generalized stochastic model is in agreement with experimental results. Time-dependent simulations indicate that a proper conducting filament rapture during the RESET process is achieved, when the product "voltage – time" is maximal. Simulations of multiple switching cycles with help of the generalized stochastic model open the path towards parameter optimization to maximize the RRAM endurance.**

Keywords - resistive switching mechanism; stochastic model; Monte Carlo method; RRAM.

I. INTRODUCTION

In modern microelectronic devices the dominant memory types are DRAM, static RAM, and flash memory. These types of memory store data as a charge state. Charge storage memory is gradually approaching the physical limits of scalability, and conceptually new types of memories based on a different storage principle are gaining momentum. Some of the technologies are already available as prototype (such as carbon nanotube RAM (NRAM), copper bridge RAM (CBRAM)), others as product (phase change RAM (PCRAM), magnetoresistive RAM (MRAM), ferroelectric RAM (FRAM)), while the technologies of spin-torque transfer RAM (STTRAM), racetrack memory, and resistive RAM (RRAM) are under research. Apart from good scalability, a new type of memory must also exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and simple structure [1, 2] .

Nonvolatile memory (NVM) technology is playing an increasingly important role in microelectronic devices. One of the most promising candidates for future NVM is memory using as basic principle of operation the phenomenon of resistive switching. This phenomenon is observed in different types of insulators, such as metal oxides, perovskite oxides, solid-state electrolyte, and chalcogenide materials. The electrical conductance of the insulator can be set at different levels by the application of an electric field. Indeed, a state with high resistance (HRS) can be interpreted as logical 1 and a state with low resistance (LRS) as logical 0, or vice versa, depending on the application. The concepts of memory using the resistive switching phenomenon can be conveniently divided into the following three categories: CBRAM, PCRAM, and RRAM. These concepts possess the simplest metal-insulator-metal (MIM) structure and, as a consequence, have good scalability. This fact gives advantages to CBRAM, PCRAM, and RRAM over other advanced memory concepts. In addition to its simple structure RRAM is characterized by a low operating voltage (< 2 V), fast switching time (< 10 ns), high density, and long retention time.

RRAM is based on metal oxides, such as TiO_x [3–6], HfO_2 [7], Cu_xO [8], NiO [9], ZnO [10], and perovskite oxides, such as doped $SrTiO_3$ [11], doped $SrZrO_3$ [12], $Pr_{1-x}Ca_xMnO_3$ [13], and employs the electric field induced difference in resistivity between the HRS and the LRS.

Several physical mechanisms based on either electron or ion switching have been recently suggested in the literature: a model based on trapping of charge carriers [14], electrochemical migration of oxygen vacancies [15, 16], electrochemical migration of oxygen ions [17, 18], a unified physical model [19, 20], a domain model [21], a filament anodization model [22], a thermal dissolution model [23], a two-variable resistor model [24], and others. However, a proper fundamental understanding of the RRAM switching mechanism is still missing, hindering further development of this type of memory.

We propose a stochastic model of the resistive switching mechanism based on electron hopping between the oxygen vacancies along the conductive filament in an oxide-layer.

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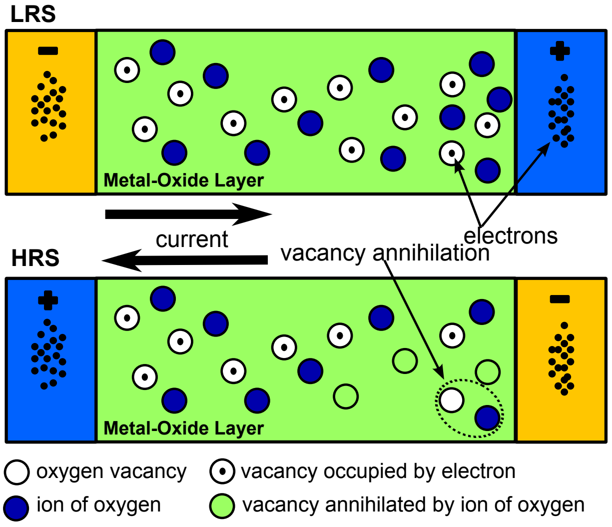

Figure 1. Schematic illustration of the conducting filament in the low resistance state (top) and the high resistance state (bottom).

II. MODEL DESCRIPTION

We associate the resistive switching behavior in oxide-based memory with the formation and rupture of a conductive filament (CF). The CF is formed by localized oxygen vacancies (V_o) [19, 20] or domains of V_o (Fig. 1). Formation and rupture of a CF is due to a redox reaction in the oxide layer under a voltage bias. The conduction is due to electron hopping between these V_o.

For modeling the resistive switching in bipolar oxide-based memory by Monte Carlo techniques, we describe the dynamics of oxygen ions (O^{2-}) and electrons in an oxide layer as follows:

- formation of V_o by O^{2-} moving to an interstitial position;
- annihilation of V_o by moving O^{2-} to V_o;
- an electron hop into V_o from an electrode;
- an electron hop from V_o to an electrode;
- an electron hop between two V_o.

In order to model the dependences of transport on the applied voltage and temperature we choose the hopping rates for electrons as [25]:

$$\Gamma_{nm} = A_e \cdot \frac{dE}{1-\exp(-dE/T)} \cdot \exp(-R_{nm}/a) \qquad (1)$$

Here, A_e is a coefficient, $dE=E_n-E_m$ is the difference between the energies of an electron positioned at sites n and m, R_{nm} is the hopping distance, a is the localization radius. The hopping rates between an electrode (0 or $N+1$) and an oxygen vacancy m are described as:

$$\Gamma_m^{iC} = \alpha \cdot \Gamma_{0m}, \Gamma_m^{oC} = \alpha \cdot \Gamma_{m0} \qquad (2)$$

$$\Gamma_m^{iA} = \beta \cdot \Gamma_{(N+1)m}, \Gamma_m^{oA} = \beta \cdot \Gamma_{m(N+1)} \qquad (3)$$

Here, α and β are the coefficients of the boundary conditions on the cathode and anode, respectively, N is the number of sites, A and C stand for cathode and anode, and i and o for hopping on the site and out from the site, respectively.

To describe the motion of ions we have chosen the ion rates similar to (1):

$$\Gamma_n^{'} = A_i \cdot \frac{dE}{1-\exp(-dE/T)} \qquad (4)$$

Here we assume that O^{2-} can only move to the nearest interstitial. A distance-dependent term is thus included in A_i. dE includes the formation energy for the m-th V_o /annihilation energy of the m-th V_o, when O^{2-} is moving to an interstitial or back to V_o, respectively.

The current generated by hopping is calculated as:

$$I = q_e \cdot \frac{\sum dx}{\sum\left(\sum_m \Gamma_m\right)^{-1}} \qquad (5)$$

Here q_e is the electron charge, dx is the hopping distance.

III. RESULT AND DISCUSSION

Despite the fact that in the binary metal oxides oxygen vacancies can have three different charge states with charge 0, +1, +2 [26], to simplify the calculations, we assume that the oxygen vacancy is either empty or occupied by one electron. This assumption is not a limitation; however, due to the energy separation between the three charge states: only two of them will be relevant for hopping and significantly contribute to transport.

A. *Calculation of electron occupation probability*

For comparison with the previous work [20] all

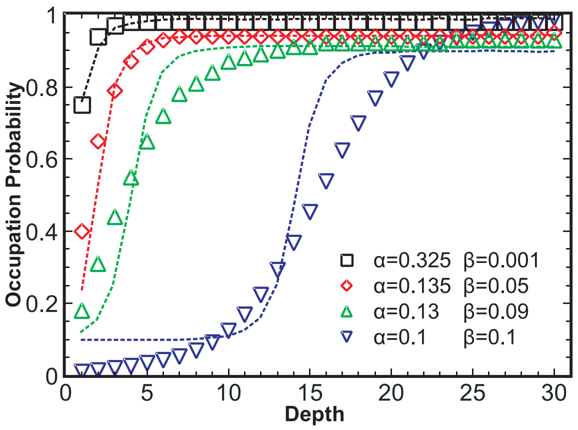

Figure 2. Calculated distribution of electron occupation probabilities under different biasing voltages. Lines are from [20], symbols are obtained from our stochastic model.

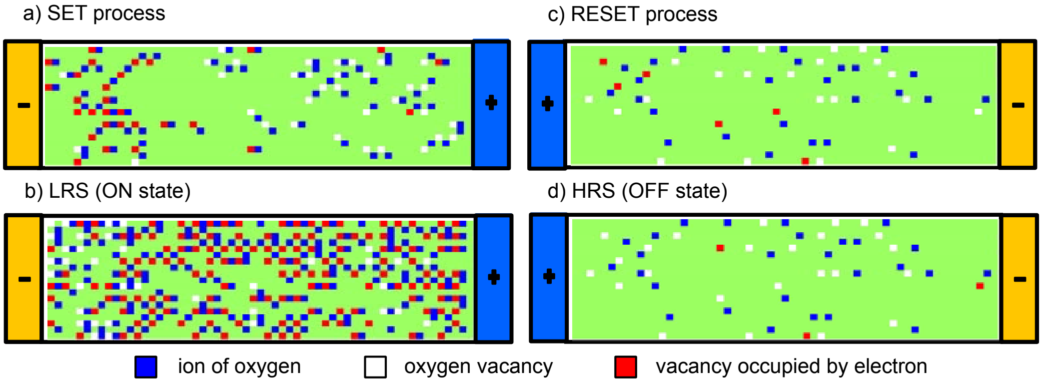

Figure 3. Modeling of the resistive switching mechanism in bipolar oxide-based memory cell: (a) SET process. (b) the conducting filament in the low resistance state (ON state). (c) RESET process. (d) the conducting filament in the high resistance state (OFF state). Only the oxygen vacancies and ions which impact the resistive switching are shown.

calculations in this subsection are made on a one-dimensional lattice consisting of thirty equivalent, equidistantly positioned hopping sites V_o.

We have calibrated our model in a manner to reproduce the results reported in [20], for V=0.6 V to V=1.4 V. Fig. 2 shows a case, where the hopping rate between two V_o is larger than the rate between the electrodes and V_o (α, $\beta < 1$). In this case a low occupation region is formed near the cathode (bipolar behavior).

B. Modeling the resistive switching

Modeling of the resistive switching in this subsection and all calculations of RRAM *I-V* characteristics are now performed on a two-dimensional lattice (*10×30*). We have investigated the process of the resistive switching by applying a voltage V with a saw-tooth like time dependence. The coefficients of the boundary conditions are constant and taken to be equal to 0.1.

Fig. 3 shows states of the model system during a full cycle of switching from HRS to LRS and back. In the first moment of time we assume that there are no vacancies $V_{o.}$ in the system. If a positive voltage is applied, the formation of a CF begins, when the voltage reaches a critical value sufficient to create V_o by moving O^{2-} to an interstitial position (Fig. 3a). During the SET and the RESET process each O^{2-} has a probability Γ'_n of moving to the nearest interstitial position (if this position is empty); moreover, each O^{2-} has a probability Γ'_n of annihilation with the nearest V_o , provided this V_o is not occupied by an electron. In addition, the dynamics of electrons according to (1-3) on the vacancies V_o already formed is taken into account giving rise to the electron current in the system. The formation of the CF leads to a sharp increase in the current signifying a transition to a state with low resistance (Fig. 3b and Section 1 of the *I-V* in Fig. 4). If we continue applying the positive voltage, the number of V_o will continue to grow which in our model can cause an unrecoverable breakdown of the insulator and further denial of switching to a state with high resistance. When a reverse negative voltage is applied, the current increases linearly, until the applied voltage reaches the value at which an annihilation of V_o is triggered by means of moving O^{2-} to V_o (Fig. 3c). The CF is ruptured and the current decreases. This is the transition to the state with high resistance (Fig. 3d, Section 3 in Fig. 4).

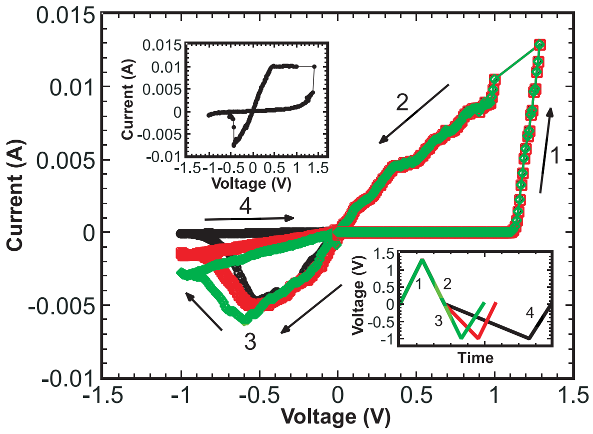

Figure 4. *I-V* characteristics showing the hysteresis cycle obtained from the stochastic model for different reset times. The inset (bottom) shows a schematic illustration of applying a voltage V. The inset (top) shows the hysteresis cycle for *M*-ZnO-*M* from [10].

C. Modeling of the time dependence RESET process

The modeling procedure is the same as it is described in the previous subsection. The simulated RRAM switching hysteresis cycle is shown in Fig. 4. The simulated cycle is in agreement with the experimental cycle from [10] shown in the inset in Fig. 4 (top).

In order to investigate the dependence of the RESET process on the time the voltage is applied, we use the same voltage amplitude V but different time intervals. A schematic illustration of voltages V applied is shown in the inset in Fig.4 (bottom). Results displayed in Fig. 4 clearly indicate that the proper CF rapture during the RESET process is achieved, when the product "voltage-time" is maximal.

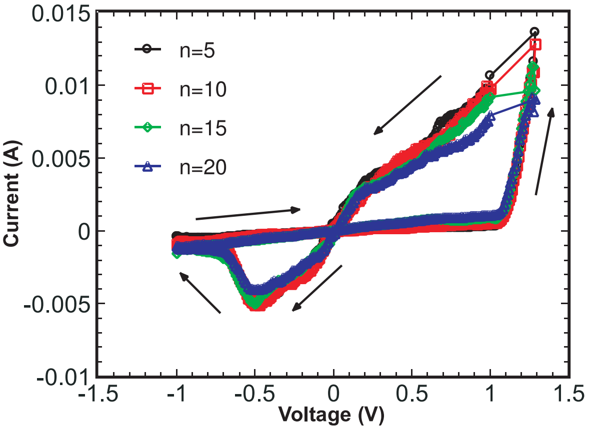

Figure 5. Multicycle *I-V* characteristics showing the hysteresis cycle obtained from the stochastic model after 5, 10, 15, and 20 cycles.

D. *Modeling of reproducible hysteresis cycles*

For modeling multicycle *I-V* characteristics we have used a saw-tooth like voltage *V,* where the product "voltage-time" is maximal. Fig. 5 shows the hysteresis cycle obtained from our generalized stochastic model after 5, 10, 15, and 20 cycles.

The attenuation of the hysteresis with the number of cycles indicates that parameters used are not optimal. Our generalized stochastic model allows enhancing RRAM endurance by properly tailoring the parameters of the cell.

IV. CONCLUSION

We have developed a stochastic model of the resistive switching mechanism. The results of our simulations are in excellent agreement with previous theoretical and experimental work. The simulated RRAM switching hysteresis cycle is in good agreement with the experimental data. The proposed stochastic model can be used for better understanding resistive switching in RRAM.

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