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Non-Linearity of Transconductance and Source-Gate Resistance of HEMTs

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***Abstract*— Experimental results from GaN-based high electron mobility transistors (HEMTs) show a pronounced decrease of the transconductance g_m at higher gate bias, due to increasing source-gate and gate-drain resistances. In this work we show through simulations that the electric field distribution and the resulting carrier velocity quasi-saturation are the main source for the transconductance collapse, consequently also for the resistance rise. A shorter source-gate distance leads to a higher g_m peak value, but a more abrupt collapse at high gate bias. These effects are further discussed with respect to device linearity.**

I. Introduction

Wide bandgap GaN-based high electron mobility transistors (HEMTs) are suitable for radio-frequency applications due to their excellent power properties. The focused extensive investigations in recent years have solved various technology issues and vastly improved the device performance [1],[2]. However, several difficulties still hamper the wide use of HEMTs, one of them being the very strong dependence of the transconductance on the gate voltage. As the derivatives of the transconductance with respect to the gate voltage are detrimental to intermodulation distortion [3], [4], a profound knowledge of the causes for the transconductance non-linearity significantly helps the selection of a proper load resistance. The problem has been addressed in numerous works (e.g. [5], [6]). Interface roughness and hot-phonon scattering have been ruled out as possible reasons for the strong dependence of transconductance on gate voltage. While real space transfer effects are relevant in GaAs-based pHEMTs [7], the lack of a significant leakage current in the studied structures counts against it. Recently, the decrease of transconductance has been attributed to the strong non-linearity of the source-gate resistance. This has been shown in a couple of studies relying on experimental measurements combined with simulations [5], [6]. Both of them employ specially tailored carrier velocity − electric field characteristics. In this work, a good agreement with experimental data is achieved by using a general model based on Monte Carlo (MC) simulation results. We study the electron transport in the source-gate and gate regions in a wide range of gate-source voltages (V_{GS}), and also discuss the impact of scaling the source-gate distance L_{SG} on transistor performance. We show, that the transconductance decrease should not be attributed to negative differential mobility effects, and is also reproduced by using a velocity-field characteristics conform to MC simulation results.

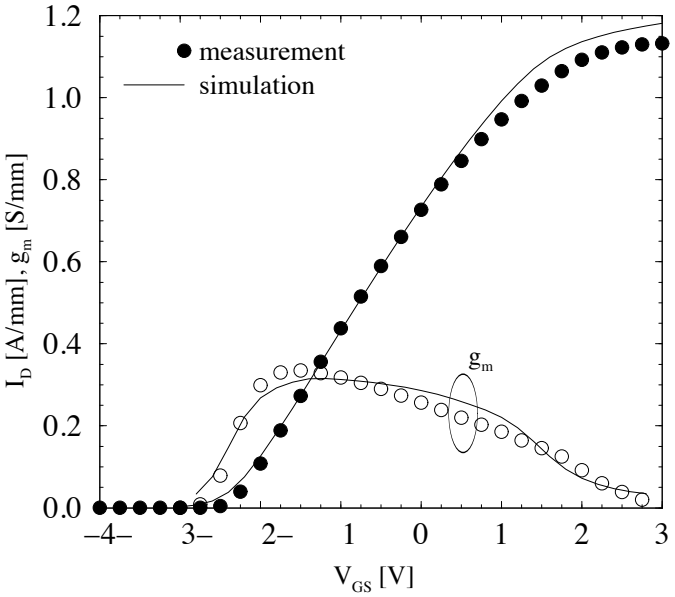

Fig. 1. Drain current and transconductance at V_{DS}=7 V: measured data compared to simulation.

II. Device Description

The epitaxial structures used in this work were grown by metal-organic chemical vapor deposition (MOCVD) on 3-inch semi-insulating SiC substrates. The layers consist of a highly-resistive c-plane GaN buffer, followed by a 22 nm thick $Al_{0.22}Ga_{0.78}N$ barrier and finally a 3 nm thin GaN cap layer. The nitride-assisted 0.25 μm T-gate was defined by e-beam lithography. We perform two-dimensional hydrodynamic simulations with our device simulator Minimos-NT, which proved to be a suitable tool for the analysis of heterostructure devices [8]. The set of models and model parameters in use was employed for the optimization of several generations of GaN-based HEMTs [9], [10].

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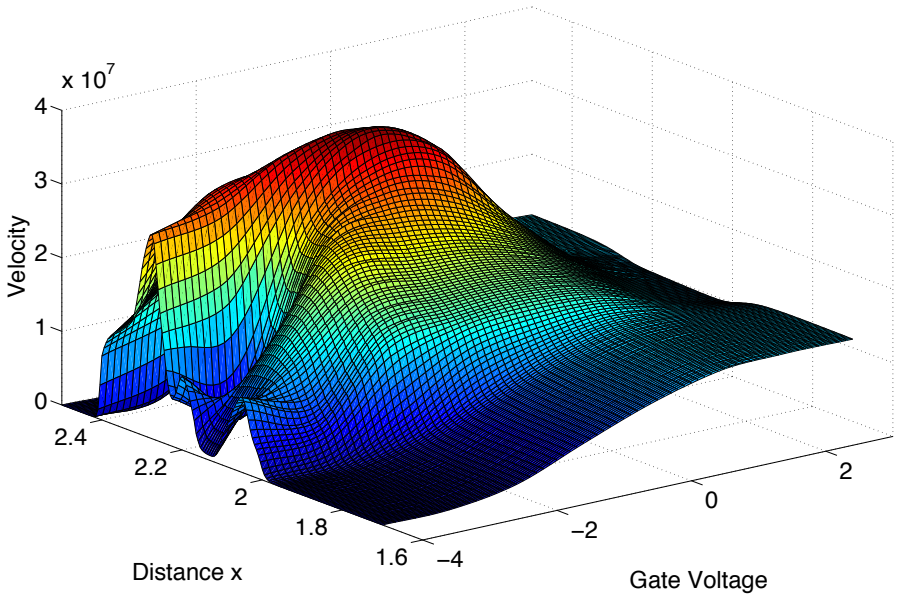

Fig. 2. Electron velocity along the channel [cm/s].

III. Simulation Results

Fig. 1 shows the measured and simulated transfer characteristics of the device. A good agreement is achieved for the drain current as well for the transconductance, without any changes in the models or model parameters. The simulated transconductance exhibits roughly the same maximum value as the measurement, and adequately follows the decrease at higher gate voltage. In order to gain a better understanding of the carrier transport process in the device, the transconductance can be expressed as:

$$g_{\mathrm{m}} = \frac{\Delta I_{\mathrm{D}}}{\Delta V_{\mathrm{GS}}} = \left(\frac{\Delta n}{\Delta V_{\mathrm{GS}}}\right) ev + \left(\frac{\Delta v}{\Delta V_{\mathrm{GS}}}\right) ne. \qquad (1)$$

The first term describes the contribution of the change in carrier concentration Δn (e is the electron charge). Our simulations show that it is substantial only under the gate, as in the source-gate and gate-drain areas only minor variation of the carrier concentration with $\mathrm{V_{GS}}$ is observed. The rapid increase in concentration in the bias range near the maximum transconductance combined with a high electron velocity (Fig. 2) indeed results in some contribution of this term to the overall $\mathrm{g_m}$. However, this contribution is limited to a small area under the gate in a narrow voltage range, therefore for the further studies we focus primary on the second term - the change in carrier velocity Δv.

Fig. 2 shows the velocity along the channel of the device for $\mathrm{V_{GS}} = -4$ V and 3 V (gate is from x=2.0 μm to x=2.25 μm). There are two distinguishable regions: the source-gate region and the effective gate region ($\mathrm{L_{G,eff}}$). The latter exhibits a high velocity up to $\mathrm{V_{GS}} = -1$ V, which then decreases abruptly. This is to be attributed entirely to the electric field profile, which is depicted in Fig. 3. The complex form at low $\mathrm{V_{GS}}$ is due to the negative differential velocity at high electric fields, for which our model accounts. As the channel under the gate is entirely depleted at this bias, there is no notable effect on the DC characteristics of the device. The flat distribution of the product Δvn (second term in Eq. 1) in the gate region as shown in Fig. 4 confirms this theory.

In the source-gate region a steady increase of the velocity is observed between $\mathrm{V_{GS}} = -3$ V and 0 V, which corresponds to the increase in the electric field. Notably, the electron velocity is very low for $\mathrm{V_{GS}} < -3$ V and almost constant over 1 V. The resulting product Δvn shows a distribution which is very similar to the transconductance characteristics. Notably, the decrease of the electric field and, consequently, of the electron velocity under the gate at $\mathrm{V_{GS}} \approx 0$ V produces a significant negative region. Further, the electron mobility in the source-gate region decreases significantly with higher $\mathrm{V_{GS}}$, which results in the higher source-gate resistance.

Based on those observations several conclusions are self-evident:

- electron velocity at low electric fields in the source-gate region has the highest impact on the transconductance,
- the decrease of transconductance is due to the quasi-saturation of the electron velocity in the source-gate region, due to the reached maximum electric field in this region,
- at very high gate bias the electric field suppresses further the velocity under the gate and causes the secondary collapse of the transconductance.

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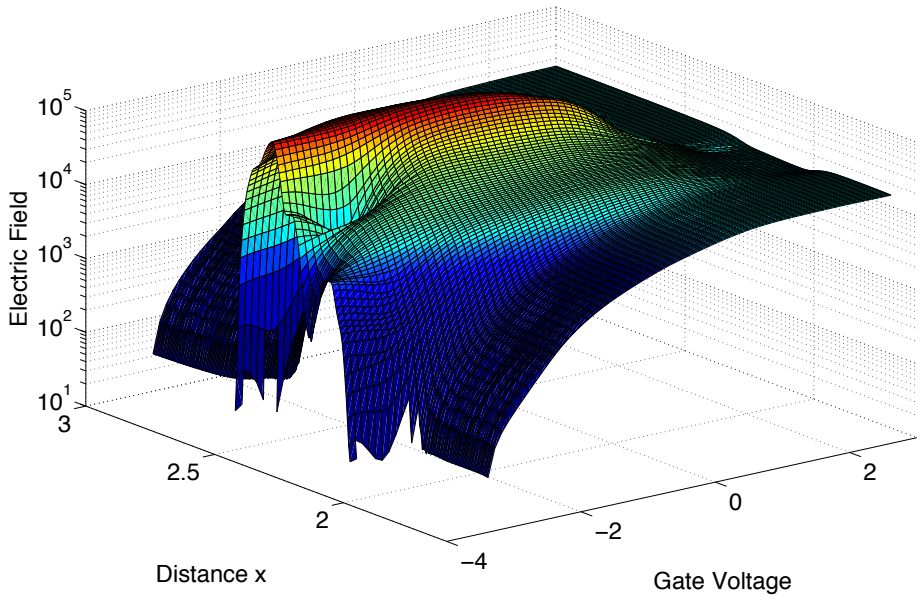

Fig. 3. Electric field along the channel [V/cm].

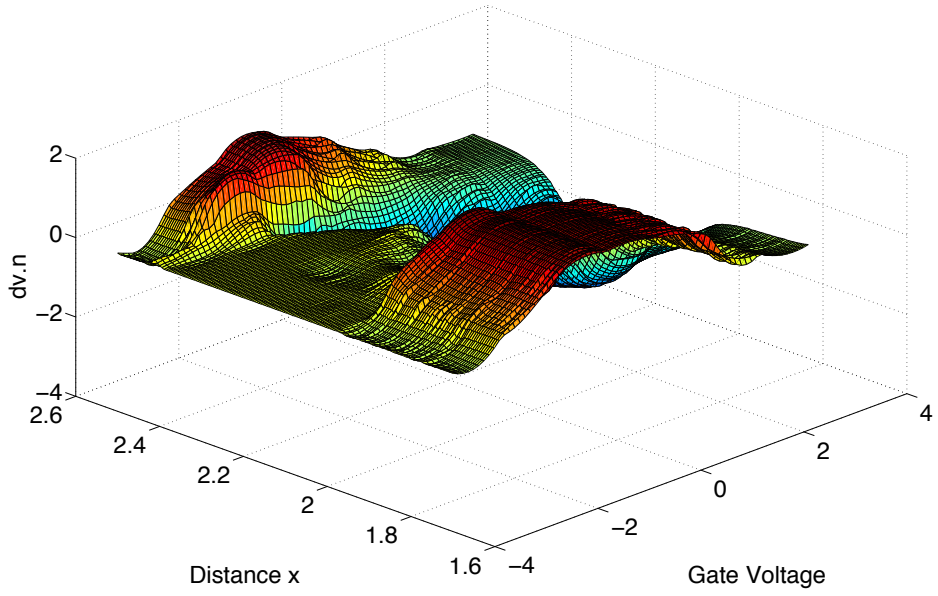

Fig. 4. Δvn (scaled) along the channel [$\mathrm{cm}^{-2}\mathrm{s}^{-2}$].

IV. Source-Gate Distance Scaling

Some authors have pointed out the positive effects of downscaling the source-gate distance (L_{SG}) on the transconductance [6], [11]. Based on the structure described above, we introduce four more devices, which share the same geometry except for the source-gate distance: one device with a source-gate distance by 0.2 μm longer than the nominal value (L_{SG}+0.2 μm), and three devices with source-gate distances shorter by 0.2−0.6 μm than the nominal value ($L_{SG} - 0.2/0.4/0.6$ μm). In agreement with previous works, decreasing the source-gate distance results in a higher peak transconductance (Fig. 5). Also, with shorter distance a flatter peak is achieved. These improvements are however at the cost of a transconductance collapse at lower V_{GS}. In order to find the source of this effect once again we study the impact of the carrier velocity and concentration separately as in Eq. 1.

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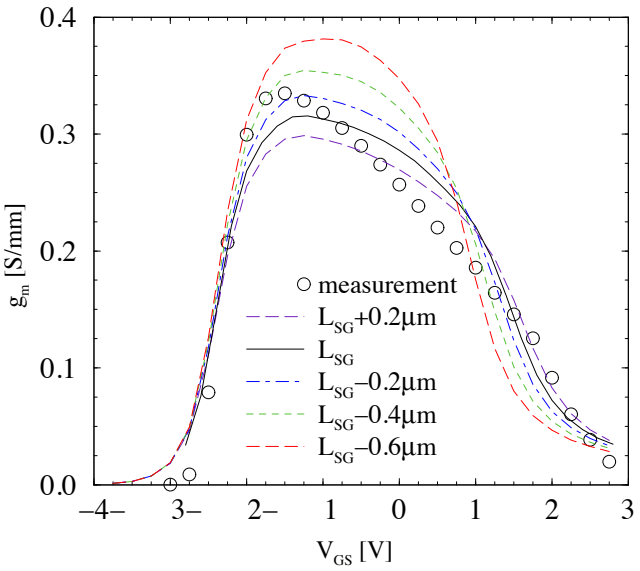

Fig. 5. Transconductance g_m vs. gate voltage V_{GS} for five devices with different source-gate length (V_{DS}=7 V).

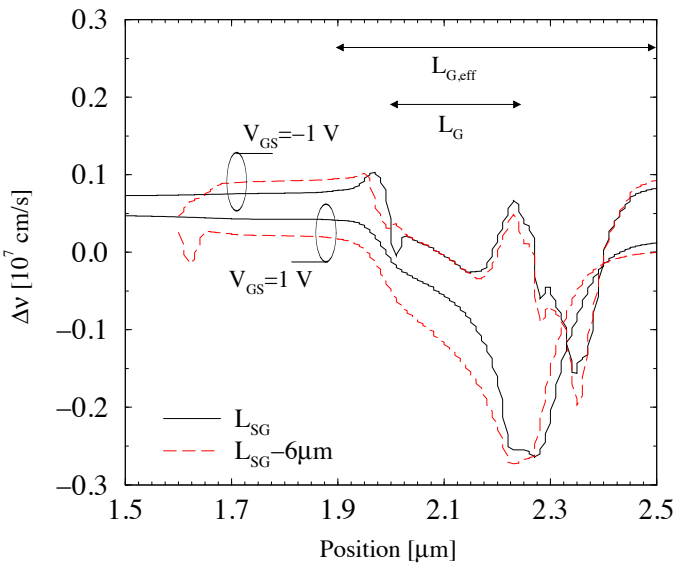

Fig. 6. Change of electron velocity Δv along the channel at V_{GS} of -1 V and 1 V for two devices with different L_{SG}.

Our simulations show that the change of carrier concentration $\Delta n/\Delta V_{GS}$ is roughly equal for devices with shorter L_{SG}, thus the different transconductance characteristics is due to the different change of the electron velocity with gate bias $\Delta v/\Delta V_{GS}$. Fig. 6 shows the velocity change in the device described in Section 2 (nominal L_{SG} and a device with a L_{SG} shorter by 0.6 μm for two gate voltages $V_{GS} = -1$ V and $V_{GS} = 1$ V. The former corresponds to the peak g_m, in which point the transconductance of the shorter device is higher. The reason is the higher Δv in the source-gate region of the smaller device, due to the considerably higher electric field. In the second point (V_{GS}=1 V) Δv in the shorter device is lower overall, thus the lower g_m. It must be noted that Δv is lower not only in the source-gate region due to reaching the maximum velocity earlier, but also in the region under the gate. There the electric field decreases more rapidly in the shorter structure, which results in the lower value of Δv.

Our results show, that the transconductance can be extensively tailored by appropriate scaling of the source-gate distance. However, down-scaling of L_{SG} is limited by breakdown effects. Contrary to other studies we do not support the introduction of channel implantation or a n^{++} cap layer, as the higher donor concentration deteriorates the electron mobility and is in contradiction with the basic HEMT mechanics. Last, we show that with a carefully calibrated setup various effects can be successfully explored.

V. Conclusion

We present a study of the transconductance collapse in GaN-based HEMTs. The main reasons are found to be the electron velocity quasi-saturation due to the electric field profile in the source-gate region and the velocity decrease under the gate. Further, we explore the effect of reducing the source-gate distance and study the improved transconductance. The possibility to tailor the device transconductance gives a novel approach to effectively improve device linearity.

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