HC degradation model: interface state profile – simulations vs. experiment

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Hot-carrier (HC) degradation remains one of the most critical reliability issues in MOS transistors. HC degradation is commonly associated with the build-up of traps at the Si/SiO_2 interface due to Si-H bond-breakage triggered by "hot" carriers. For non-scaled devices the interface state generation is dominated by a single-particle process while for scaled devices the multiple-particle process dominates [2,3]. Thus even when the device dimensions are extremely scaled the expected halt of degradation is not observed. Therefore, the key issue in the modelling of HC degradation is the information about carrier distribution over energy. We have already presented [3] a model for HC degradation based on a carrier distribution function (DF) evaluation by means of a full-band Mote-Carlo device simulator [4]. There, the interface state profiles (the concentration N_{it} vs. the coordinate along the interface x) were already obtained as result of the model and used in our device simulator MINIMOS-NT [5] to simulate output characteristics of degraded device. However, at that stage we were not yet able to compare the predicted profiles with real N_{it} profiles obtained for instance by the charge-pumping (CP) technique [6]. This will be done in the following, thereby demonstrating the correctness of our modeling approach.

Low voltage n-MOSFETs fabricated on a standard 0.35 μm technology (Fig. 1) were stressed for $t = 10^5$ s at the gate and drain voltages of $V_{gs} = 2.0$ V and $V_{ds} = 6.75$ V. The chuck temperature was $T = 40$ °C. The experimental transfer characteristics are well reproduced by MINIMOS-NT (Fig. 1, inset).

To obtain experimental N_{it} profiles a CP technique with a constant base level V_{gl} and varying high level V_{gh} of the gate pulses has been employed [7,8]. The pulse frequency is 25 kHz. Using the approach proposed by Tsuchiaki et al [9] we have extracted the dependences of the flat-band V_{fb} and threshold V_t voltages on x for the "fresh" device (Fig. 2, upper inset). The soundness of this approach was checked by calculating these curves with MINIMOS-NT using the widely-adopted routine [6] based on the concept of free electron/hole interface concentration for V_t and V_{fb} evaluation. For the extraction of the N_{it} profiles from CP data we used a standard procedure based on the effective channel length variations when gate pulses are applied [7,8]. The family of N_{it} profiles for different stress times is depicted in Fig. 3. These profiles demonstrate a peak at the end of the gate electrode shifted respectively the maximum of the electric field (Fig.2, lower inset).

The experimental N_{it} profiles are reproduced by our model for interface trap generation [3], Fig. 3. The model is based on the carrier acceleration integral (AI) which is coordinate-dependent and obtained by integrating the DF weighted with the Si-H bond-breakage cross section and the density-of-states over energy. Note that the peak of N_{it} just coincides with the peak of the AI (not depicted here). The agreement between experiment and theory may be refined by more thorough calculation of the DF with a smaller step by x in the vicinity of the N_{it} peak.

Conclusion: We have undertaken a direct comparison between the experimental interface state density profile generated during HC stress and that simulated with our model and obtained a good agreement between experiment and theory.

References

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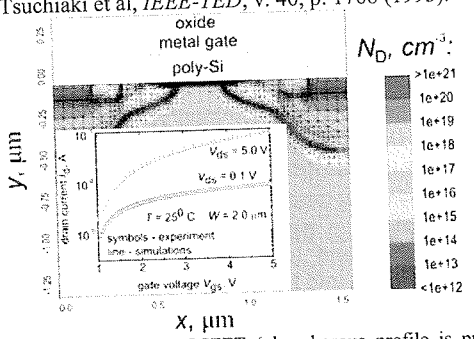

Fig.1. The topology of n-MOSFET (phosphorous profile is present). Inset: the transfer characteristics (experiment vs. simulations)

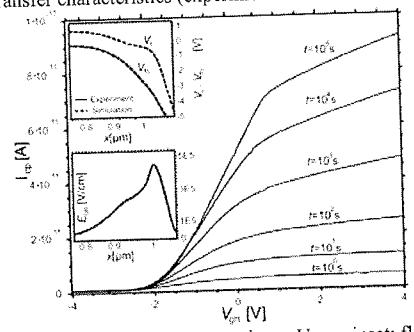

Fig.2. The CP current for several stress times. Upper inset: flat-band and threshold voltages. Lower inset: the electric field vs. the coordinate x.

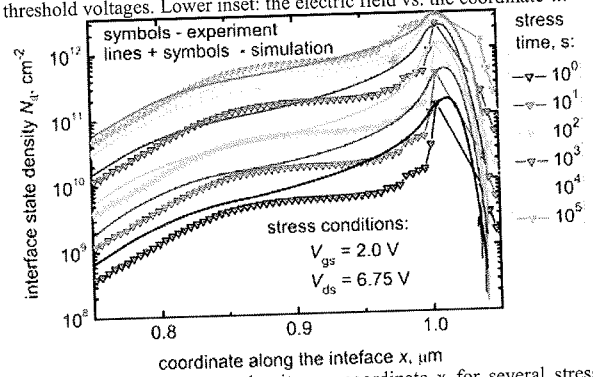

Fig. 3. The interface state density vs. coordinate x for several stress times experiment vs. theory.