Modeling Floating Body Z-RAM Storage Cells

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Abstract— **Advanced floating body Z-RAM memory cells are studied. In particular, the scalability of the cells is investigated. First, a Z-RAM cell based on a 50nm gate length double-gate structure corresponding to state of the art technology is studied. A bi-stable behavior essential for Z-RAM operation is observed even in fully depleted structures. It is demonstrated that by adjusting the supply source-drain and gate voltages the programming window can be adjusted. The programming window is appropriately large in voltage as well as in current.**

We further extend our study to a Z-RAM cell based on an ultra-scaled double-gate MOSFET with 12.5nm gate length. We demonstrate that the cell preserves its functionality by providing a wide voltage operating window with large current differences. An appropriate operating window is still observed at approximately 25-30% reduced supply voltage, which is an additional benefit of scaling. The relation of the obtained supply voltage to the one anticipated in an ultimate MOSFET with quasi-ballistic transport is discussed.

I. INTRODUCTION

Standard DRAM cell scaling is hampered by the presence of a capacitor which is difficult to reduce in size. Recently, a revolutionary concept of a DRAM memory cell based on a transistor alone was introduced [1–8]. The ultimate advantage of this new concept is that it does not require a capacitor, and, in contrast to traditional 1T/1C DRAM cells, it thus represents a 1T/0C cell named Z (for zero)-RAM.

Although based on the two states of a MOSFET with different threshold voltages, the working principle of a Z-RAM cell is different from that of flash memory cells. Flash memory is based on a MOSFET with two gates. In addition to the top control gate used to open and close a MOSFET, the second gate called floating gate can trap charges. The floating gate is insulated from the channel and the control gate and may retain the trapped charge for years. A charge stored in the floating gate alters the threshold voltage of the cell. Depending on the amount of charge in the floating gate the MOSFET may be in an open or closed state at a given voltage at the control gate. Single-level cells are able to store one bit of information, while multi-level cells allow to store more than one bit per cell by choosing between multiple levels of electrical charge in the floating gate of a cell. Charging of the floating gate is performed by hot-electron injection or by quantum mechanical tunneling through the potential barrier of a dielectric insulating the floating gate from the channel. Flash memory cells store the charge in a polysilicon floating gate. Due to electrical interference between adjacent cells, caused by the electric field of the electrons stored in the polysilicon gates, it is difficult to scale the floating gate cells beyond 45 nm technology node [9].

Replacement of the flash stack by a SONOS charge trapping stack allows to continue scaling [10]. In SONOS devices the floating gate is replaced by a non-conductive nitride layer with a high density of deep charge trapping sites able to store the charge. SONOS is not susceptible to drain turn-on and floating gate interference. The gate stack of SONOS is up to $\sim 50\%$ thinner as compared to flash. SONOS stacks offer a higher quality charge storage due to the smooth homogeneity of the nitride film compared to the polycrystalline film of flash and are less prone to oxide defects. Because of the insulating nature of the nitride film, a leakage path is usually locally confined and only able to affect a few traps. Therefore, SONOS is less sensitive to stress induced leakage currents, when the bottom oxide layer is thinner than in flash. A thinner oxide layer enables faster programming and lower write/erase voltages.

Recently a 10 nm bulk-planar SONOS type memory cell with a double tunnel junction, exhibiting good scalability while offering low write/erase voltages and excellent charge retention characteristics at the same time was demonstrated [11]. To increase the gate coupling factor silicon dioxide between the gates should be replaced with a high-k material. For charge trapping devices also high-k materials are needed as blocking oxides between the trap layer and the control gate. This demands high-k materials with large band gaps and band offsets,which limits the materials of choice and restricting the permittivity values in the moderate range from $\sim 9 - 20$ [12].

Contrary to flash memory cells, a Z-RAM cell does not contain an extra floating gate and is based on an SOI MOSFET alone. The functionality of the first generation Z-RAM is based on the possibility to store the majority carriers in the floating body. The carriers are generated by impact ionization caused by the minority carriers close to the drain. The threshold voltage is modified because of the charge accumulated in the body

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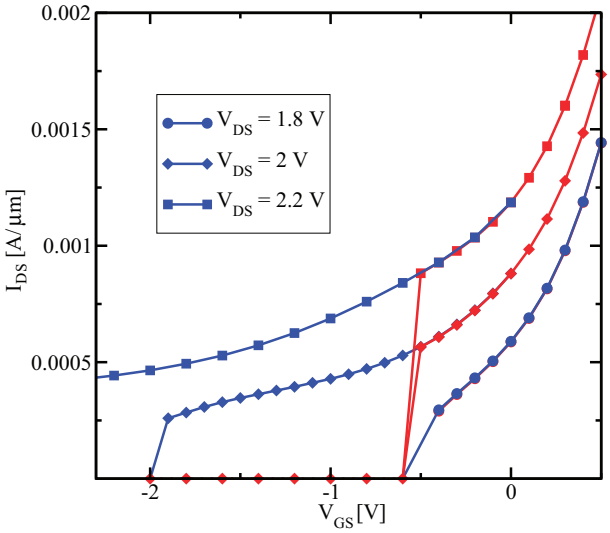

Fig. 1. $I_{DS} - V_{GS}$ for a 50nm double gate MOSFET with silicon body thickness 10nm for different source-drain voltages V_{DS}. The hysteretic behavior is clearly observed for V_{DS} = 2.0V, while for V_{DS} = 2.2V the transition to the low current state is not observed even for $V_{GS} \approx$-2V.

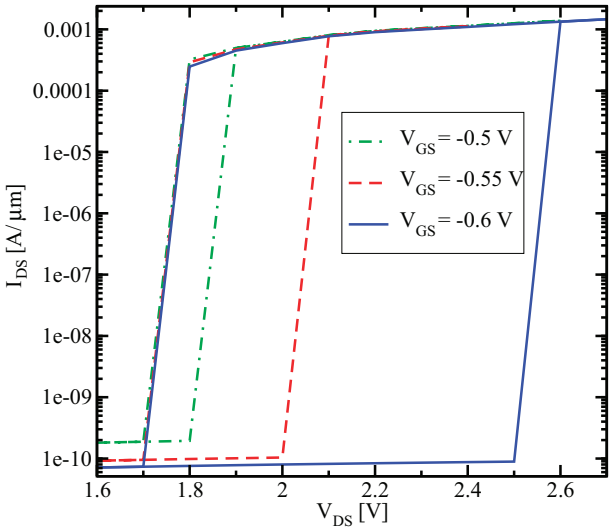

Fig. 2. $I_{DS} - V_{DS}$ in a logarithmic scale for a 50nm double gate MOSFET with silicon body thickness 10nm, for different gate voltages V_{GS}. Hysteresis behavior is clearly observed for V_{GS} =-0.6V and V_{GS} =-0.55V, while it is nearly extinct at V_{GS} =-0.5V.

thus guaranteeing the two states of a MOSFET channel, open and close, for a gate voltage chosen between the two thresholds.

Already the first generation Z-RAM is characterized by the two current values corresponding to the two logical states sufficient for applications [1]. In order to increase the size of the programming window one can use not only a MOSFET but also a bipolar transistor which is known to exist in SOI MOSFETs [21]. The bipolar transistor is usually considered as parasitic: when opened it hinders the functionality of the field-effect transistor.

The idea of the second generation Z-RAM is to exploit the properties of the bipolar transistor [13], allowing to expand the Z-RAM applicability to such of advanced non-planar devices as FinFETs, multi-gate and gate-all-around FETs. Contrary to the first generation, the current is flowing through the body of the structure. This increases the value of current by roughly the ratio of the fin radius to the surface layer thickness. The majority carriers are generated due to impact ionization. They are stored under the gate at the silicon/silicon dioxide interface. The stored charge provides good control over the bipolar current, in contrast to the first generation Z-RAM where the charge was stored in the area close to the buried oxide.

While keeping all advantages of the first Z-RAM generation, the most recent generation of Z-RAM cells [13] is characterized by a significantly enlarged programming window and much longer retention times. Recently, a 128Mb floating body RAM was designed and developed [8].

With CMOS downscaling continuing the question obviously arises, whether a Z-RAM cell is also scalable. The goal of our study is to demonstrate that a Z-RAM cell preserves its functionality and remains operational for scaled MOSFETs.

In order to reach this goal, several issues must be addressed. Multi-gate FETs and finFETs are the most promising candidates for the upcoming CMOS MOSFETs beyond the 22nm technology node. The functionality of both generations of Z-RAM cells on partially depleted SOI structures was recently demonstrated [13]. With channel length reduced, maintaining control over the channel becomes increasingly challenging, and several measures must be taken to preserve it. Apart from improving electrostatic control by downscaling oxide thickness, the channel width can be reduced. This is achieved by artificially confining carriers within an ultra-thin silicon film. Due to the small dimensions of the silicon body there will be only few impurities inside. This results in unacceptably large threshold voltage fluctuations [14]. Fully depleted double-gate MOSFETs with undoped intrinsic silicon body are perfectly functionable [15,16]. They preserve a good channel control, reasonable DIBL, large I_{on}/I_{off} ratio, and gain down to a channel length as short as 5nm [17]. It has recently been demonstrated that the functionality of a Z-RAM cell based on a fully depleted scaled MOSFET is preserved [18].

Because of the importance of impact ionization, the source-drain voltages are higher for Z-RAM operation, namely for writing, than for CMOS logic. An important question is whether this voltage can be reduced while scaling the device down. We demonstrate that, as for CMOS devices, this is generally true. Calcu-

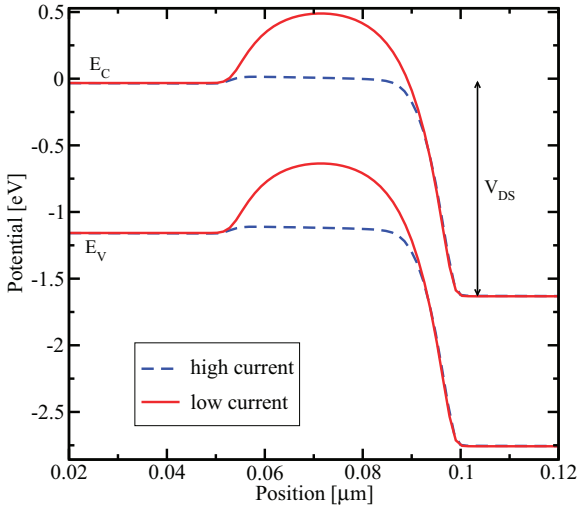

Fig. 3. Cross section of the potential energy from the source to the drain along the middle of the channel in a 50nm double gate MOSFET at V_{GS} = -1V and V_{DS} =2V. The potential barrier is high in the low current state, and the transistor is closed. In the high current state there is no barrier, and the transistor is opened.

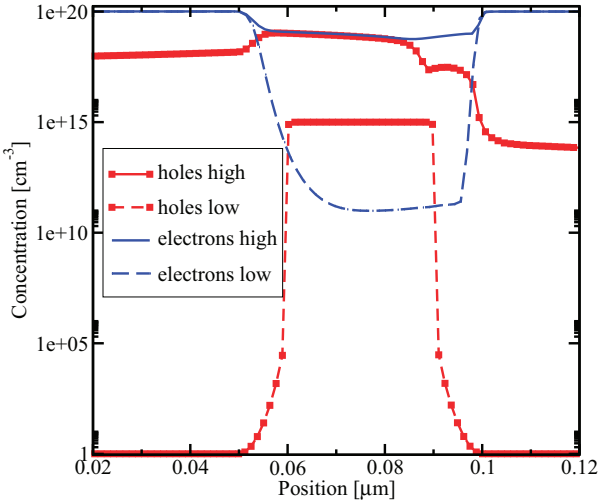

Fig. 4. Cross section of the electron and hole concentrations along the middle of the channel in a 50nm double gate MOSFET at V_{GS} =-1V and V_{DS} =2V for the two current states. The higher majority carrier concentration in the channel in the high current state is due to holes captured in the potential wells clearly seen in Fig. 3 under the gates.

lated voltages for scaled Z-RAM cells are around 1.4V. This value is also in agreement with the writing voltage in a quasi-ballistic MOSFET with an ultra-short channel, which is considered as a good candidate for an ultimate MOSFET [14]. The value is higher than the projected supply voltage for upcoming MOSFETs. However, the current prototypes of a Z-RAM cell operate now at 2.2V [13]. Therefore, a decrease in supply voltage to 1.4V is significant.

II. STRUCTURES

For our analyses we have chosen two double-gate structures. One structure has a gate length of 50nm and a lightly doped ($N_A = 10^{15}\text{cm}^{-3}$) Si body of 10nm thickness. We have used metal gates with mid-gap work function and oxide with equivalent thickness of 2nm. Source and drain extentions are heavily doped to $N_D = 10^{20}\text{cm}^{-3}$ in order to provide enough injected electrons. This structure corresponds to the current technology node [19].

The scaled double-gate structure has a gate length of 12.5nm and a lightly doped Si body of 3nm thickness. An oxide with an equivalent thickness of 1nm is chosen, The source and drain extensions are heavily doped to $N_D = 10^{20}\text{cm}^{-3}$.

The analyses were performed with the MINIMOS-NT device simulator [20]. Impact ionization is essential to the functionality of a Z-RAM cell. Electron-hole recombination is very important as antagonistic mechanism. Similar parameters for impact ionization and for recombination are used for both structures. Band-to-band tunneling was also included with a standard model [20].

III. RESULTS

The results for current calculations as function of the gate voltage for a 50nm double-gate structure are shown in Fig. 1 and Fig. 2. At high positive gate voltages the current values do not depend on the gate voltage scan direction.

For negative gate voltages the situation is completely different. In a forward scan direction for the gate voltage, the current stays low for both values of the source-drain voltage until a certain critical value is reached. This part of the $I_{DS} - V_{GS}$ corresponds to the subthreshold regime. Due to negligible DIBL in a 50nm double-gate structure, the current dependence in the subthreshold regime is similar for both values of the source-drain current.

As soon as a critical current value is reached, the source-drain current rapidly increases by several orders of magnitude. The current keeps increasing for positive gate voltage values.

In a reverse gate voltage scan, the current first slowly decreases. For positive gate voltages, the current takes exactly the same values as for the forward scan. Therefore, the $I_{DS} - V_{GS}$ curve is completely reversible for both values of the source drain voltage, as already mentioned. However, the current value does not decrease sharply for moderately negative values of gate voltages, although it keeps slightly decreasing. The current values at the reverse scan remain several orders of magnitude higher than the values for the forward scan. The relatively large current value is maintained down to V_{GS}=-2V for V_{DS}=2.0V, where it abruptly decreases by several orders of magnitude. Thereby the MOSFET

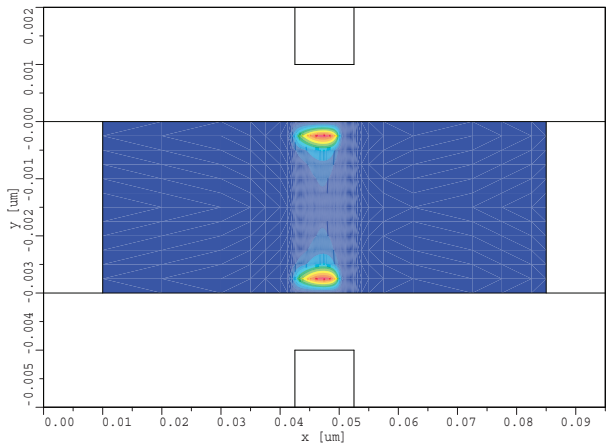

Fig. 5. Contour plot of the hole distribution in the 12.5nm long MOSFET channel for the high current state. Close to the gates the hole concentration is high. Due to quantum correction, the centroid of the hole concentration is at a certain distance from the gates.

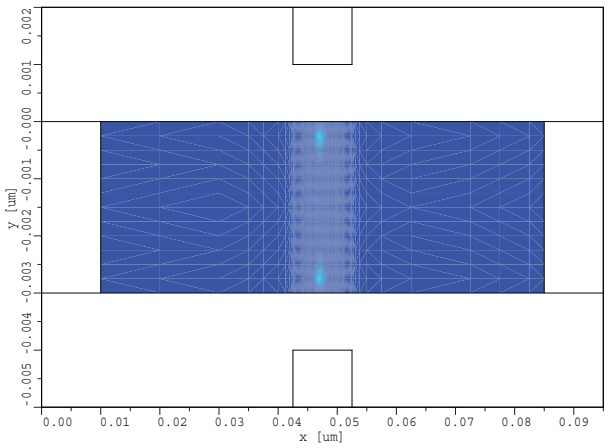

Fig. 6. Contour plot of the hole distribution in the 12.5nm long MOSFET channel for the low current state. The concentration is small. Due to quantum correction, the centroid of the hole concentration is at a certain distance from the gates.

is turned back into the subthreshold regime, completing the hysteresis loop. Indeed, the previous current value cannot be reached just by inverting the scan direction. Instead, if one increases the gate voltage, the current will follow the lower subthreshold branch, until the critical current value is reached at V_{GS}=-0.6V. The point with relatively high current at V_{GS} =-2V can only be reached by inverting the gate voltage scan after the high current value was achieved at positive gate voltages. Interestingly, if we increase the source-drain voltage to V_{DS}=2.2V, the abrupt transition to the subthreshold regime during the reverse voltage scan cannot be observed for technically relevant negative gate voltage values. A similar behavior is observed when a parasitic bipolar transistor turns on in floating body SOI structures [21], which is usually considered as undesirable.

The two different current states corresponding to the same drain and gate voltages, seen also on $I_{DS} - V_{DS}$ characteristics shown in Fig. 2 are essential for Z-RAM functionality [13]. We are now analyzing the physical reasons for these two different current states.

Fig. 3 displays the potential profile from the source to the drain electrode, cut in the middle of the silicon body, for two different current states corresponding to the same source and drain voltage. In the low current state the potential has a large barrier under the gate preventing the current flowing from the source to the drain. On the contrary, in the high current state the potential is nearly flat in the source-gate region, and the transistor is opened. Such a difference in potential profiles is due to different charge distributions in the system shown in Fig. 4. In the state with low current the electron concentration in the channel is small and the majority carrier concentration (holes) is small too (Fig. 4). In the state with high current one naturally has a higher electron concentration in the channel. More important, the hole concentration in the channel has also increased as shown in Fig. 4. The hole concentration in the channel is higher close to the gates, in agreement with [13]. Holes are generated close to the drain region due to impact ionization. The electric field in the channel close to the drain region drives generated holes in the body region, where they accumulate. This accumulated positive charge pins down the conduction band to the potential in the source and opens the transistor.

Holes recombine with electrons primarily via the Shockley-Read-Hall mechanism. Excess holes visible in Fig. 4 flow into the source region. Their extra positive charge is compensated by additional electrons, resulting in a slightly higher electron concentration than the equilibrium concentration determined by $N_D = 10^{20}\text{cm}^{-3}$.

The nature of the two current states analyzed above allows to determine conditions, where the transitions between them occur. One important ingredient is obviously impact ionization which is usually characterized by the multiplication factor $M > 1$. The positive feedback loop is activated, when the collector current is larger than the base current. Since the hole base current is proportional to $M - 1$, the positive feedback corresponds to the condition [21]

$$\beta_F(M - 1) > 1, \tag{1}$$

where β_F is the common-emitter current gain. The increase of the drain current is triggered by the positive

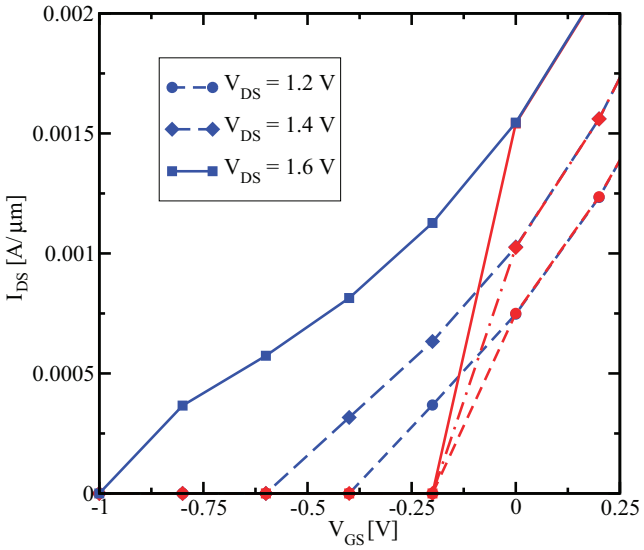

Fig. 7. $I_{DS} - V_{GS}$ for a scaled double gate MOSFET with the gate length 12.5nm and silicon body thickness 3nm, for three source-drain voltage. Hysteresis behavior is clearly observed.

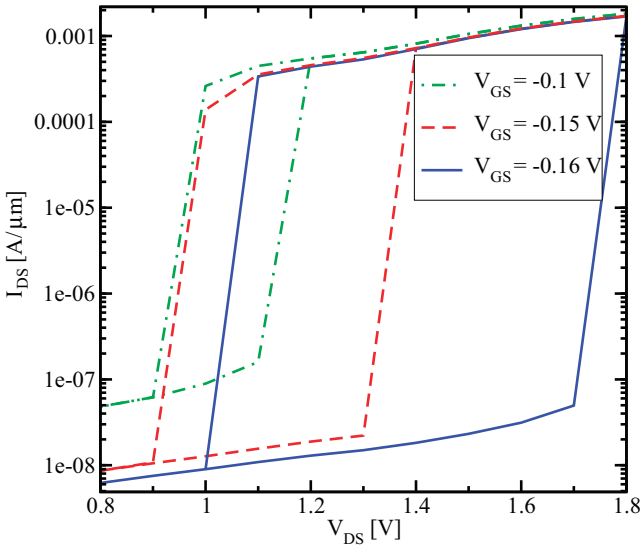

Fig. 8. $I_{DS} - V_{DS}$ in a logarithmic scale for a 12.5nm double gate MOSFET with silicon body thickness 3nm, for different gate voltages V_{GS}. Hysteresis behavior is clearly observed.

feedback, saturating when the transistor opens.

If we now reduce the gate voltage, an increasing number of holes must be stored under the gate to compensate the gate voltage decrease and keep the transistor open. This results in an increased recombination rate which reduces β_F. At large negative gate voltages the condition (1) cannot be fulfilled. The positive feedback loop breaks, which results in a sudden decrease of the current. The number of generated holes drops. Their concentration under the gate reduces and they cannot screen the gate potential. This leads to a potential barrier increase which further reduces the current. The process stops, when the transistor is closed.

The consideration above can explain the $I_{DS} - V_{GS}$ behavior at V_{DS} =2.0V for the reverse gate voltage scan. For the forward gate voltage scan the transistor stays in the closed state for higher gate voltages than for the reverse scan. The reason is the absence of current in the closed state. However, due to an exponential current increase in the subthreshold regime at a gate voltage close to zero, the current reaches a critical value after which the positive feedback loop opening the transistor activates. The critical current values only slightly depend on drain voltage, due to a dependence of β_F on drain voltage.

We have demonstrated that a programming window, which is formed by the two current values and the two gate voltage values when switching appears, is sufficiently large for stable Z-RAM operation on 50nm double-gate transistors. We now present simulations of a double-gate structure with 12.5nm gate length. Excess hole concentrations in the open and close states corresponding to the large and low values of the current are shown in Fig. 5 and Fig. 6, respectively. Due to quantum correction included in simulations, the charge centroid is shifted away from the interface. Results of $I_{DS} - V_{GS}$ calculations and hole concentrations shown in Fig. 7 and Fig. 8 clearly display a hysteretic behavior similar to that observed for a 50nm MOSFET. For all considered source-drain voltages the transition to the high current state appears at slightly negative gate voltages. For the reverse scan the transition to the low current state is observed at large negative gate voltages for V_{DS} =1.6V, while for V_{DS} =1.2V the hysteresis has nearly disappeared. For V_{DS} =1.4V, the transition to the low current state occurs at V_{GS} = -0.6V. This results in a relatively large programming window sufficient for successful Z-RAM cell operation. It is thus demonstrated that a Z-RAM cell built on a scaled double-gate MOSFET with 12.5nm gate length preserves its functionality.

IV. DISCUSSION

The $I_{DS} - V_{GS}$ behavior for a 12.5nm gate length MOSFET looks principally analogous to the behavior of a 50nm MOSFET. One difference between the results is that the current density for a thinner and shorter double-gate structure is nearly an order of magnitude smaller. However, this is not a substantial limitation, because the important criterion for Z-RAM functionality is the difference between the two values of current in the two different current states, which is still several orders of magnitude for a 12.5nm double-gate structure.

Although our simulations show that a very small Z-RAM cell is functionable, the program window was found to reduce gradually with scaling. This suggests that for more accurate predictions a more refined treatment of quantum effects beyond quantum correction

is needed. Another anticipated direction for improvement is a choice of a more accurate model for band-to-band tunneling. Although band-to-band tunneling was included within a standard model [20], a different model for band-to-band tunneling indicates a possible failures during "Read 0" operation in ultra-scaled Z-RAM cells [24].

Our simulations predict that the supply voltages are 25-30% smaller for a Z-RAM based on a scaled MOSFET. The obtained substantial decrease in supply voltage is comparable with the anticipated decrease for scaled logic devices. We should add, however, that the impact ionization model used in the simulations depends on the local field only. When the channel length is reduced, the local field in the channel at the drain end is expected to increase. Therefore, the local field impact ionization model can overestimate impact ionization. Another potential limitation of the applicability of our approach is that in scaled devices transport becomes quasi-ballistic, and the impact ionization models used in Monte Carlo simulations of hot carrier transport [22] become relevant. These models are characterized by threshold energies above which impact ionization starts, with the lowest threshold of 1.2eV. It was recently argued that due to the presence of energetic carriers in an injected distribution substantial impact ionization can be present even, when the source-drain voltage is smaller than the threshold [23]. However, because of the gap increase due to size quantization in a 3nm silicon film, we believe that 1.2eV is a fair estimate of a Z-RAM cell supply voltage, which is consistent with $V_{DS} = 1.4$V obtained in our simulations.

V. CONCLUSION

We have shown that a Z-RAM cell built on a scaled double-gate MOSFET preserves its functionality by providing a wide voltage operating window with large current differences. We also predict a decrease in the supply voltage to 1.2-1.4V, which is about 25-30% smaller than in current prototypes. Results are in agreement with recent considerations of floating body RAM scaling down to 32nm technology node based on experimental results [8].

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