Dependence of the Negative Bias Temperature Instability on the Gate Oxide Thickness

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***Abstract*—The exact location and type of defects created under negative bias temperature (NBT) stress in pMOS field effect transistors is still a highly debated topic. We present a detailed study on equivalent devices with different oxide thicknesses (5 to 30 nm) where we show experimentally that the basic mechanisms behind the NBT instability are the same in thin and thick oxide technologies. In particular, voltage driven degradation like impact ionization or anode hole injection are not the driving forces for the larger degradation of thick oxide devices. Finally, we show that defects created under NBT stress are not solely located at the interface but extend a few nanometers into the oxide.**

I. Introduction

During negative bias temperature stress (NBTS), a negative shift in the threshold voltage of pMOS devices is observed [1–5]. This shift is due to energetically widely spread defects which emerge via bond breaking and subsequent charging of donor-like defects or positively charged oxide defects. However, besides the position in energy, also the exact location and type of the defects within the gate oxide is a widely debated topic [1, 6–8] raising the question, if the physical mechanisms behind the negative bias temperature instability (NBTI) are the same when comparing thin and thick oxide technologies. In particular, thick oxide devices are often assumed to have a larger contribution of oxide defects, while NBTI degradation of thin oxide devices is sometimes mainly attributed to the creation of interface states [4, 9, 10]. This view is often physically argued by degradation mechanisms like impact ionization or anode (hot) hole injection which would increase the observed degradation of thick oxide devices. During impact ionization, carriers, which had tunneled through a part of the oxide layer or had been thermally activated, become accelerated by the electric field. They are then capable of creating electron-hole pairs in the SiO_2, which may cause fixed positively charged oxide traps [11]. In the anode hole injection model, it is assumed that electrons tunnel from the poly gate towards the silicon substrate, where they excite deep valence band electrons. These electrons leave behind (hot) holes which may penetrate back into the oxide causing oxide damage [12]. Both processes are initiated by electrons which tunnel through a part of the gate oxide barrier and then are accelerated by the electric field in the oxide or the substrate. The maximum energy of the electrons arriving from the poly gate depends highly on the voltage drop across the oxide (V_{ox}). Hence V_{ox} has to exceed the band gap of the SiO_2 insulator of $\approx 9\,\text{eV}$ before these mechanisms become efficient [13–16]. This means, when applying conventional oxide fields during NBTS $|E_{\text{ox}}| < 7\,\text{MV/cm}$, this critical voltage drop is reached as the gate oxide thickness exceeds roughly $13\,\text{nm}$.

We chose our oxide thicknesses such that identical stress fields imply voltage drops from far below to well above the band gap of the oxide. This helps to investigate whether the voltage driven degradation effects mentioned above contribute and thus completes the work of earlier studies [17]. We paid particular attention to equivalent stress and measurement conditions for the different devices, namely identical oxide fields during stress and equal Fermi level positions relative to the conduction and valence band edges during recovery. In the analysis of our measurement results we account for the different capacitances of the oxides. Considering all this, we are able to perform an exact comparison of thin and thick oxide technologies.

II. Experimental Setup

For our study we used pMOS devices with n^{++} poly gates with effective oxide thicknesses of $5.6\,\text{nm}, 13.9\,\text{nm}$ and $29.1\,\text{nm}$, calculated out of capacitance measurements in accumulation, and stressed them at the same temperature ($125°\text{C}$) and under the same negative oxide field with $|E_{\text{ox}}| < 7\,\text{MV/cm}$. The temperature was kept constant throughout the whole experiment. Note that when applying the same electric fields to different oxide thicknesses, we end up with completely different voltage drops across the oxide (V_{ox}), which are roughly half of the SiO_2 band gap for the thin oxide device and roughly twice the band gap for the thick oxide device. In order to compare NBTI induced V_{TH} shifts of different oxide thicknesses, it is important to assure the following experimental conditions:

- All devices must be stressed equivalently. It is generally assumed that the oxide field and/or the hole population at the interface are the driving forces causing NBTI degradation [8]. However, we remark that the same oxide field implies similar carrier concentrations at the interface for different oxide thicknesses.
- During recovery, the Fermi level position and the carrier concentrations at the interface must be identical as well to assure equivalent occupancy levels of the interface states and identical recovery conditions for the defects created during stress.

A. Equivalent stress conditions

To determine the relationship between the oxide field (E_{ox}) and the voltage applied to the gate (V_G), we used the method

$$E_{ox}(V_G) = \frac{\int_{V_1}^{V_G} C(V)\,\mathrm{d}V}{\varepsilon_{SiO_2}} + \text{const} \qquad (1)$$

proposed in [17]. The constant in Eq. (1) is determined by the condition that the oxide field has to be close to zero at the flat-band voltage. V_1 can be chosen arbitrarily except for the requirement $V_G < V_{FB} < V_1$ for negative stress voltages.

B. Equivalent recovery conditions

Using a drain current criterion, we estimated the correct gate voltages during recovery that guarantee a similar Fermi level position. The drain current is directly proportional to the density of inversion channel carriers and therefore also proportional to the Fermi level position at the interface. We determined the appropriate readout voltages V_R for different oxide thicknesses from virgin transfer curves to be $V_R = -0.76\,\mathrm{V}, -0.82\,\mathrm{V}$ and $-1.04\,\mathrm{V}$ for $T_{ox} = 5.6\,\mathrm{nm}, 13.9\,\mathrm{nm}$ and $29.1\,\mathrm{nm}$, respectively which is around the V_{TH} of all devices.

By using Berglund's method [18], which gives the dependency of the surface potential ψ_S on the applied gate voltage V_G, we experimentally verified that the drain current criterion actually assures similar surface potentials with an accuracy of around $60\,\mathrm{mV}$ (c.f. Fig. 1).

C. Experimental details

Fig. 2 shows the evolution of the voltages applied to the gate and to the drain during a basic measurement cycle. During stress, we applied the stress voltage V_S for $t_{str} = 10^0, 10^1, \ldots, 10^5\,\mathrm{s}$ to the gate of the device. After stressing the device, the gate voltage was switched to the appropriate readout level V_R and simultaneously the drain bias was switched from $0\,\mathrm{V}$ to $V_D = -100\,\mathrm{mV}$ for $t_{rec} = 10^0, 10^1, \ldots, 10^5\,\mathrm{s}$. The V_{TH} recovery of the device was monitored by measuring the change in the drain current and subsequent conversion to a corresponding V_{TH} shift [19]. Following constant bias recovery, the interface trap density was monitored for $t_{CP} = 10\,\mathrm{s}$ by recording the maximum charge pumping (CP) current [20, 21]. We used the same experimental CP setup for all three oxide thicknesses, namely $1\,\mathrm{MHz}$ gate pulsing frequency and a pulse amplitude of $2\,\mathrm{V}$ ranging from deep accumulation ($+0.5\,\mathrm{V}$) to deep inversion ($-1.5\,\mathrm{V}$). Since we observed a vanishing influence of V_{TH} and V_{FB} for different T_{ox} on the energy range scanned by CP [21], the dependence of the maximum CP current on the oxide thickness is negligible. By switching the gate bias between inversion and accumulation during CP, repeatedly majority electrons become attracted to the interface during the accumulation phase, favoring neutralization and annealing of positively charged oxide defects located close to the interface [8, 22]. Recent findings [23] suggest the that remaining V_{TH} shift after CP can be considered to be permanent on the timescale of an experiment. The remaining degradation was recorded for $t_{perm} = 10\,\mathrm{s}$.

The experiments described above were performed on three different devices on three different wafers having different oxide thicknesses. The devices had been carefully selected to have similar virgin maximum CP currents, which was found to guarantee similar degradation behavior [24].

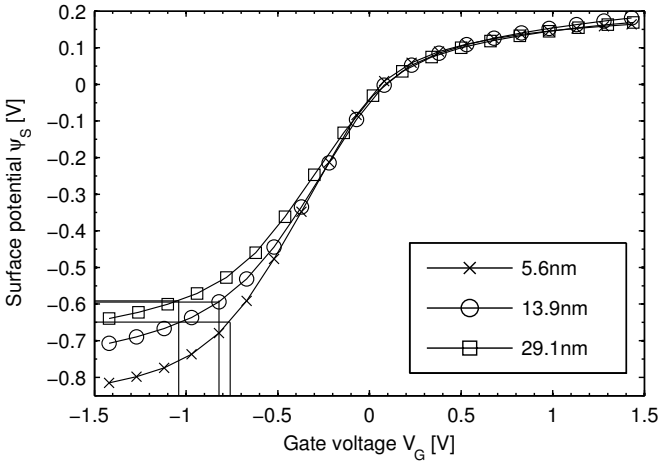

Fig. 1. Measured change of the surface potential ψ_S with the gate voltage V_G calculated according [18]. In inversion different voltages correspond to the same surface potential for different oxide thicknesses.

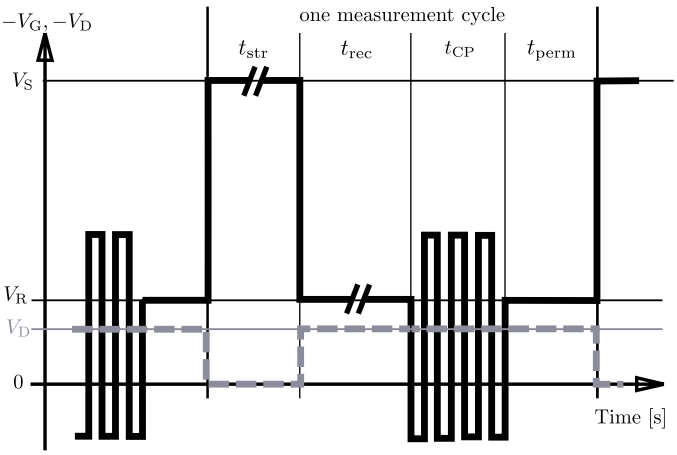

Fig. 2. Evolution of the voltage applied to the gate (V_G) and the drain (V_D) over time. During t_{str}, t_{rec} and t_{perm} a constant bias is applied to the gate and the drain contact. During t_{CP} a charge pumping measurement is performed.

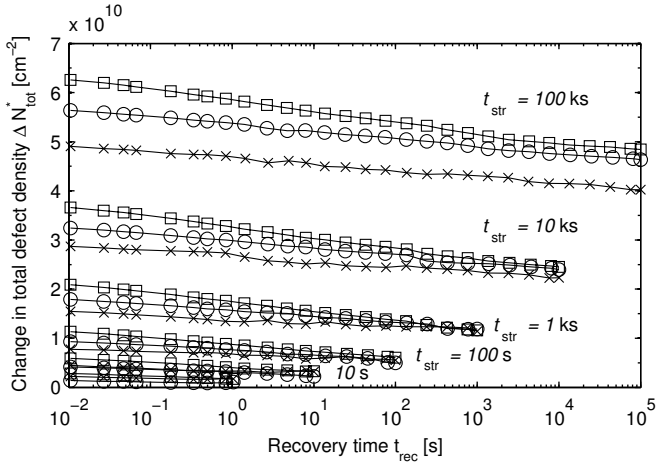

Fig. 3. The change of total effective defect charge density per area ΔN^*_{tot} over recovery time t_{rec} for six different stress times. Crosses $\times$ indicate the $5.6\,\text{nm}$, circles $\odot$ the $13.9\,\text{nm}$ and squares $\boxdot$ the $29.1\,\text{nm}$ device.

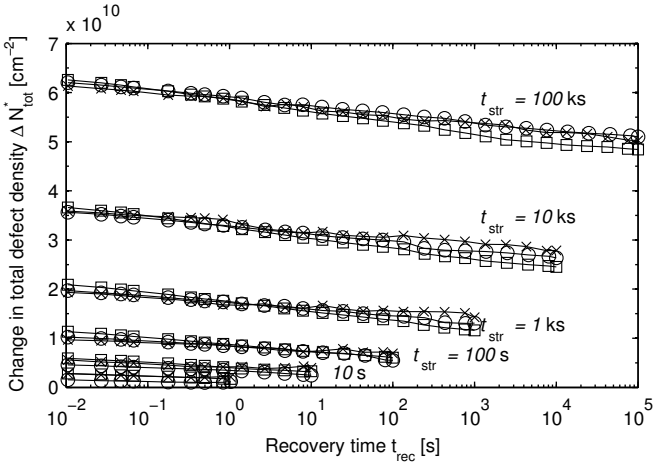

Fig. 4. Scalability holds for different oxide thicknesses. Depicted is the data of Fig. 3 multiplied with 1.25 for the $5.6\,\text{nm}$ device and 1.10 for the $13.9\,\text{nm}$ device.

III. Experimental results

As already mentioned in [17], the different oxide capacitances C_{ox} have to be taken into account when comparing the V_{TH} shifts of different oxide thicknesses. This is because a single charge q located at the silicon substrate – silicon dioxide interface causes a threshold voltage shift of $\Delta V_{\text{TH}} = q/C_{\text{ox}}$. Thus, a more general way to compare the V_{TH} shifts of devices with different capacitances is to characterize them by their change in effective defect charge density per area

$$\Delta N^*_{\text{tot, perm}} = \frac{\Delta V_{\text{TH}} C_{\text{ox}}}{q}, \tag{2}$$

with q the elementary charge, assuming that all defects are located close to the interface.

The recovery traces of the devices right after stress are illustrated in Fig. 3. Remarkably, multiplying the data of the $5.6\,\text{nm}$ device with 1.25 and the data of the $13.9\,\text{nm}$ device with 1.10 leads to a very good agreement of the recovery characteristics, as can be seen in Fig. 4. The very first data points in each trace in Fig. 3, that is to say the actual drifts 10ms after termination of stress, are plotted as a function of stress time t_{str} in Fig. 5. We remark that apart from these small scaling factors, the overall stress and recovery behavior of the devices is similar, if not equivalent.

A. Permanent degradation and interface states

In Fig. 6 the total change in defect density as well as the change in permanent defect density is illustrated as a function of the stress time. The values for ΔN^*_{tot} are taken from the data of Fig. 3 (recorded $10\,\text{ms}$ after termination of stress). The permanent degradation ΔN^*_{perm} was measured after constant bias recovery and CP. During the positive bias phase of the CP gate pulse, when majority electrons accumulate at the interface, positive bulk traps may exchange carriers with the silicon substrate by tunneling processes [6]. Once an electron is captured, the trap is neutralized and it may anneal

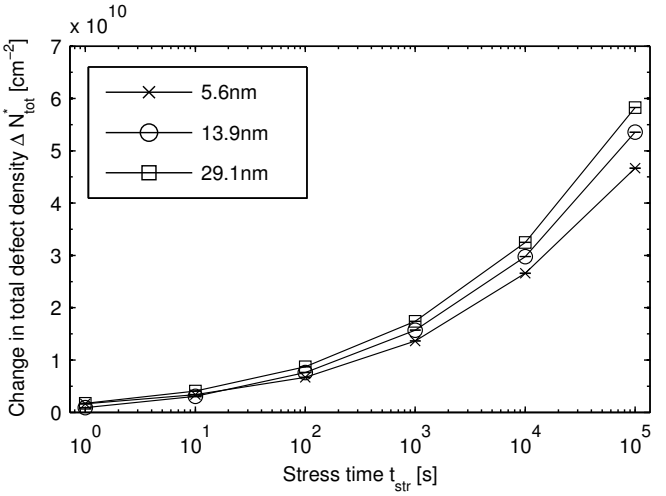

Fig. 5. The total change in effective defect charge density ΔN^*_{tot} per area $10\,\text{ms}$ after termination of stress is illustrated over the stress time t_{str}.

subsequently [2]. The remaining defects are assumed to have very long time constants compared to the time scale of our experiment. Hence the remaining shift after CP is labeled as permanent in this study. The change in the maximum CP current ΔI_{CP} is depicted in Fig. 7. Note that the increase in the maximum CP current after stress is similar for all three oxide thicknesses indicating an equivalent increase of interface traps.

Impact ionization or anode hole injection during NBTI are of vanishing probability in our thinnest oxide device ($5.6\,\text{nm}$) because of the small voltage drop across the oxide ($V_{\text{ox}} < 4\,\text{V}$) [25]. Since all analyzed larger oxide thickness devices have a similar degradation behavior we suggest that impact ionization or anode hole injection do not play a crucial role when subjecting devices to NBTS at commonly used oxide fields. In particular, this argument holds even for devices where V_{ox} may greatly exceed the band gap of the dielectric.

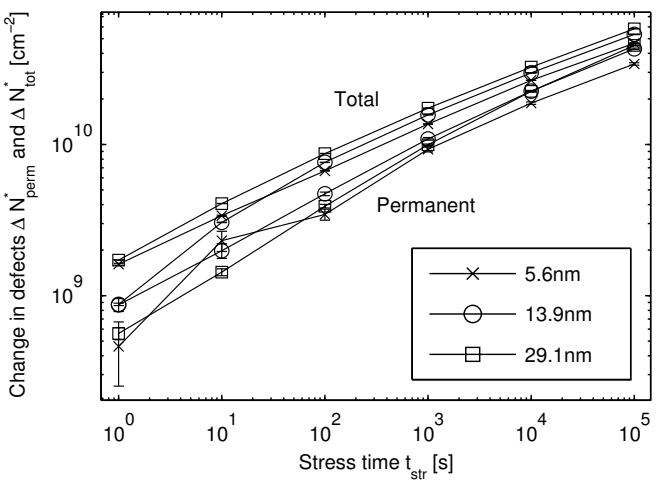

Fig. 6. The total change in effective defect charge density ΔN^*_{tot} per area $10\,\text{ms}$ after termination of stress with t_{str} seconds duration and the permanent change in effective defect charge density per area ΔN^*_{perm} is illustrated over the stress time t_{str}. The data for ΔN^*_{perm} are the average values of measurements with $t_{\text{perm}} = 10\,\text{s}$ duration. We have drawn error bars according the standard deviation of the measured ΔN^*_{perm} data.

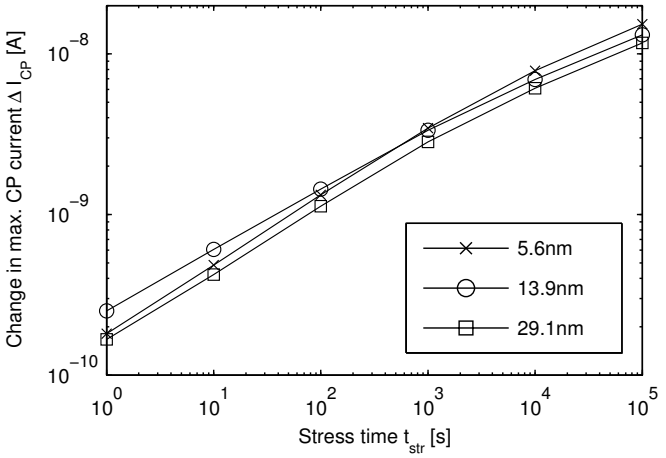

Fig. 7. Change of the maximum charge pumping current after $t_{\text{str}} = 10^0, \ldots, 10^5\,\text{s}$ of stress and $t_{\text{rec}} = 10^0, \ldots, 10^5\,\text{s}$ of recovery measured for $t_{\text{CP}} = 10\,\text{s}$. Error bars of the standard deviation of the measurement data would be smaller than the size of the symbols and are thus not depicted here.

B. Spatial defect distribution

The remaining discrepancy of the recovery traces in Fig. 3 can be fully explained by assuming that the defects are not located directly at the interface, as assumed by the capacitance scaling approach Eq. (2), but rather extend a few nanometers into the bulk of the oxide. In Fig. 8 the V_{TH} shifts of the devices $10\,\text{ms}$ after termination of stress are depicted as a function of oxide thickness. Assuming equal effective defect charge density for the different devices, the capacitance scaling approach Eq. (2) would suggest a linear correlation with an interception in the origin in Fig. 8. It is clearly shown that the capacitance scaling approach is not sufficient to fully explain the observed behavior and consequently defects at the interface alone cannot be made responsible for the observed degradation.

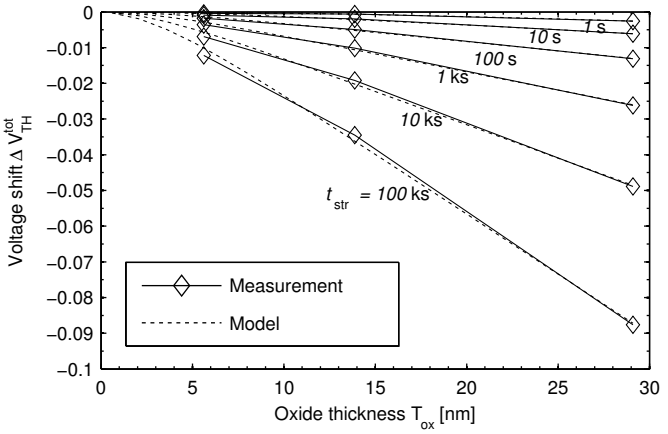

Fig. 8. Threshold voltage shifts $10\,\text{ms}$ after termination of stress over oxide thickness. The six different lines indicate six different stress times $t_{\text{str}} = 10^0, \ldots, 10^5\,\text{s}$. The dotted lines show the ideal relationship assuming the exponential defect density distribution Eq. (4).

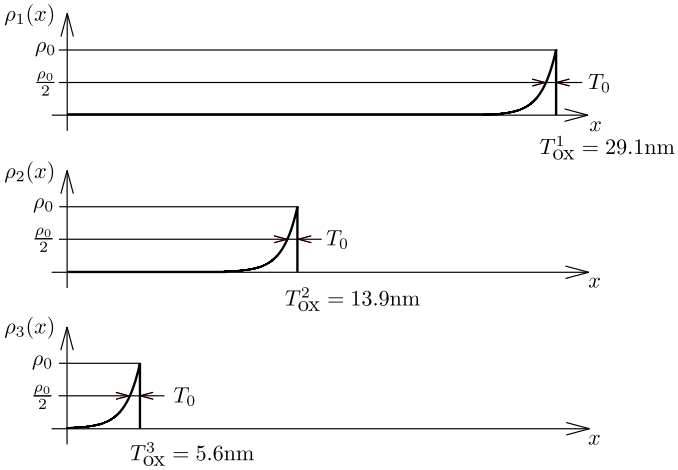

Fig. 9. Spatial defect density distributions for different oxide thicknesses $T^1_{\text{ox}}, T^2_{\text{ox}}, T^3_{\text{ox}}$ under the assumption that equivalent NBTS causes equivalent defect density distribution.

A spatial defect distribution $\rho(x)$, with x being the distance from the poly gate – oxide interface towards the semiconductor, causes a shift in the threshold voltage according to Gauss's law of

$$\Delta V_{\text{TH}} = -\frac{1}{C_{\text{ox}}}\left(\frac{1}{T_{\text{ox}}}\int_0^{T_{\text{ox}}} x\rho(x)\mathrm{d}x\right). \tag{3}$$

Assuming that equivalent NBTS causes equivalent spatial defect distributions for the different oxide thicknesses (c.f. Fig. 9), we may draw conclusions on the spatial defect distribution within the bulk of the oxide. We observe strikingly good fits (c.f. Fig. 8) using the distribution

$$\rho(x) = \rho_0 \exp\left(\frac{x - T_{\text{ox}}}{T_0/\ln(2)}\right), \tag{4}$$

with a half-value defect depth T_0 and a maximum charge density per volume ρ_0. Our data fitting results give an average value of T_0 of roughly $2\,\mathrm{nm}$, slightly decreasing with increasing stress time t_{str}. However, we remark that our study might be insufficient to make unambiguous statements on the exact distribution of defects in the bulk of the oxide because our data are limited to only three different oxide thicknesses. Nevertheless, it is clearly demonstrated that interface states alone can not be made responsible for all of the NBTS induced V_{TH} shift. We speculate that this statement holds for arbitrary oxide thicknesses, at least in the 5 to $30\,\mathrm{nm}$ range.

IV. Conclusions

By monitoring NBTI degradation on equivalent devices with different gate oxide thicknesses ranging from $5.6\,\mathrm{nm}$ to $29.1\,\mathrm{nm}$, we draw three main conclusions on the influence of the oxide thickness:

- Oxide bulk degradation originating from impact ionization or anode hole injection, which depends highly on the voltage drop across the oxide V_{ox}, do not play a crucial role in NBTI degradation.
- The increase of the charge pumping current is similar for all tested oxide thicknesses. Thus comparable stress induces a comparable number of broken silicon-hydrogen bonds at the interface, independent of the oxide thickness.
- The total number of NBTI induced defects is the same within a 15% range assuming all defects at the interface. This discrepancy vanishes if we assume the defects to extend a few nanometers into the bulk of the oxide.

Consequently, it has to be concluded that the physical mechanisms leading to NBTI are the same for thin and thick oxide devices. Future studies should involve a larger number of oxide thicknesses. This would help to derive more precise information about the particular distribution of oxide defects in the bulk of the oxide.

Acknowledgment

This work was jointly funded by the Federal Ministry of Economics and Labor of the Republic of Austria (contract 98.362/0112-C1/10/2005) and the Carinthian Economic Promotion Fund (KWF) (contract 98.362/0112-C1/10/2005).

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