6Å EOT $Si_{0.45}Ge_{0.55}$ pMOSFET with Optimized Reliability (V_{DD}=1V): Meeting the NBTI Lifetime Target at Ultra-Thin EOT

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Abstract

6Å EOT $Si_{0.45}Ge_{0.55}$ pFETs with 10 year lifetime at operating conditions (V_{DD}=1V) are demonstrated. Ultra-thin EOT is achieved by interfacial layer (IL) scavenging. Negative Bias Temperature Instability (NBTI) is alleviated using a high Ge fraction, a thick SiGe quantum well (QW) and a thin Si cap. Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB) are shown also to not constitute a showstopper for optimized SiGe devices.

Introduction

Negative Bias Temperature Instability (NBTI) is considered a major reliability issue for scaled CMOS technologies (1). Constant voltage scaling enhances NBTI due to the increased oxide electric field (E_{ox}). As a consequence, for ultra-thin EOT (<1nm) Si pFETs, a 10 year lifetime cannot be guaranteed for the expected operating V_{DD}=1V ($|V_G-V_{th}|$=0.7V for a $|V_{th}|$=0.3V, as per (2)), as shown for the ref. data (*Si channel*) in Fig. 2-5 (3). We have recently shown that high-mobility Ge (4) and especially SiGe pFETs with buried channel architecture can improve the NBTI reliability (5,6). In particular, high Ge fractions, thicker SiGe quantum wells (QW) and thinner Si caps were shown to boost the device lifetime under NBTI stress conditions. However, this has been shown only for SiGe devices with EOT>1nm. In this paper, a 6Å EOT $Si_{0.45}Ge_{0.55}$ pFET with 10 year lifetime at operating conditions (V_{DD}=1V) is demonstrated.

Experimental

The gate-stack of the buried SiGe channel p-FET is depicted in Fig. 1 (7-8). Different Ge fractions, QW and Si cap thicknesses were used (as noted in the figures). Three different metal gates (M^A, M^B, and M^C with thicknesses M^A>M^B>M^C) were used for EOT reduction by interfacial layer (IL) scavenging (9,10). The capacitance equivalent thickness is always reported in inversion (T_{inv} at V_{th}-0.6V ≈ EOT+4Å due to the known T_{inv} penalty (7)). The NBTI failure criterion is defined as 30mV threshold voltage shift (ΔV_{th}) at 125°C. The extended Measure-Stress-Measure (eMSM) technique with t_{relax}=2ms was used to account for the relaxation of the ΔV_{th} (11).

Results

As we have recently shown (5-6), the Si cap has a considerable impact on the NBTI reliability with thinner caps enhancing device lifetime. As shown in Fig. 2, the same trend is observed for sub-1nm EOT devices. Fig. 3 shows that EOT reduction by IL scavenging degrades the NBTI reliability faster than high-k scaling. A similar trend is observed for Si channel devices in Fig. 4. In particular, as one can see in Fig. 3b, there is an additional reliability deterioration on top of that caused by the electric field increase due to EOT scaling (maximum operating E_{ox} vs. T_{inv} would stay constant as observed for thick EOT Si devices). The additional degradation reduces the operating E_{ox} at the same slope as for ultra-thin EOT Si channel devices that implement IL scavenging. A possible explanation for the observed trend is that a thinner SiO_2 interfacial layer can enhance the hole tunneling probability toward the traps in the dielectric, which is one of the causes of NBTI. Nevertheless, IL scavenging is preferred to high-k scaling to control the gate leakage. As shown in Fig. 5, gate-stack optimization can salvage the degraded NBTI reliability observed for the most aggressive IL scavenging (M^C). The high Ge fraction combined with a thicker QW and a thinner Si cap, boost NBTI lifetime to meet the target condition ($|V_G-V_{th}|$=0.7V at T_{inv}=10Å, EOT~6Å). Other CMOS degradation mechanisms, including Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB) also do not constitute a showstopper for our optimized SiGe device (Fig. 6). Such device shows also superior performance to Si ref., as discussed elsewhere (8).

Discussion

As shown, the most beneficial impact on the NBTI reliability is related to the use of a thin Si cap. Improvements related to the higher Ge fraction and thicker QW were already discussed in (6), while the decisive impact of the Si cap

remained controversial. One hypothesis proposed there (6) was that the higher initial interface trap density (N_{it}) observed for a thin Si cap could cause slower creation of new traps (ΔN_{it}) during NBTI stress. On the contrary, Fig. 7 shows that ΔN_{it} during NBTI stress at fixed conditions follows a power law on the stress time with the same exponent (~0.25) for different Si caps. Fig. 8 shows the measured total ΔV_{th}, which can be split in the so-called Permanent (P) ΔV_{th} caused by ΔN_{it} and the Recoverable (R) ΔV_{th} (11-13) caused by filling of pre-existing oxide traps (N_{ot}). The use of a thin Si cap is shown to reduce both R and P, with the R reduction being of higher importance on the total ΔV_{th} (~95% of the total shift).

A. Permanent component

N_{it} creation during NBTI stress is commonly attributed to de-passivation of H-passivated Si dangling bonds (P_{b0}) at the Si/SiO_2 interface. Electron spin resonance spectroscopy (ESR) measurement (14) performed on a Ge substrate with a thick Si cap revealed a high P_{b0} density (~$1x10^{12}$ cm^{-2}) while it could not detect these defects (<10^{11} cm^{-2}) for a very thin Si cap (Fig. 9). This suggests that the higher Ge segregation at the Si/SiO_2 interface reported for thin Si caps (15,16), can reduce the NBTI precursor N_{it} defect density and therefore reduce ΔN_{it} during NBTI stress.

B. Recoverable component

Recent works suggest that the same oxide defects are responsible for both the NBTI R-component and low frequency (1/f) noise (17,18). In agreement with this, SiGe devices with a thin Si cap also show reduced 1/f noise (Fig. 10). This trend was observed in (19-21) and can be explained as shown in Fig. 11: the noise reduction is related to a misalignment of the Fermi level E_F in the SiGe QW w.r.t. to the valence band edge of the Si cap at the oxide interface E_{VS}. Higher misalignment causes carriers to interact with a reduced density of oxide traps N_{ot} (assuming a typical "U-shaped" arbitrary distribution of defects across the Si bandgap (22)). MEDICI simulations of the band diagrams were done to calculate E_F-E_{VS} as a function of the gate overdrive, shown in Fig. 11b for two Si cap thicknesses. The observed reduction in the interaction with N_{ot} for the typical noise measurement voltage range is enhanced for typical NBTI stress conditions, explaining the observed NBTI reduction even when assuming a higher N_{ot} average density for thin Si caps as observed in (23). This model can also explain the distinct relation between the initial V_{th0} and ΔV_{th} during stress observed in our SiGe devices (Fig. 12).

Conclusions

A 6Å EOT $Si_{0.45}Ge_{0.55}$ pFET with 10 year lifetime at operating conditions was demonstrated for the first time. Gate-stack optimization with high Ge fraction, thick QW and thin Si cap alleviated NBTI for ultra-thin EOT device implementing IL scavenging. A thin Si cap has a beneficial impact on both the R and P component of NBTI.

Acknowledgments

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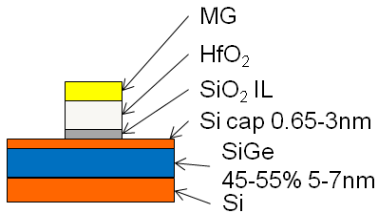


Fig. 1: Gate-stack sketch of the SiGe device.

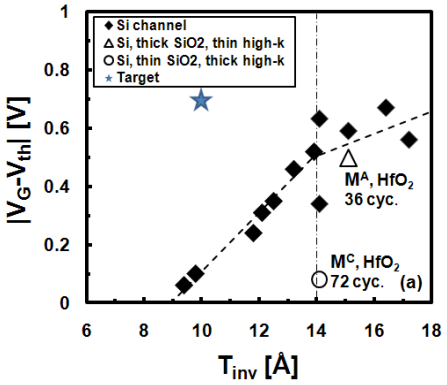
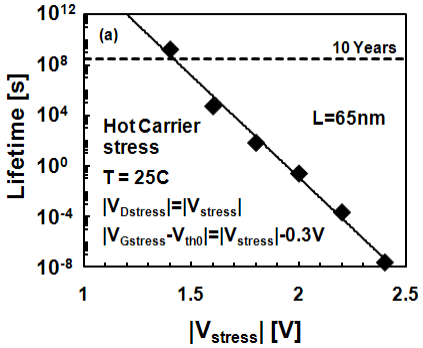


Fig. 4: Similar T_{inv} was obtained on a Si ref. device with thin HfO_2 + weak scavenging (M^A) and with thick HfO_2 + aggressive scavenging (M^C). IL scavenging is shown to reduce NBTI reliability remarkably more than high-k scaling.



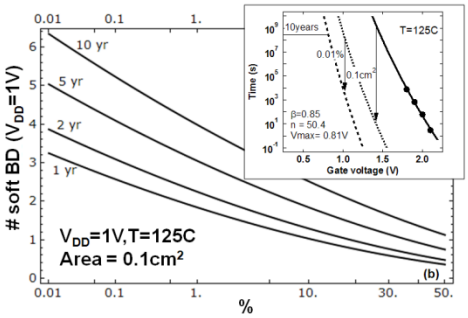


Fig. 6: Hot Carrier Injection (a) and Time Dependent Dielectric Breakdown (b) do not constitute a showstopper for our optimized SiGe device. In particular, < 6 soft breakdowns per chip (Area=0.1cm^2) can be expected during application lifetime at V_{DD}=1V (inset documents extrapolation of TDDB data).

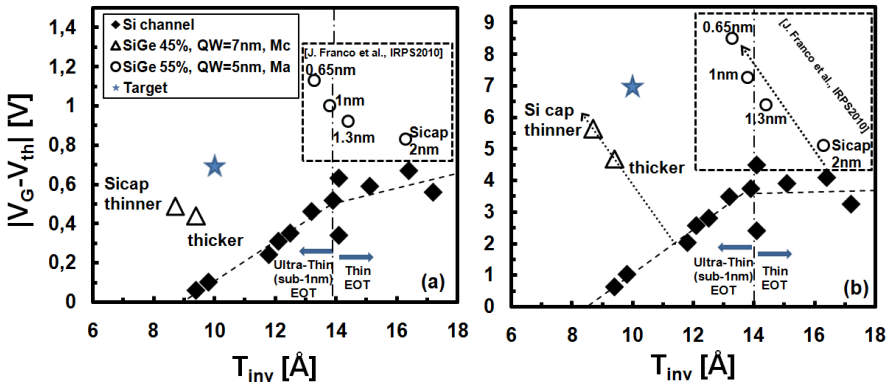


Fig. 2: (a) Maximum operating gate overdrive for 10 year lifetime under NBTI stress (T=125C, failure criterion ΔV_{th}=30mV) vs. T_{inv} (at V_{th}-0.6V). SiGe devices with a thin Si cap offer improved NBTI reliability, i.e. higher maximum operating gate overdrive. (b) Same data as in (a) but with gate overdrive converted to maximum operating equivalent oxide electric field ($E_{ox}\approx|V_G-V_{th}|/T_{inv}$). With NBTI being a field accelerated mechanism, EOT scaling is expected to reduce the operating voltage, while E_{ox} should stay constant (as observed for thick EOT on Si ref.). In contrast to that, ultra-thin EOT Si devices show reduced maximum operating E_{ox}. SiGe devices with a thin Si cap can improve NBTI reliability and therefore increase maximum operating E_{ox} even at ultra-thin EOT.

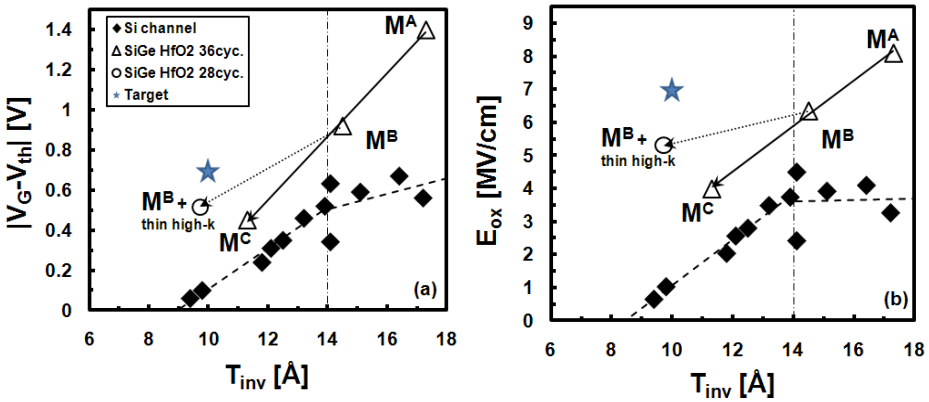


Fig. 3: (a) T_{inv} reduction by IL scavenging degrades the NBTI reliability faster than high-k scaling. (b) Converting operating gate overdrive to maximum operating E_{ox} shows that IL scavenging reduces SiGe maximum operating E_{ox} with the same slope observed for ultra-thin EOT Si devices implementing similar IL scavenging techniques.

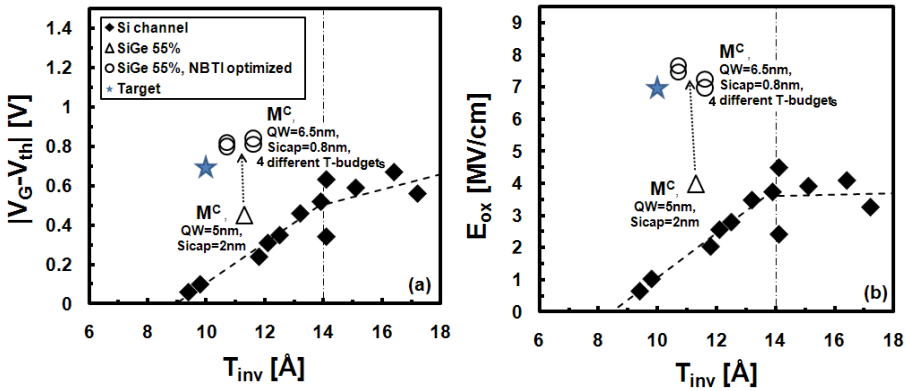


Fig. 5: A high Ge fraction (55%) and thick SiGe QW (6.5nm) combined with the use of a thin Si cap (0.8nm) boost NBTI lifetime to meet the target condition ($|V_G-V_{th}|$=0.7V at T_{inv}=10Å, EOT~6Å) on devices implementing aggressive IL scavenging (M^C).

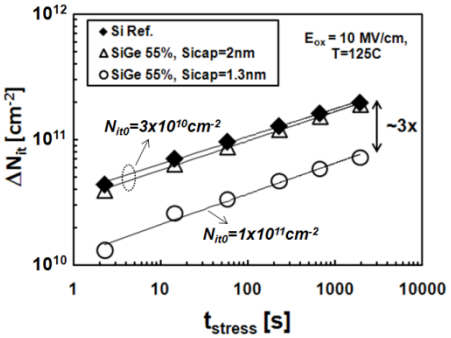


Fig. 7: ΔN_{it} measured with charge pumping during NBTI stress at fixed stress conditions on a Si Ref. and on SiGe devices with a thick (2nm) and a thinner (1.3nm) Si cap. ΔN_{it} follows a power law on the stress time with the same exponent (~0.25) on all three samples.

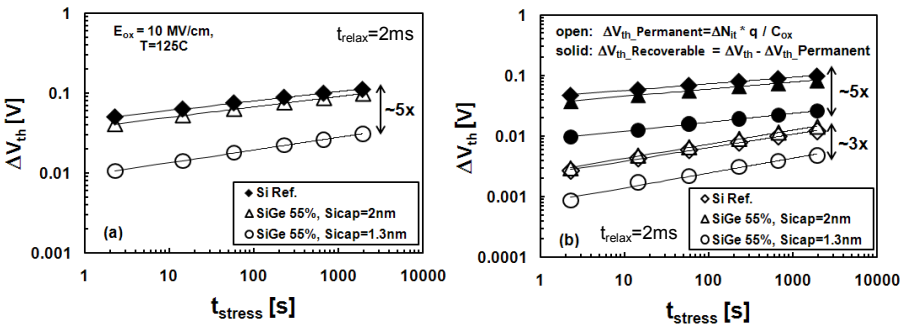


Fig. 8: (a) Measured ΔV_{th} during NBTI stress at fixed stress conditions on a Si Ref. and on SiGe devices with a thick (2nm) and a thinner (1.3nm) Si cap. The SiGe device with a thin Si cap show remarkably reduced V_{th} instability. (b) Total ΔV_{th} can be split in a permanent (P) ΔV_{th}, assumed to be caused by ΔN_{it}, and a recoverable (R) ΔV_{th}, assumed to be caused by filling of pre-existing oxide traps (N_{ot}). The use of a thin Si cap is shown to reduce both R and P, with the reduction of R being of higher impact on the total ΔV_{th} (R contributes to ~95% of the total shift).

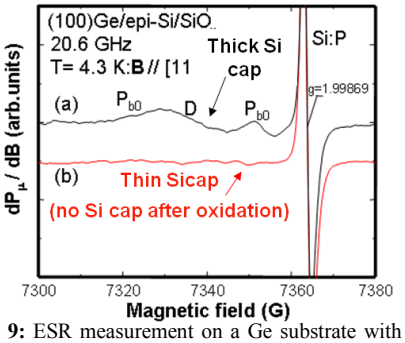


Fig. 9: ESR measurement on a Ge substrate with a thick Si cap top revealed a high P_{b0} density (~1x 10^{12} cm^{-2}) while these defects could not be detected (<10^{11} cm^{-2}) for a very thin and almost completely oxidized Si cap.

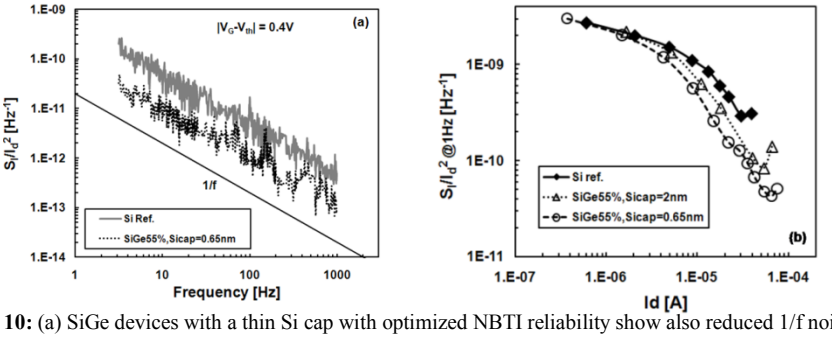
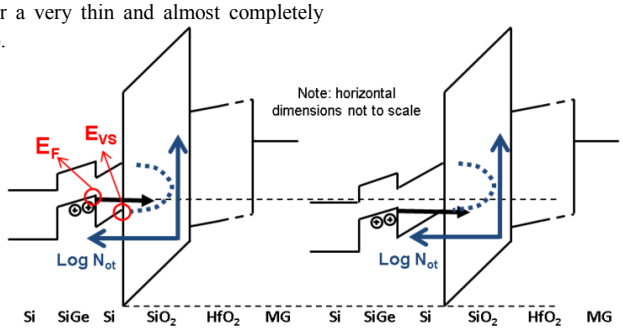


Fig. 10: (a) SiGe devices with a thin Si cap with optimized NBTI reliability show also reduced 1/f noise w.r.t. a Si ref. device with similar gate-stack, (b) and also w.r.t. a SiGe device with thicker Si cap.



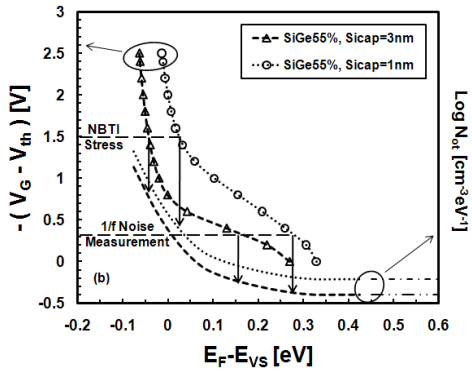


Fig. 11: (a) The noise reduction observed in a buried channel SiGe device with thin Si caps is related to the misalignment of the Fermi level E_F in the SiGe QW w.r.t. to the valence band edge of the Si cap at the oxide interface E_{VS}. Higher misalignment causes the carriers to interact with a reduced density of oxide traps N_{ot} (assuming a typical "U-shaped" distribution of defects across the Si energy bandgap, dashed line). (b) E_F-E_{VS} as a function of the gate overdrive calculated by simulating the band diagrams of our SiGe devices with different Si cap thickness in MEDICI. The observed reduction in the interaction with N_{ot} for the typical noise measurement voltage range is enhanced for typical NBTI stress conditions, explaining the observed NBTI reduction even when assuming a higher N_{ot} average density for the thinnest Si cap (dashed vs. dotted "U-shaped" arbitrary defect distributions) as observed in previous works at the SiO_2/high-k interface (23).

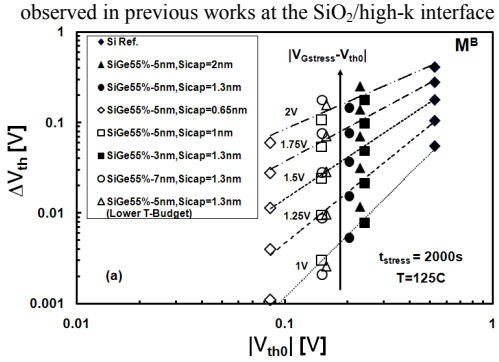


Fig. 12: (a, left) A clear correlation between the initial V_{th0} and ΔV_{th} during NBTI stress was consistently observed on our SiGe devices with different gate-stacks: devices with lower initial V_{th0} always showed reduced V_{th} instability, at any given stress condition ($|V_{Gstress} - V_{th0}|$). (b, right) This remarkable trend can be explained with the model proposed in Fig. 11.