Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs

J. Franco[1], B. Kaczer, M. Toledano-Luque, Ph. J. Roussel, J. Mitard, L.-Å. Ragnarsson, L. Witters, T. Chiarella, M. Togo, N. Horiguchi, G. Groeseneken[1]
imec
Leuven, Belgium
Phone: +32 16 28 10 85, e-mail: Jacopo.Franco@imec.be
[1]also at ESAT, K.U. Leuven, Belgium

M. F. Bukhori
Universiti Kebangsaan
Malaysia

T. Grasser
Institute for Microelectronics, T.U. Wien
Wien, Austria

A. Asenov
University of Glasgow
also with Gold Standard Simulations, Ltd.
Glasgow, United Kingdom

***Abstract*—We report extensive statistical NBTI reliability measurements of nanoscaled FETs of different technologies, based on which we propose a 1/*area* scaling rule for the statistical impact of individual charged gate oxide defects on the electrical characteristic of deeply scaled transistors. Among the considered technologies, nanoscaled SiGe channel devices show smallest time-dependent variability. Furthermore, we report comprehensive measurements of the impact of individual trapped charges on the entire FET I_D-V_G characteristic. Comparing with 3D atomistic device simulations, we identify several characteristic behaviors depending on the interplay between the location of the oxide defect and the underlying random dopant distribution.**

Keywords: finFET, Nanoscale, Negative Bias Temperature Instability, pMOSFETs, SiGe, Time-Dependent Variability.

I. INTRODUCTION

Due to the aggressive transistor scaling, the number of dopant atoms, as well as the number of defects, in each device is being reduced to numerable levels [1]. This results in increased time-zero (i.e., as-fabricated) variability, but also considerable time-dependent variability (i.e., reduced NBTI reliability) [2]. This trend has recently lead to a shift in our perception of reliability: the "top-down" approach (deducing the microscopic mechanisms of *average* NBTI degradation in large devices) is being replaced in deeply-scaled devices by the "bottom-up" approach, in which *the time-dependent variability* (i.e. nanoscaled NBTI reliability) *is understood in terms of charging and discharging of individual defects* [3].

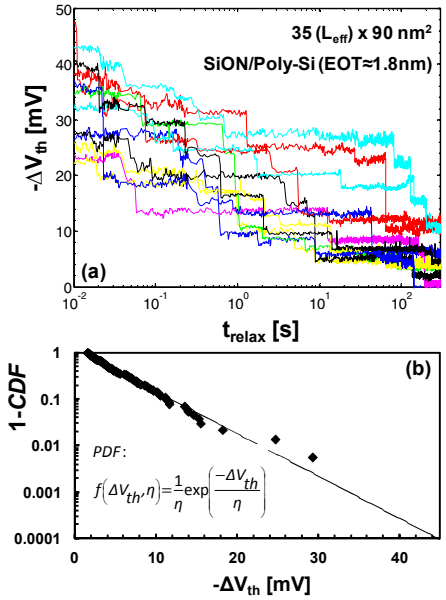

Figure 1. (a) Typical NBTI relaxation transients recorded on nanoscaled pFETs (W=90nm, L_{eff}=35nm, SiON/Poly-Si, EOT≈1.8nm). Each step corresponds to a *single* gate oxide defect discharge event. Each device presents a different number of active defects and the total ΔV_{th} observed after the same NBTI stress strongly varies from device to device. (b) The ΔV_{th} step heights corresponding to the individual discharge events observed in the relaxation transients plotted on a complementary cumulative distribution function (1-*CDF*) plot. The ΔV_{th} step heights appear exponentially distributed with an average step height η.

We and others have recently shown that the properties of individual charged gate oxide defects can be observed and measured [4,5]. Several groups have already foreseen an entire simulation flow based on this "atomistic" approach [6-8]. In particular, such circuit simulations will require understanding of i) the rules describing the impact of individual trapped charges on devices of varying dimensions (scaling rules) and ii) the impact of individual trapped charges on the entire FET current characteristics (compact models). On top of this, it is also necessary to assess the impact of individual trapped charges on the device characteristics for each of the different technologies which are currently being considered for the next CMOS scaling nodes (e.g., Si finFETs, SiGe channels).

In this paper we demonstrate the measurements of the impact of *individual charged defect*s on nm-scaled Si pFinFETs of *varying* dimensions and we show that *the average impact of scaling follows 1/area (A)*. Furthermore, we report NBTI *data* recorded on nanoscaled devices *from several technologies* (planar: Si high-k/Metal Gate, Si undoped channel, SiGe channel; Si finFETs) showing that the use of a SiGe channel offers a significant reliability improvement, which can relax the lifetime distribution prediction. Finally, the measurement of the entire I_D-V_G characteristic of planar pMOSFETs *before and after the capture of a single hole* is demonstrated. Both increases and decreases of *apparent* mobility are observed and are matched well by atomistic device simulations.

II. Experimental

NBTI-like measurements were used in order to assess the impact of individual charged gate oxide defects on the characteristics of nanoscaled devices [9]. A typical set of NBTI relaxation transients recorded on nanoscaled pFETs is shown in Fig. 1a. As one can see, the total ΔV_{th} observed after the same NBTI stress strongly varies from device to device. Individual gate oxide defect discharge events are clearly visible in the relaxation traces, with ΔV_{th} step heights which appear to be exponentially distributed ($f(\Delta V_{th},\eta)=\exp(-\Delta V_{th}/\eta)/\eta$, Fig. 1b), with an average ΔV_{th} step height η. It is worth noting that the step heights and the trap emission times were observed to be uncorrelated (not shown) [9].

In order to estimate η, the same NBTI sequence including a stress and a relaxation phases was repeated on a large set of nominally identical devices (large enough to capture the signatures of some 100 active defects, i.e. typically a few tens of devices). The relaxation transients were measured at a sense gate voltage (V_{Gsense}) equal to the threshold voltage of the fresh device (V_{th0}). The experimental temperature was 25ºC.

The ΔV_{th} steps observed in the relaxation traces were then plotted in a Complementary Cumulative Distribution Function ('1-*CDF*', see Fig. 1b) plot, and a Maximum Likelihood fit was performed in order to extract the exponential distribution parameter η and the average number of active traps per device N_T (i.e., the average number of observed ΔV_{th} steps).

The methodology described above was used on Si high-k/MG (CET≈1.7nm) pFinFETs [12] of varying dimensions for the results presented in Section IIIA. In Section IIIB, the same methodology was used on planar high-k/MG Si devices with undoped channel and on planar SiGe channel pFETs (with varying Si cap thicknesses and SiO_2 interfacial layer thicknesses) [13,14]. Finally, the devices used for the single trapped charge I_D-V_G experiment presented in Section IIIC were planar SiON/PolySi pMOSFETs (EOT≈1.8nm).

III. Results and Discussion

The geometry dependence of η is discussed in Section A. Section B discusses the technology dependence of η and N_T. Finally, the V_G dependence of the single trap ΔV_{th} is discussed in section C, demonstrating the measurement of the entire I_D-V_G of nanoscaled FETs before and after the capture of an elementary charge.

A. Single Trap ΔV_{th} : geometry dependence

The average step height (η), i.e., *the average impact of a single defect on the FET behavior*, is expected to increase when scaling the device dimensions. However, different scaling rules have been suggested in literature [1,10-11]. To test this experimentally, we collected an extensive dataset of NBTI relaxation transients on high-k/MG bulk Si pFinFETs [12] with different W and L. The results shown in Fig. 2 suggest η scaling proportionally to A^{-1}, with A the effective area of the finFET.

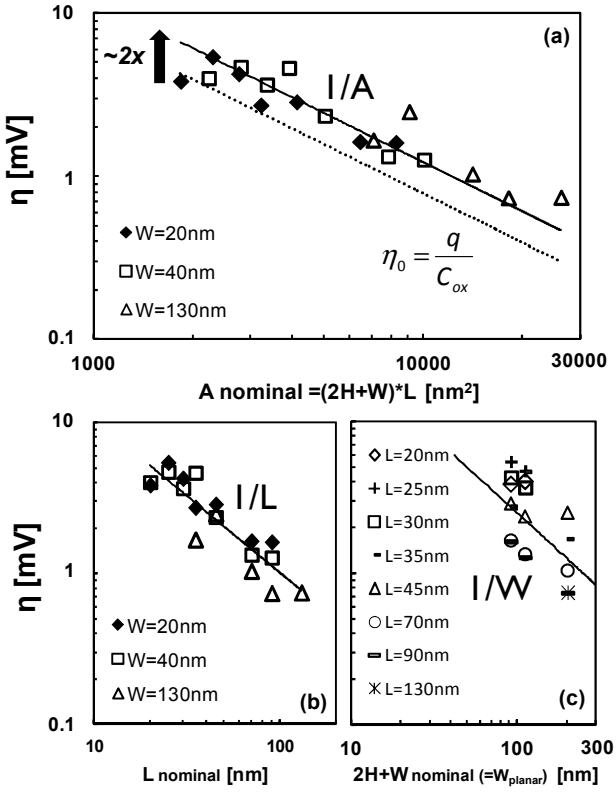

Figure 2. The average step height η is shown to scale inversely with A ($\eta \propto A^{-1}$) on Si pFinFETs (high-k/MG, CET≈1.7nm) with varying W and L. Each point is extracted as shown in Fig. 1 from a set of multiple devices with identical dimensions. Over the whole range of considered $A=L*(W+2H)$, η is 2x higher than the expected single charge ΔV_{th} as calculated with a simple charge sheet approximation ($\eta_0=q/C_{ox}$). (b) Same data plotted vs. $L_{nominal}$ ($\eta \propto L^{-1}$), and (c) vs. W ($\eta \propto W^{-1}$).

This experimentally observed dependence proves to be significantly more severe with respect to (e.g.) the $W^{-1}L^{-1/2}$ proportionality previously reported for RTN amplitude in flash memory cells [10].We speculate the severe *1/area* scaling is related to the improved channel control of the finFET device, maximizing the channel area sensitive to the full impact of individual traps [11]. Note also that over the whole range of considered A, η is 2x higher than the expected single charge ΔV_{th} as calculated with the simple charge sheet approximation $\eta_0=q/C_{ox}$.

B. Single Trap ΔV_{th} : technology dependence

Fig. 3 reports a comparison between different CMOS technologies. SiGe channel planar pFETs show a strongly reduced (<1/10x) average number of active defects (N_T) contributing to the total NBTI V_{th}-shift (Fig. 3a) w.r.t. their Si counterparts. We have previously ascribed such reduction to a favorable alignment of the Fermi level in the small-bandgap SiGe channel w.r.t. the oxide defects, as discussed in [13,14]. However, the reduced N_T, while complicating the experimental estimation of η (i.e., larger sample sets are required for a sufficiently sound statistics), does not significantly improve a real circuit (i.e., including billions of devices) lifetime, as we have shown in [15]. Interestingly, undoped SiGe pFETs also show *significantly reduced* η [14] when compared to Si devices with doped or undoped channel (Fig. 3b). A fairer comparison is obtained when normalizing the measured η values by the calculated η_0 for a given technology (Fig. 3c), in order to account for the different CET of different technologies. However, as one can see the optimized SiGe devices still show a significant η/η_0 reduction (<1/2x).

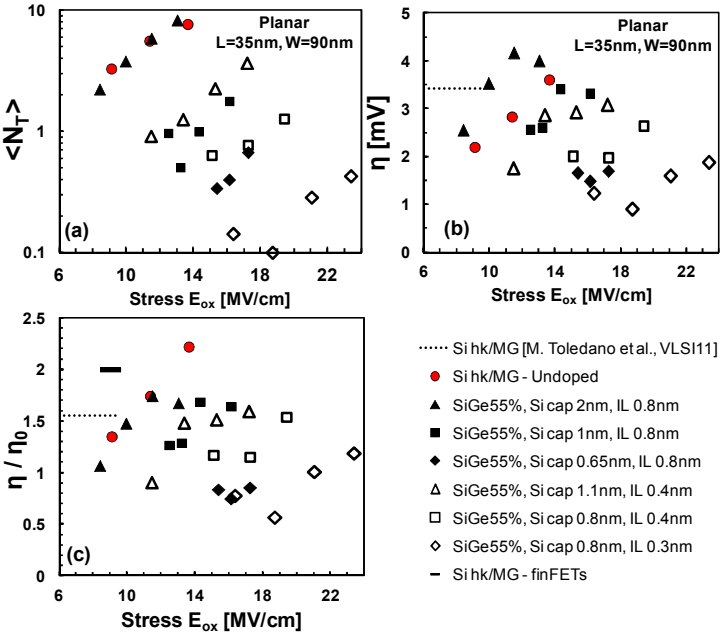

Figure 3. Technology comparison from the perspective of the impact of individual trapped charge. (a) The observed average number of active defects (N_T) is strongly reduced for optimized undoped SiGe channel pFETs with a reduced Si cap thickness even w.r.t. undoped Si ref. (b) The same SiGe devices also show reduced η values. For a fair comparison, (c) the η values are normalized w.r.t. η_0, to account for the different C_{ox} between devices of different technologies. SiGe devices still show the best η/η_0 values.

Although the η reduction offered by the SiGe channel technology converts to a strong improvement of the entire lifetime distribution of a realistic device population at the current technology node [15], the severe *1/area* η-scaling we observed in Section IIIA could jeopardize the reliability of further scaled technology nodes. In order to refine the reliability prediction for realistic populations of deeply scaled devices, it is hence of utmost importance to carefully understand the impact of a single charge on the FET current characteristics at operating conditions, as shown next.

C. Single Trap ΔV_{th} : V_G dependence

A set of 315 planar Si (SiON/Poly-Si, EOT≈1.8nm) pFETs, with L_{eff}=35nm and W=90nm, manifesting in total some 1200 active defects, was screened in order to select a smaller set of 30 devices complying with the following criteria:

(1) the device shows a single dominant active trap;

(2) the single trap ΔV_{th} is large [note that some gigantic responses up to ~45mV (probability of ~10^{-4}, cf. Fig. 1b) are found];

(3) the characteristic trap emission time is large enough (>1s) to allow a full I_D-V_G measurement sweep before the hole is emitted.

It is worth emphasizing that these criteria are solely chosen for the reason of experimental resolution. Fig. 4 shows the typical relaxation transients recorded on one such device.

The entire I_D-V_G characteristics measured on this device with and without the trapped charge are shown in Fig. 5: the shift can be characterized as ΔV_{th} (horizontal shift, Fig. 5c) or ΔI_D (vertical shift, Fig. 5d). As one can see, this particular trap causes a ΔV_{th} that depends on the applied gate voltage [$\Delta V_{th}(V_G)$], with the maximum impact at V_G slightly above the threshold voltage of the fresh device (V_{th0}).

However, every nanoscaled device is expected to behave differently due to different configurations of the dopants in the channel and of the oxide defects. This is experimentally confirmed in Fig. 6 where $\Delta V_{th}(V_G)$ measurements on all the 30 selected devices are shown.

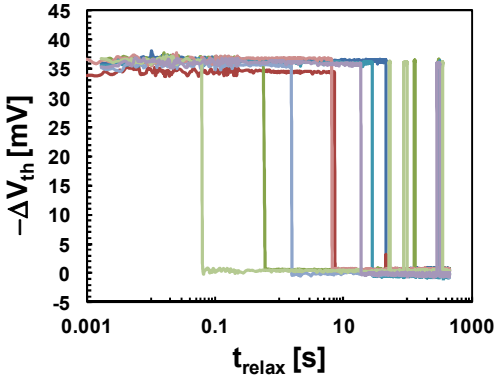

Figure 4. Ten typical relaxation traces recorded on the same device from a larger, 315 device set: one single dominant trap is observed, with ΔV_{th}≈35mV and τ_e>1s. Such device is experimentally suitable for the single trapped charge I_D-V_G measurement (see Fig.5). Note the random telegraph noise (RTN) signal produced by the same trap in some cases [16].

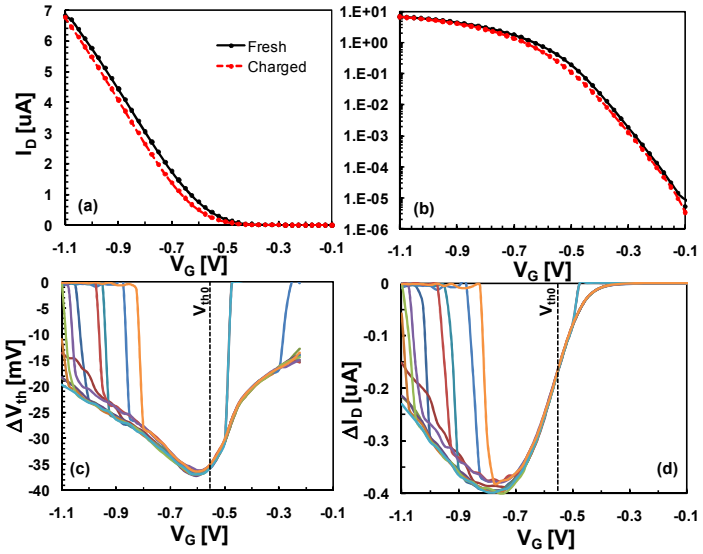

Figure 5. (a,b) I_D-V_G curves measured on the device characterized in Fig. 4, *with the single oxide defect uncharged and charged* (lin and log I_D scales). The characteristic shift can be described as (c) a ΔV_{th} shift (defined as a simple "geometrical" horizontal distance of the 2 curves at a given V_G) or (d) a ΔI_D (vertical) shift. This particular defect on this given device shows a V_G-dependent ΔV_{th}, with a maximum ΔV_{th} for V_G slightly above V_{th0}. In this case, the maximum ΔI_D is observed for V_G corresponding to the maximum transconductance (g_m). The measurements were repeated 12 times (c,d) with excellent reproducibility (note the single charge was emitted prematurely in some cases).

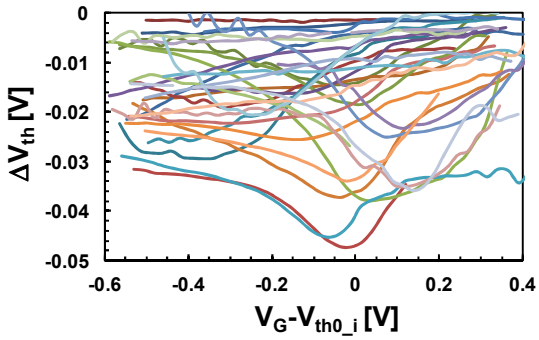

Figure 6. (a) Different $\Delta V_{th}(V_G)$ defect characteristics are found when measuring 30 different (but nominally identical) devices before and after the capture of a single hole. Note that these devices were chosen to show large impact of the single charged gate oxide defect and do not represent the entire population.

From *3D atomistic device simulations*, performed with the Glasgow 'atomistic' simulator GARAND [17] (Fig. 7), different characteristics are expected as a function of the distance (r) between the oxide trap and the critical spot of the channel current percolation path: the maximum ΔV_{th} near V_{th0} is ascribed to a trap located directly above the critical spot, while a larger ΔV_{th} at $|V_G|>>|V_{th0}|$ is expected for a trap located far from the critical spot (Fig. 8) [18].

The measured $\Delta V_{th}(V_G)$ characteristics shown in Fig. 6 can therefore be grouped by similar properties, depending on r (Fig. 9). Each group compares favorably with the device simulation, notably correctly predicting an *apparent mobility increase* after the capture of a single charge close to the critical spot (see Fig 9 a-f).

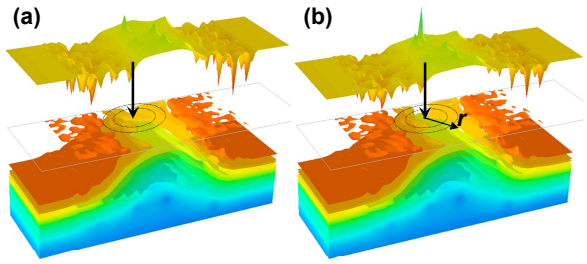

Figure 7. 3D atomistic simulations [16] of (a) a nanoscaled device showing a current percolation path located close to one longitudinal channel edge. (b) An oxide defect located exactly above the critical confinement spot of the current percolation path (demarcated by the vertical arrow) can effectively suppress the channel current when charged. The simulations show the defect impact on the device characteristics depends on the radial distance r from the critical spot.

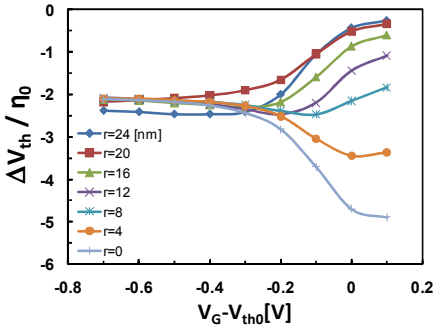

Figure 8. 3D atomistic device simulations results: different $\Delta V_{th}(V_G)$ characteristics are expected as a function of r: a maximum ΔV_{th} for $V_G \approx V_{th0}$ is ascribed to a charged trap located directly above the critical spot, while a larger ΔV_{th} for increasing $|V_G|$ is expected for a trap located further from the critical spot.

Finally, Fig. 10 shows that, according to the simulation results shown in Fig. 8, the probability of getting a given ΔV_{th} appears to be an exponential distribution when sensing at $V_G \approx V_{th0}$ as normally done for η estimation (cf. Fig. 1b). The additional variation in $\Delta V_{th}(V_G)$ observed in Fig. 6 is ascribed to the variation in the confinement magnitude of the critical percolation spot due to different dopant configurations. It is worth noting that the V_{th} shifts which are largest at V_G around V_{th0}, are strongly *reduced at higher* $|V_G$*'s*$|$ (see Fig. 8 and 9a-b) where the FETs are typically operated. The resulting ΔVth distributions at higher sense $|V_G|$ are consequently expected to be narrower than the distributions customarily measured at $V_{Gsense} \approx V_{th0}$, hence relaxing the device lifetime distribution prediction at operating conditions [19].

IV. Conclusions

We have reported extensive statistical reliability measurements performed on different device technologies, based on which we have experimentally observed the η scaling being proportional to A^{-1} for deeply scaled finFETs. Optimized undoped SiGe channel devices showed reduced N_T and η, confirming the superior NBTI robustness (i.e., reduced time-dependent variability) of the SiGe technology. However, the

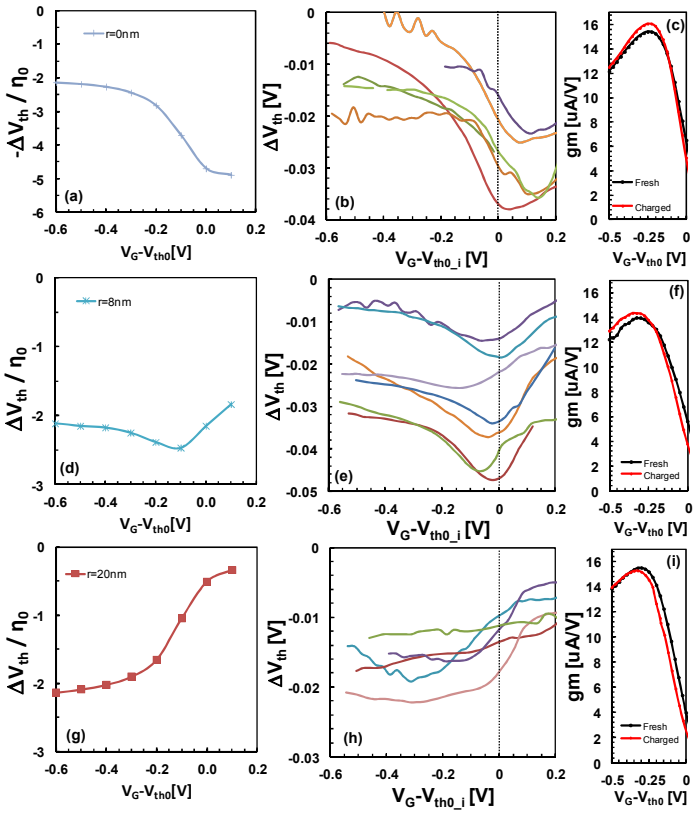

Figure 9. The simulated (a,d,g) and measured (b,e,h) $\Delta V_{th}(V_G)$ characteristics for different nanoscaled devices, grouped by similar properties. Three typical cases are shown: (a,b) a peak ΔV_{th} for $V_G \approx V_{th0}$ is ascribed to a defect positioned above the critical spot; (d,e) a peak ΔV_{th} for $|V_G| > |V_{th0}|$ is ascribed to a defect positioned at a medium distance, while (g,h) an increasing $\Delta V_{th}(V_G)$ characteristics is due to a trap far away from the critical spot. The measured curves compare favorably with the simulated behavior, supporting the proposed interpretation. (c,f,i) The apparent mobility *increases/decreases* after the capture of a single charge close/away from to the critical spot.

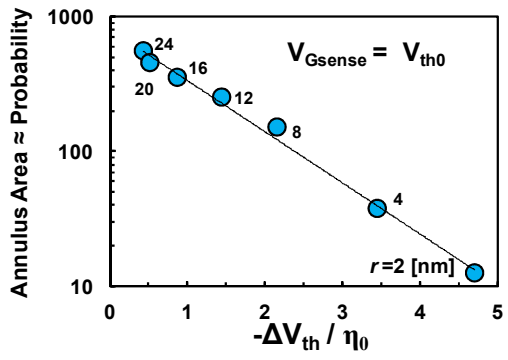

Figure 10. The channel area can be divided into concentric annuli with increasing r, centered on the critical spot (see Fig. 7). The probability of finding a trap in a given annulus (i.e. the probability to have a trap with a given characteristic, see Fig. 8) is proportional to the area of each annulus. This interpretation makes the probability of getting a given ΔV_{th} appear exponentially distributed, as observed experimentally (Fig. 1b).

severe 1/*area* scaling rule observed might jeopardize the reliability prediction of further scaled nodes also for this promising technology.

In order to refine the reliability prediction, we assessed the impact of individual charged gate oxide defects on the nanoscaled device characteristics at increasing sense gate voltages (up to operating V_G), by means of measuring the entire FET I_D-V_G before and after the capture of a single hole. Comparing with 3D atomistic device simulations, we have identified different I_D-V_G behaviors, depending on the location of the oxide defect w.r.t. the critical spot of the current percolation path in the channel. In the light of these observations, the ΔV_{th} distributions at operating conditions are expected to be narrower than the distributions customarily measured at $V_{Gsense} \approx V_{th0}$, hence relaxing the device lifetime distribution prediction at operating conditions. These results should also help in developing the next generation of atomistic circuit simulators.

ACKNOWLEDGMENT

This work was performed as part of imec's Core Partner Program. It has been in part supported by the European Commission under the 7th Framework Programme (Collaborative project MORDRED, contract No. 261868).

REFERENCES

[1] A. Asenov, R. Balasubramaniam, A. R. Brown, and J. H. Davies, "RTS Amplitude in Decananometer MOSFETs: 3-D Simulation Study", in IEEE Trans. Electron Devices, Vol. 50, no. 3, 2003, pp. 839-845.

[2] V. Huard *et al.*, "NBTI Degradation: from Transistor to SRAM Arrays", in *Proc.* IEEE International Reliability Physics Symposium, 2008, pp. 289-300.

[3] M. Toledano-Luque *et al.*, "Response of a Single Trap to AC Negative Bias Temperature Stress, in *Proc.* IEEE International Reliability Physics Symposium, 2011, pp. 364-371.

[4] V. Huard, F. Cacho, Y. Mamy Randriamihaja, A. Bravaix, "From Defects Creation to Circuit Reliability", in Microelectronic Engineering, Vol. 88, no. 7, 2011, pp. 1396-1407.

[5] T. Grasser *et al.*, "Recent Advances in Understanding the Bias Temperature Instability", in *Proc.* IEEE International Electron Device Meeting, 2010, pp. 82-85.

[6] M. Nafria *et al.*, "Time-dependent Variability of high-k based MOS devices: nanoscale characterization and inclusion in circuit simulators", in *Proc.* IEEE International Electron Device Meeting, 2011, pp. 127-130.

[7] B. Kaczer *et al.*, "Atomistic Approach to Variability of Bias-Temperature Instability in Circuit Simulations", in *Proc.* IEEE International Reliability Physics Symposium, 2011, pp. 915-919.

[8] A. R. Brown, V. Huard, and A. Asenov, "Statistical Simulation of Progressive NBTI Degradation in a 45-nm Technology pMOSFET", in IEEE Trans. Electron Devices, Vol. 57, no. 9, 2010, pp. 2320-2323.

[9] B. Kaczer *et al.*, "Origin of NBTI Variability in Deeply Scaled pFETs", in *Proc.* IEEE International Reliability Physics Symposium, 2010, pp. 26-32.

[10] A. Ghetti, C.M. Compagnoni, A.S. Spinelli, A. Visconti, "Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Deca-Nanometer Flash Memories", in IEEE Trans. Electron Devices, Vol. 56, no. 8, 2009, pp. 1746-1752.

[11] K. Sonoda, K. Ishikawa, T. Eimori, O. Tsuchiya, "Discrete Dopant Effects on Statistical Variation of Random Telegraph Signal Magnitude", in IEEE Trans. Electron Devices, Vol. 54, no. 8, 2007, pp. 1918-1925.

[12] T. Chiarella et al., "Benchmarking SOI and bulk FinFET alternatives for PLANAR CMOS scaling succession", in Solid-State Electronics, Vol. 54,. No. 9, 2010, pp. 855-860.

[13] J. Franco *et al.*, "Superior NBTI Reliability of SiGe Channel pMOSFETs: Replacement Gate, FinFETs, and impact of Body Bias", in *Proc.* IEDM, pp. 445-448, 2011.

[14] J. Franco *et al.*, "On the impact of the Si passivation layer thickness on the NBTI of nanoscaled $Si_{0.45}Ge_{0.55}$ pMOSFETs", in Micr. Eng., Vol. 88, No. 7, pp. 1388-1391, 2011.

[15] M. Toledano-Luque *et al.*, "From Mean Values to Distributions of BTI Lifetime of Deeply Scaled FETs through Atomistic Understanding of the Degradation", in *Proc.* VLSI Symp. 2011, pp. 152-153.

[16] T. Grasser *et al.*, "Switching Oxide Traps as the Missing Link Between Negative Bias Temperature Instability and Random Telegraph Noise", in *Proc.* IEEE International Eelctron Device Meeting, 2009, pp.729-732.

[17] http://www.goldstandardsimulations.com/services/service-simulations/reliability-sources/

[18] M.F. Bukhori, T. Grasser, B. Kaczer, H. Reisinger, A. Asenov, in *et al.*, in *Proc.* IEEE International Integrated Reliability Workshop, 2010, pp. 76-79.

[19] B. Kaczer *et al.*, "The Relevance of Deeply-Scaled FETs Threshold Voltage Shift for Operation Lifetime", in *Proc.* IEEE International Reliability Physics Symposium, 2012, *in press*.